Tamper Respondent Envelope Solutions Realized by Additive Manufacturing


Fraunhofer Institute for Electronic Nano Systems, Chemnitz, Germany
Chemnitz University of Technology, Center of Microtechnology

Smart Packaging Solutions for Secure Applications
Motivation for tamper responded envelopes
Technologies to enable customizable tamper responded envelopes
Process Chain and build-up insights
Reliability and security investigations
Conclusion
Motivation
Functionalized Packaging Components as tamper responded secure features

A new security tool box for secure electronic systems is introduced by cooperation between
- Thales – System Architecture, Electronic Design, Use Cases and Reliability Characterizations
- AT&S – Embedding of Active and Passive Components into PCB
- Nanium – Secure System in Package Solutions
- Epoche&Espri – Security Evaluation
- FRAUNHOFER ENAS – Tamper Responded Envelope Solutions

Combining the Know-How of all partners a novel high-tech security toolbox for electronic systems is presented
Technologies
Concept

Process development to enable a scalable, 3D ready process chain capable of fabricating fine feature tamper detection envelope solution for electronic systems with a lot sizes from 1-10000 pieces.

Needed:

- Digital fine pitch, 3D ready deposition process for conductive materials
- Conformal dielectric coating technology for 3D substrates
- Process for via fabrication to enable a multilayer mesh approach

Low temperature processes < 150°C to enable the usage of sensitive / polymer / low cost substrates
Within UNSETH a **novel process flow** is introduced to fabricate **customized tamper detection** components for electronic packages.
Technologies
Aerosol Jet Printing

Toolbox

a. Mask: mask less → digital manufacturing using i.e. dxf file

b. Pneumatic or ultrasonic atomizer, impactor, shutter and print head

c. X&Y vacuum table to move the substrate

d. Material: Ink system [colors, insulators, solder, metals, etchants, ...]

Source: www.AZONANO.com

Technologies
Aerosol Jet Printing

Toolbox

a. Layout file
b. Printhead and shutter
c. Ink system
Technologies
Aerosol Jet Printing

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Example / Demo: printing on PCB, overprinting mold

Aerosol - Jet Toolbox
Layout file

Ink system
Technologies
Aerosol Jet Printing

- 300 x 300 mm x-y-Vacuum stage
- Print Speed: max. 200 mm/s
- 2 Atomizer systems
  - Pneumatic Atomizer [1cP – 1000cP, 15ml fluid]
  - Ultrasonic Atomizer [1cP – 5cP, 1ml fluid]
- Aerosol-, Ink- and substrate heater
- Fine feature print head [min. line width 10 µm]
- Laser-Curing-System [IR Laser, 700mW, 830nm]
- Material in-flight mixing option

Equipment at ENAS

Application Examples

- 3D Metallization
  - High resolution Interconnects
- Flexible Packaging
  - Integration of electrical components
- Fine-Line Metallization
  - up to 10 µm printable feature sizes
- Vertical system integration
  - Printed interconnects for SiP
Technologies

Parylene C CVD

- Conformal coating close to room temperature < 5% thickness variation
- Conformal coating for high aspect ratio patterns
- Conformal coating for 3D objects (Chemical vapor deposition)
- Highly transparent (security aspect)
- Good moisture barrier
- Stable $\varepsilon_r \sim 3,3$

**Properties of Parylene C**

<table>
<thead>
<tr>
<th>Property</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Melting point</td>
<td>290°C</td>
</tr>
<tr>
<td>Temperature stability</td>
<td>125°C</td>
</tr>
<tr>
<td>Peak Temperature</td>
<td>200°C</td>
</tr>
<tr>
<td>Water absorption in 24h</td>
<td>0.06%</td>
</tr>
</tbody>
</table>

Equipment at ENAS

Applications Examples

- Conformal Parylene Coating
  - X-section TSV Top
  - X-section TSV Bottom
Technologies
Laser Ablation

- 355nm wavelength has been developed for 50 \( \mu m \times 200 \ \mu m \) vias for 1 \( \mu m \) and 2.5\( \mu m \) thick Parylene C.

Microscopy of 200 \( \mu m \times 50 \ \mu m \) Via

Schematic cross section of via process

Multi-Wavelength PS Laser

<table>
<thead>
<tr>
<th>Wavelength</th>
</tr>
</thead>
<tbody>
<tr>
<td>266 nm</td>
</tr>
<tr>
<td>355 nm</td>
</tr>
<tr>
<td>532 nm</td>
</tr>
<tr>
<td>1064 nm</td>
</tr>
</tbody>
</table>

Application Examples

- \( \mu \) Fluidic
  - patterned glass wafer
- PCB-Cu-Au-Parylene
- Silicon
  - cutting, treches, vias
Results
Fabricated Demonstrators

- AJP + Parylene CVD + Laser Via process enables reliable multilayer mesh build

| Build up | 2 x conductive Mesh layers  
|          | 2 x dielectric Parylene C layers  
|          | 1 x via layer  
| MESH     | 4 independent loops (each ~ 3m)  
|          | (Line width ~ 150µm, Spacing ~ 250µm)  

FIB cross-sections of via area  
Top View Secure envelope
Results

Fabricated Demonstrators

- **Materials**
  - Conductive Mesh: Ag Nanoparticle Ink
  - Dielectric: Parylene C
  - Substrate: PPS (GF enhanced)

- **Fabrication**
  - Combination of AJP, CVD, Laserablation
  - All processes less than 125°C

- **Electrical properties**
  - Via < 5Ω
  - Printed Tracks < 1kΩ/m

- **Security**
  - Line/Space: 150/250µm
  - Evaluation ongoing

- **Reliability**
  - Tested

FIB cross-sections showing the relation of multilayer mesh and metal tap for interconnection towards PCB
## Reliability investigations

### Conclusion

**Tested**
- Multilayer Build-Up 2xAg layers, 2xparylene layers, laser vias
- Interconnection approach (Pogo pin, metal tap)

→ Combination of printed Ag nanomaterial and Parylene dielectric layer is a reliable material concept

<table>
<thead>
<tr>
<th>Test</th>
<th>Result</th>
<th>Comments</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Thermal Cycling</strong> -55°C/125°C, 30min</td>
<td>&gt; 500 cycles passed</td>
<td>No failures detected</td>
</tr>
<tr>
<td><strong>Thermal Storage @125°C</strong></td>
<td>1000h passed, within + 5% resistance change</td>
<td>No delamination, no cracks</td>
</tr>
<tr>
<td><strong>Torsion Test 7° &amp; 10° at 30°</strong></td>
<td>&gt; 20,000 cycles passed @ 7°</td>
<td>Test performed with CAP on PCB → PCB components will fail 1st</td>
</tr>
<tr>
<td><strong>Vibration Test</strong></td>
<td>Passed Step-Stress Test @ resonance frequency</td>
<td>Test mainly dedicated to test the pogo pin interconnection → PCB components will fail 1st</td>
</tr>
<tr>
<td><strong>Pull Test &amp; Shear Test</strong></td>
<td>Adhesion for Ag nanoparticle ink on different substrate materials available</td>
<td>Pretreatment procedure developed before the printing step (Ar/O₂ plasma treatment)</td>
</tr>
</tbody>
</table>
Reliability investigations

XRAY for security

- XRAY Invisibility for full area cap scan
  - Resolution limited (> 50µm) when analyzing the 164 x 110 CAP substrate
Reliability investigations
XRAY for security

- XRAY Invisibility for full area cap scan
  - Resolution limited (> 50µm) when analyzing the 164 mm x 110 mm CAP substrate

- Idea of Mesh Build achievable for small area scan
  - High resolution scan (without damaging/cutting the substrate ~7µm) on 14 mm x 10 mm

Not easy to enter!
Enormous effort is needed to understand the secure mesh build-up even when using HighEnd XRAY Tomography

Printed tracks visible but multilayer build-up not clear
Conclusion

- Secure tamper respondent envelope presented
  - Realized by digital additive manufacturing
  - Lot size 1 could be realized / design could be changed with each product

- Scalable and customizable process chain developed and tested
  - Process temperatures < 125°C
  - Suitable for low cost polymers
  - Process flow is transferable to other substrates and geometries

- Reliability investigations show that the combination of Ag nanoparticle Ink and Parylene C enables multilayer mesh approach

→ Outlook: full security evaluation for the system (CAP, SiP, PCB)
Thank you for your attention!

Contact:
Frank Roscher
Frank.Roscher@enas.fraunhofer.de

Fraunhofer ENAS
Department System Packaging
Technologie Campus 3
09126 Chemnitz
Germany

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Motivation

Nanoparticle Inks/Pastes – Post-treatment and sintering

- Suspensions of metal particles in solvents and binders
- Pretreatment for dense layer and electrical conductivity:
  - Drying out solvents, burning out organic shells, sintering

Sintering without pressure

- Particle necking due to diffusion effects

Experimental Setup

- Sintering of Ag Nanoparticles and SEM investigation at different temperature steps

SEM Investigation - Sintering of Ag Nanoparticles and grain size at 60°C, 100°C, 200°C, 250°C, 300°C
Technologies

Concept & Process flow (schematic)

- PPS Substrate
- Parylene coating
- Fiducials AJP
- Bottom layer AJP in two steps
- Parylene coating

- Laser via opening
- Middle layer AJP in two steps
- Parylene coating
- Laser via opening
- Top layer AJP in two steps