Next generation of electronic systems: Challenges and solutions for microelectronic packaging

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Outline

Microelectronic Packaging: Situation Analysis

Microelectronic Packaging DNA

Driving Factors, Examples

Wafer Level- and Panel Level Packaging

History
Microelectronic Packaging: Situation Analysis

Market Changes
- Consumer wants more & more functionality – MEMs, Sensors & more.
- Product Cost expectations are given
- Smart Phone superseded PC as the Market Driver
- Dynamic consumer business = new players dominating

With the mobile and smart phone era, the packaging industry is experiencing a flowering of new packages and reinvention of traditional packages.
Re-inventing Packaging DNA

History
• For 40+ years, basic packaging DNA has been Au wirebond & Flip Chip
• Au wire bond was the interconnect work horse for the industry
• QFP, BGA and QFN were major innovations
• Flip Chip BGA on ceramic and on organic substrates have been the package of choice for PC MPU & GPU.

In last couple years, we have introduced new DNA:
• Cu Wirebond
• Flip Chip Cu Pillar
• Wafer level Packaging: WLCSP + WL fanout
• Embedded technologies
• 2.5 D Interposer – TXV
• 3D Packaging
• Heterogeneous integration
ASE Group Technology Roadmap

Moore’s Law

90 nm
65 nm
45 / 40 nm
32 / 28 nm

1st Generation
LF & TAB

2nd Generation
BGA

3rd Generation
FC & 3D SiP

4th Generation
Opto/MEMS integration

CPI

Heterogeneous Integration

Wireless Interconnect

Optical Interconnect

Ref.: Jioso & ASE
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„THIN AND SMALL IS IN“
Example: Development of highly efficient SiC-Solar inverter

Packaging of Modules

Optimization of power loss

State of the art: Si, 16 kHz, 45 kg

IZM Gen1: SiC, 48 kHz, 15 kg

IZM Gen 2: SiC, 250 kHz, 3 kg < 1 liter?

Mechanical and electrical design with EMC

Thermal simulation and design
Google's Little Box Challenge; A $1 Million Prize For Creating A Better, Smaller, Solar Power Inverter

10.05.2014

Today at an event with President Obama, we announced the Little Box Challenge, a $1 million prize to develop the next generation of power inverters. This prize is one of Google’s many efforts to advance a clean energy future. We have a goal of powering our operations with 100% renewable energy, and to that end have contracted over a gigawatt of wind energy for our data centers. Beyond powering our own operations, we’ve also committed over $1 billion to 16 renewable energy projects around the world. Keep an eye on www.littleboxchallenge.com for more information in the coming months!
Example: Miniaturized Wafer-Level-Camera

- Wafer level integration of optics and camera electronics
- Module size: 0.7 x 0.7 x 1.0 mm³
- Application: Medical Devices

Courtesy of Awaiba
Wafer Level Systemintegration

- Thinfilm technologies, Bumping
- Wafer thinning, Thin Wafer Handling
- Through Silicon Via (TSV) Formation
- High density metallization, redistribution
- Interposer, assembly and interconnection technologies
Demonstrators with Embedded Components
Manufactured at IZM on Panel Level

Power

Ultra-low inductance power module
600 V / 20 A with DC link inductance
below 8 nH (today’s world record)

Signal Processing

Modular camera with embedded 32 bit image processor, 2 memory chips, 4 voltage regulators and 72 passives
Solutions with polymer substrates

Panel Level Systemintegration

- High density wiring
- High K and low K dielectrics
- Thin chip handling and assembly
- Ultra thin interconnects
- Embedded actives and passives
- Functional layer integration
Roadmap Panel Level and Wafer Level

Source: Yole
Panel Level is: The intelligent combination of
Wafer Level Processing and Printed Circuit Board Processing

- Finer lines and spaces in combination with semiconductor equipment and organic substrates
- Embedding of bare dies into organic substrates
The New DNA for Power Packaging

Integration of components into organic substrate structures

replacement of bond wires by plated Cu connections

Al wire bonded IGBT on DCB embedded MOSFET
Power Chip Embedding - Opportunities

wire bonding on DCB

embedding

➔ strong restriction of designs by technological limits

➔ a huge design space is open for exploration
History and DNA of Fraunhofer IZM!
2008: Independence of Prof. Geßner’s group

Groundbreaking ceremony in Chemnitz

Since that time we established a good cooperation between IZM an ENAS, and many personal relationships have been the result of this cooperation
Congratulations to the 60th birthday of Prof. Thomas Geßner
(Pioneer in Microtechnology)

Staff: Fraunhofer IZM