Electrodeposition of Aluminum towards wafer level thermo compression bonding

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Electrodeposition of Al: Why?

**Microsystem technology**
- Al as conducting and connection material
- Al as bonding material → assembly and packaging
- Al and its anodized layer → medical applications, micro fluidics, micro reactors, insulated micro coils
- Al as optical material due to highly reflective character → micro optics

**Printed circuit board**
- Cu as metal for numerous of applications
  - Electricity net (buried cables)
  - Electrode material in Li-Ion batteries
  - PCBs
  - Supply bottlenecks for PCB industry
- Al as alternative material due to higher specific conductivity and availability

source: www.ariva.de
Electrodeposition of Al: Why?

Al-Al Thermo compression bonding

State of the Art

- High temperatures and bond pressures needed
- Diffusion is inhibited because of native oxide layer
- Removal of Al oxide prior to bonding not possible (except of in situ plasma treatment)
- Use of thin PVD layers → compression is limited

Why could electroplated Al overcome some current challenges?

- Grains in as-deposited Al layers are thermally active
- ECD-Al shows higher roughness than PVD-Al → cracking of Al oxide layer
- Al as well-malleable material → thicker Al layer as intermediate bonding material can improve the thermo-compression bonding process
- No specific grain orientation
Electrodeposition of Al: How to?

- $E^0_{\text{Al}} = -1.67 \text{ V vs. NHE}$ → deposition from aqueous solutions is not possible
  → ionic liquids (ILs) are used
- ILs= organic salts with a melting temperature < 100 °C
  - Properties are tunable by varying the composition
  - Wide electrochemical window
- Use of EMImCl/AlCl$_3$ 1:1.5 (~150 g/l Al)
- Moisture sensitivity of IL requires inert gas atmosphere
Electrodeposition of Al: Process equipment
Electrodeposition of Al: Process equipment

@ Fraunhofer ENAS:
- Plating setup for 6 inch waferlevel inside a glovebox
- 180 ° tiltable cathode face up, Anode face down

@ NB Technologies:
- Plating in standard fume hood
- deposition cell is rinsed with N₂ during sample exchange
- Cathode face down, anode face up
Electrodeposition of Al: Process development steps

- Electrodeposition process of Al on various substrates developed incl. pretreatment of seed layer
  - Si wafer
  - Glass and ceramics
  - PCBs
- Up-scaling from chip to 4 inch to 6 inch wafer level coating
- Optimization of the plating set up using fluid dynamic simulation
- Pattern Plating with photoresists and selective etching of Cu seed layer
- Showing the feasibility of Al deposition in vertical interconnects down to 200 µm in PCBs (AR: 1:5)

From chip level to wafer level
Optimization of plating equipment
Al as alternative material in PCB industry
Electrodeposition of Al: wafer level plating

- Deposition parameters have to be adjusted for different seed layer
- Al ECD on Al seed layer needs further process development
  ⇒ First bonding trials with Al on Au seed layer
- Deposition on highly doped Si without seed layer possible
  - thermal post treatment necessary for sufficient adhesion
Electrodeposition of Al: wafer level plating

- Preparation of wafers with Au seed layer for bonding trials
- Deposition with same parameters shows reproducible layer thickness
  - Overall average thickness: $8,17 \pm 0,30 \, \mu m$ (12 wafer)
- Some wafers are post treated with CMP
Bonding with electrodeposited Al: overview

<table>
<thead>
<tr>
<th>Wafer ID</th>
<th>Materials</th>
<th>F(MPa)</th>
<th>Temp</th>
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<tr>
<td>1+1 (program error)</td>
<td>ECD+PVD</td>
<td>47</td>
<td>500°</td>
</tr>
<tr>
<td>2+2</td>
<td>ECD+PVD</td>
<td>47</td>
<td>500°</td>
</tr>
<tr>
<td>11+3</td>
<td>ECD+PVD</td>
<td>35</td>
<td>400°</td>
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<tr>
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<td>ECD+PVD</td>
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<td>400°</td>
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<tr>
<td>5+9</td>
<td>ECD+PVD</td>
<td>35</td>
<td>400°</td>
</tr>
</tbody>
</table>

Limit of bonder (EVG540) → are the asperities too high? Substrate cracking?

Temperature reduction

ECD vs ECD Al, What are challenges here?

Same parameters with same behavior?

CMP pretreatment: How is the bonding working without the high roughness
Bonding with electrodeposited Al: dicing yield

Further characterization

- **1+1**: 500 °C, 47 MPa, bond program failure
- **2+2**: 500 °C, 47 MPa
- **11+3**: 400 °C, 35 MPa
- **12+4**: 400 °C, 52 MPa
- **3+13**: 400 °C, 52 MPa, 80 to 60 µm with bond mismatch due to roughness
- **4+14**: 450 °C, 35 MPa
- **16+5**: 450 °C, 35 MPa
- **17+7**: 450 °C, 35 MPa
Bonding with electrodeposited Al: dicing yield

- CMP pretreatment to remove asperities from ECD layer

Nearly 100% dicing yield → missing chips on the edges should not have been bonded due to current collectors
Bonding with electrodeposited Al: cross sections

- High pressure + high temperature result in good bonding without visible interface (1+1, 2+2)
- Bonding of ECD vs. ECD need CMP at least on one side to reduce misalignment
Asperities can be pressed into PVD-Al layer

Roughness is too high to achieve a void-free interface

FIB preparation shows grain structure

- Large grains for ECD-Al

- Grain interdiffusion started on asperities at 400 °C
Bonding with electrodeposited Al: cross sections

- Cross sections look well bonded
- Interface is visible in higher magnifications
- FIB preparation shows large Al grains on ECD side, but small grains on PVD side with no tendency to grow
  → no interaction at the interface due to Al oxide
Bonding with electrodeposited Al: bond strength

- 10 samples per method characterized
- Pull test dependents on glue interface to stud
- Without optimized parameters the strength can be compared to other TCB combinations
Conclusion

- ECD of Al on wafer level is a reproducible process @ ENAS
- ECD-Al peaks can crack the Al oxide layer
  - Roughness to high to compress it
- Parameter scan for Al-Al-TCB
- Bonding with ECD-Al is possible: 400 °C, 35 MPa as lowest parameter set
- CMP can be applied to remove asperities of ECD-Al
- Hermeticity not clear yet
- ECD-Al is thermally active: grains can diffuse together
- PVD-Al is sputtered with highest power → grains are thermally inactive and show no diffusion any more
Outlook

- Deposition process development of Al on Al seed layer ongoing
- Using low power sputtered Al for bonding to achieve better grain diffusion
- Bonding of ECD vs ECD Al with at least one CMP treated side
- Further reduction of bond temperature and pressure
- Detailed pull strength analyzation
- Hermeticity tests
Outlook and Roadmap for ECD-Al

Investigation of the bonding behavior of ECD-Al in Al-Al-Thermo-compression bonding

First results presented

2017 2019 2023 2027

Basics of Al-ECD on various substrate evaluated within AioLi-project

Al in PCBs

Al coated multilayer PCBs incl. via technology and soldering on Al surfaces

Al-Pillars for Flip Chip assembly resulting in an homogeneous package between MEMS, ASIC and PCB

AI-TSVs for MEMS applications and hybrid wafer bonding with Al

Development duration is an estimation: acceleration is possible if industry push it in application cases

Advanced Packaging of all components
Thank you for your attention

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