[Cheminitzer Seminar  23\textsuperscript{th} June, 2015]
A 3D stacked CMOS image sensor with 16Mpixel global-shutter mode using 4 million interconnections

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Conventional Image Sensor

Rolling shutter (RS) operation

› To prevent “rolling shutter distortion”, mechanical shutter is necessity.

Rolling shutter image sensor : line by line exposure
=> It has the distortion when captured moving target
Background (Motivation)

Global shutter (GS) CMOS image sensor (CIS) ideal for digital cameras

- No rolling shutter distortion/no mechanical shutter
  - High speed continuous shooting
  - Seamless shooting between still mode and movie mode
  - No black-out period for electronic view finder
Our Targets

To develop a GS image sensor for digital cameras with:

› High resolution: 16M pixels
› High image quality: 3.8-um BSI pixel
› No artifacts: small parasitic light sensitivity
General Problems of Global Shutter CIS

Storage node in same substrate as Photo Diode (PD)
Storage node beside PD

**Problems**

- PD area decreased because of storage node => Low full well capacity
- Shielding light to storage node difficult => High parasitic light sensitivity
3D stacking technology with micro bumps

- Light
- Carriers
- Si substrate

Light shield
- Interconnection (micro bump)
- Light shield
- Storage node
- Si substrate

**Our Previous Work (ISSCC2013)**

- **Chip size**: 6.5 × 6.5 mm
- **Effective pixels**: 704 (H) × 512 (V)
- **Pixel size**: 4.3 × 4.3 µm
- **Number of interconnections**: 90,112
- **Minimum pitch of interconnection**: 8.6 µm
- **Parasitic light sensitivity (PLS)**: -160 dB
## FSI, BSI, 3D stacked image sensor

<table>
<thead>
<tr>
<th>Structure</th>
<th>FSI</th>
<th>BSI</th>
<th>3D stacked</th>
</tr>
</thead>
<tbody>
<tr>
<td>Light</td>
<td></td>
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<tr>
<td>Si</td>
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<tr>
<td>PD</td>
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<tr>
<td>Metal</td>
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<tr>
<td>Support wafer</td>
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<tr>
<td>Circuit wafer</td>
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</table>

### Feature
- **FSI**: Easy to fabricate
- **BSI**: PD can receive much more light
  - Pixel metal layout is easier
- **3D stacked**: Higher functionality
  - Higher performance

### Process
- **FSI**: Normal CIS process
- **BSI**: Wafer bonding
  - Wafer thinning
- **3D stacked**: Wafer bonding
  - Inter connection
  - Wafer thinning
## Our New Work

### ISSCC2013

<p>| | |</p>
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### New Target

- Bigger chip size
- Higher resolution
- Smaller pixel size
- Higher number
- Smaller pitch
- Keep high performance
- Better image quality
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  - Future work
Appearance of Die

Chip Size
20.1 × 19.7 (mm)

Pixel Area
17.5 × 13.2 (mm)

Effective Pixels
4608 × 3480

Pixel Size
3.8 × 3.8 (µm)
Device Structure

7.6-µm micro bump pitch

Cross Section
Schematic of a pixel unit circuit

- Souse Follower output
- For SF in global readout
- Clamp_Cap
- S-H_Cap
Timing Diagram of Image Sensor

Timing from PD to storage node in GS mode

=> 4-time frame reset & transfer

Reset and signal levels are readout for pixel CDS.

1st  2nd  3rd  4th

4-time frame reset  Exposure  4-time frame transfer

100us  100us
Timing Diagram of Image Sensor

Timing from storage node to column circuit in GS mode

=> Rolling readout at 5 fps

Ref. and signal levels are readout for column CDS.
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Captured Image : Color sample

16Mpixel high resolution image with On-chip color filter
Captured Image : B/W sample

Scene: A target (a fan) moving very fast
Tint: 125us

Captured in RS 60-fps mode with a commercially available camera

Captured in GS mode with our image sensor
# Specifications

<table>
<thead>
<tr>
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<th>This work</th>
<th>Previous work</th>
</tr>
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<tbody>
<tr>
<td>Fabrication process of top substrate</td>
<td>0.18-µm 1P6M</td>
<td>0.18-µm 1P6M</td>
</tr>
<tr>
<td>Fabrication process of bottom substrate</td>
<td>0.13-µm 1P6M</td>
<td>0.18-µm 1P6M</td>
</tr>
<tr>
<td>Chip size</td>
<td>20.1 × 19.66 mm</td>
<td>6.5 × 6.5 mm</td>
</tr>
<tr>
<td>Pixel area size</td>
<td>17.51 × 13.22 mm</td>
<td>3.03 × 2.20 mm</td>
</tr>
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<td>4608 (H) × 3480 (V)</td>
<td>704 (H) × 512 (V)</td>
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<td>3.8 × 3.8 µm</td>
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</tr>
<tr>
<td>Read out rate</td>
<td>5 fps</td>
<td>30 fps</td>
</tr>
<tr>
<td>Supply voltage</td>
<td>3.3 V</td>
<td>3.3 V</td>
</tr>
<tr>
<td>Number of interconnections in pixel array area</td>
<td>4,008,960</td>
<td>90,112</td>
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- **Bigger**
- **Higher**
- **Finer**
Measurement Results

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<th>Previous work (Pixel Size: 4.3 × 4.3 µm)</th>
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<tr>
<td>Conversion gain</td>
<td>35 µV/h+</td>
<td>26 µV/h+</td>
</tr>
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<td>Full well capacity</td>
<td>35,000 h+</td>
<td>30,000 h+</td>
</tr>
<tr>
<td>Sensitivity with 3200-K light source (B/W sample)</td>
<td>35,000 h+/lxs</td>
<td>60,000 h+/lxs</td>
</tr>
<tr>
<td>Dark current at 60°</td>
<td>50 h+/s</td>
<td>1000 h+/s</td>
</tr>
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<td>Parasitic light sensitivity (PLS)</td>
<td>-180 dB</td>
<td>-160 dB</td>
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Photodiode process and pixel layout were optimized
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Conclusion

◆ Key technology

› Wafer on wafer bonding
› Interconnection at 7.6-µm pitch
› 4 million interconnections in pixel area

◆ Achievements

› 16Mpixel global-shutter function with -180-dB PLS
› High image quality
Future Work

◆ Technology
  - Finer pitch interconnection
  - Improvement sensor specs for global shutter (frame rate, random noise)

◆ Applications
  - Advanced image sensor using pixel level interconnection (minimum chip size, in-pixel ADC, WDR)
  - 3D stacked image sensor with other chips (DSP, memory)