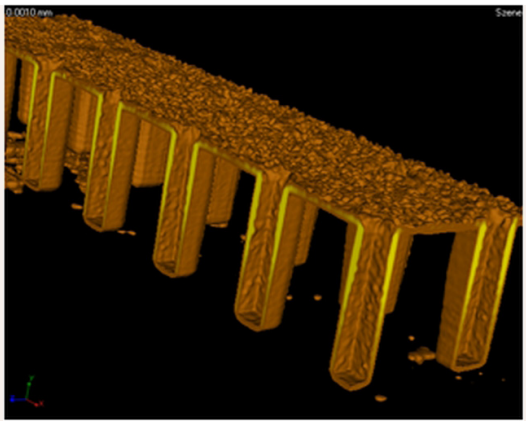
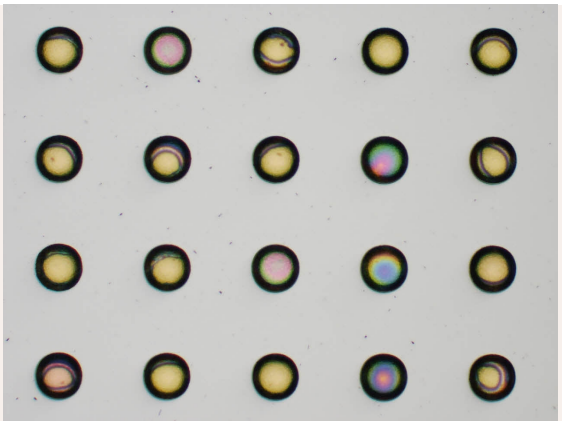
3D INTEGRATION: TSV PROCESSES AND WAFER THINNING





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Vertical Integration of MEMS devices implies the incorporation of various functionalities and materials. Through Substrate Vias (TSVs) with high aspect ratio (AR) add up to further complexity. The major processes within the 3D technology for MEMS comprise substrate thinning, wafer bonding, and TSV fabrication.

Research Topics

The department BEOL has been working in the field of 3D integration for several years with focus on the development of TSV processes and wafer thinning.

Via Etching

The geometry of TSV's has large impact on the subsequent filling with conductive materials. We are developing etch processes for optimized via profiles such as tapered openings.

Via passivation

TEOS processes are used for conformal insulating layers as well as thermally grown oxide layers for best dielectric properties.

Via metallization

TSVs with small diameters (< 3 µm) are filled with a Cu-CVD process. For larger TSVs Cu-CVD seed layers are applied for subsequent Cu-Electroplating (ECD). As diffusion and barrier layer, TiNx is deposited with MOCVD/PECVD. An ECD bottom-up process is used for small aspect ratios (2 – 3) and a conformal process for partial filling of large TSVs.

Wafer thinning

With coarse and fine grinding processes Si, glass or ceramic wafers could be thinned to thicknesses as low as 50 µm. Chemical Mechanical planarization/polishing of various materials is used to achieve mirror-like surfaces e.g. for wafer direct bonding processes. A wet chemical spin etch process ensures the removal of grinding defects and is used for TSV reveal from the wafer backside.

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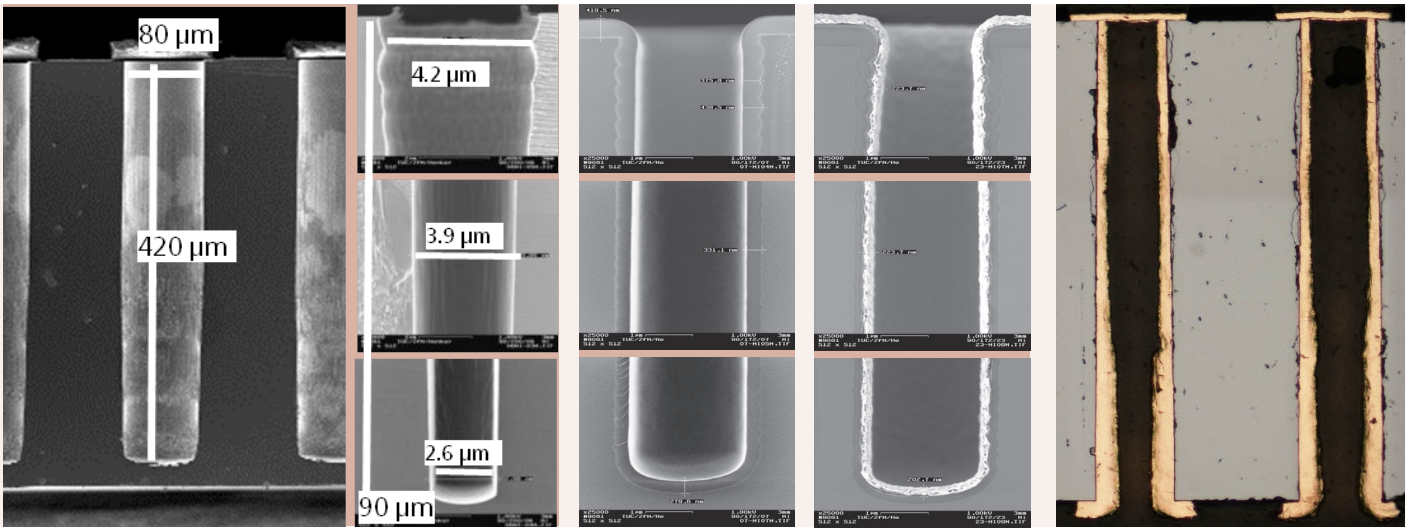

Equipment

Via Etching

- STS with ICP source for wafer sizes of 100 and 150 mm
- SPTS Omega i2L DSi Rapir for 150 mm and 200 mm wafers
- Using Bosch process: SF6 + sidewall passivation
- Mask: photo resist or thermal oxide, or combination of both
- Etch selectivity: to resist > 45% / to SiO_2 > 100%
- Edge exclusion: 7 mm
- Etch rates depends on layout, aspect ratios, sidewall quality: 0,5 µm/min – 10 µm/min
- Aspect ratios up to 15
- TSV size/geometry depends on application: (e.g. 5 x 100 µm … 80 x 450 µm)
- Tapered via openings with 86° (top to sidewall angle)

Via passivation

- Thermally grown oxide in Centrotherm oven for 100 – 200 mm wafers
- TEOS Ozone oxide in an AMAT P5000 for 200 mm wafers (smaller samples via adapter)

Via metallization

- AMAT P5000 for MOCVD Cu and TiNx on 200 mm wafers (smaller samples via adapter)
- Cu-CVD filling for TSVs with DM<5 µm and AR up to ~10
- Step coverage of Cu-CVD seed layers: ~50% for AR~ 9

- RENA EPM 101 tool for ECD of Cu, Ni, Au on wafer size of 100…200 mm
- ECD-TSV filling for AR up to 3.5
- Conformal metallization for large TSVs (diameter > 50 µm)
- Vertical plating tools for ECD of Cu, Ni, Au, Sn on wafer sizes up to 200 mm as well as on customized samples

Wafer thinning

- DISCO DAG 810 grinding tool
- 100 – 200 mm wafers
- Final thickness as low as 50 µm
- Grinding of Si, glass, ceramics

- AMAT Mirra CMP tool
- 150 and 200 mm wafers
- CMP of Si, SiO2, ceramic, metals (Cu, Al, Ni)

- IPEC 472 CMP tool
- CMP of Si, SiO_2 and ceramics on 100 – 200 mm wafers

- G&P 428 brush cleaner
- G&P 412 brush cleaner

- SPS Polos Spin etch tool
- Si etching by using KOH or HNO_3/HF/CH_3COOH chemistry
- 100 – 200 mm wafers
- Removal of grinding defects
- Soft TSV reveal process from the wafer backside

Pictures:
page 1: CT image of TSVs (left); TSV reveal via spin etching (right).
page 2: Different TSV sizes etched via DRIE (left); TEOS ozone isolation and Conformal Cu-MOCVD seed layer (middle); Conformal Cu-ECD TSV metallization (right).

Photo acknowledgements: Fraunhofer ENAS

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