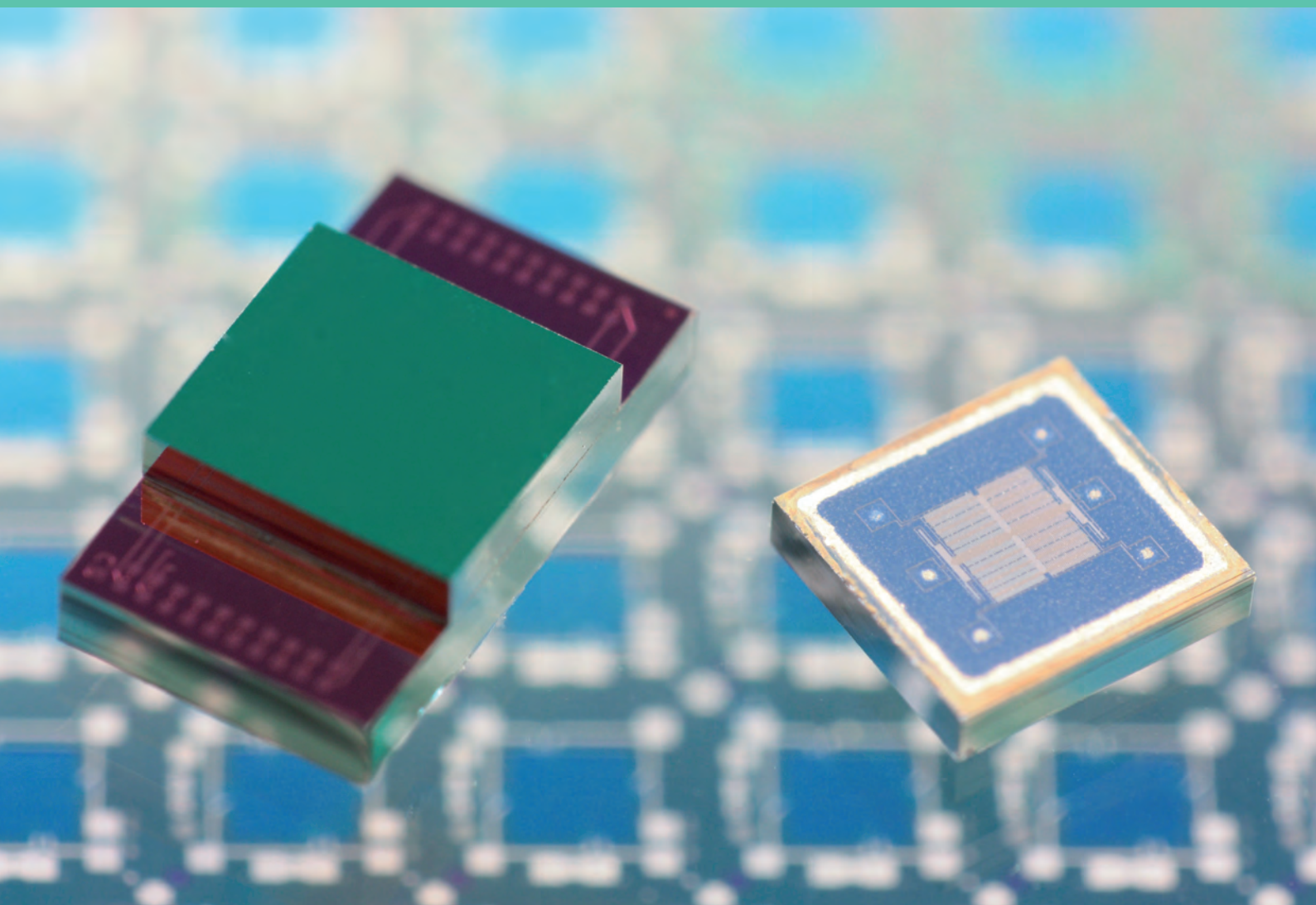
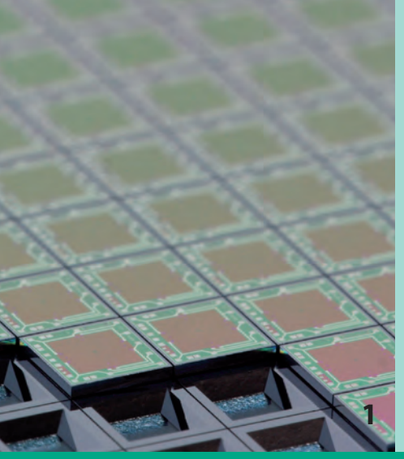
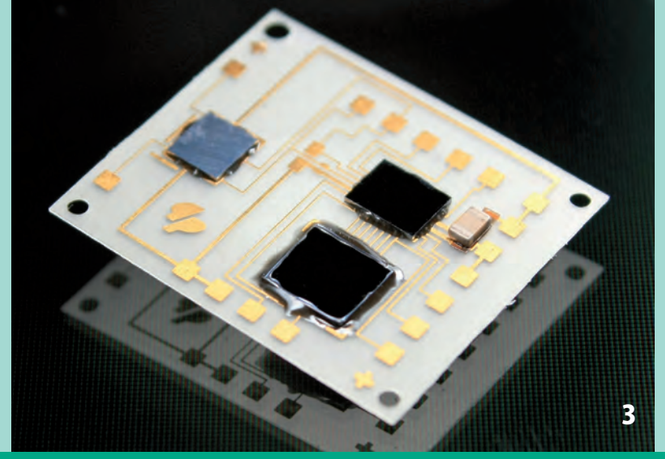
Fraunhofer
ENAS

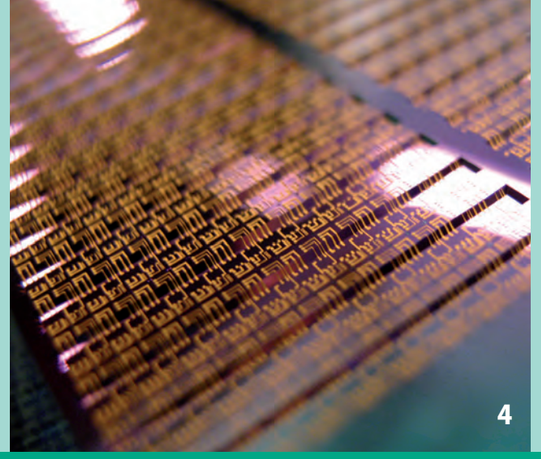
FRAUNHOFER INSTITUTE FOR ELECTRONIC NANO SYSTEMS ENAS

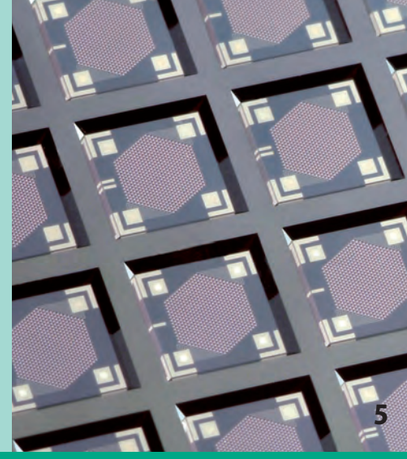
SYSTEM PACKAGING











The actual developments of micro and nano technologies are fascinating. Undoubted they are playing a key role in today's product development and technical progress. With a large variety of different devices, different technologies and materials they enable the integration of mechanical, electrical, optical, chemical, biological, and other functions into one system on minimum space.

The Fraunhofer Institute for Electronic Nano Systems ENAS in Chemnitz focuses on research and development in the fields of Smart Systems Integration by using micro and nano technologies with partners in Germany, Europe and worldwide. Based on prospective industrial needs, Fraunhofer ENAS provides services in:

- Development, design and test of MEMS and NEMS (micro and nano electro mechanical systems),
- Wafer level packaging of MEMS and NEMS,
- Metallization und interconnect systems for micro and nano electronics as well as 3D integration,
- New sensor and system concepts with innovative material systems,
- Integration of printed functionalities into systems,
- Reliability and security of micro and nano systems.

Versatile packaging technologies are focused by the department System Packaging and its applied research. In addition to packaging of MEMS and NEMS at different levels of the packaging hierarchy, also micro and nano patterning of surface areas in micro systems technology is a further main topic.

Besides different wafer bonding techniques, such as silicon direct bonding, anodic, eutectic, adhesive, and glass frit bonding, technologies such as laser assisted bonding, reactive bonding as well as low-temperature and thermo-compression bonding are researched and adapted for special application areas. All wafer bonding techniques are characterized in terms of their bonding quality, strength and hermiticity. The competence of the department involves the dicing, the chip and wire bonding as well as technologies for the integration of complex, miniaturized and even smart systems. The potentials of integration are abundant, ranging from hybrid integration of the components on application-specific substrate carriers over monolithic integration of electronic, sensing and actuating components on a silicon substrate or interposer substrate, to the vertical integration. The 3D stacking is getting more and more important in the fields of chip and wafer level packaging. In addition to the functionality and reliability, the miniaturization and the integration are the greatest challenges for 'More-than-Moore' strategy. With the department's research work this trend results in new, customer-specific applications.

MEMS Packaging and 3D Integration

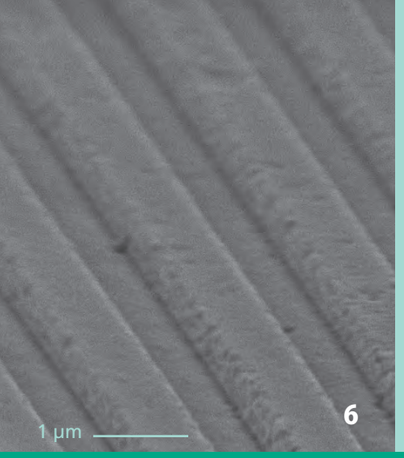
The importance of MEMS packaging can be deduced from its share of production costs of a micro system. Herein, manufacturing costs range from 20 to 95 percent, whereas this wide margin results from specific application requirements. The MEMS package has to allow access for the desired media to be measured, like liquids, gases or light, but at the same it has to protect the sensing part from undesired external influences, and thus to guarantee long-term functionality. Current packaging technologies are not only applied to passive elements such as inertial or gas sensors, but also to active elements like micro mirrors and print heads. In view of the further advanced system integration, electronic components can also be implemented into the MEMS package.

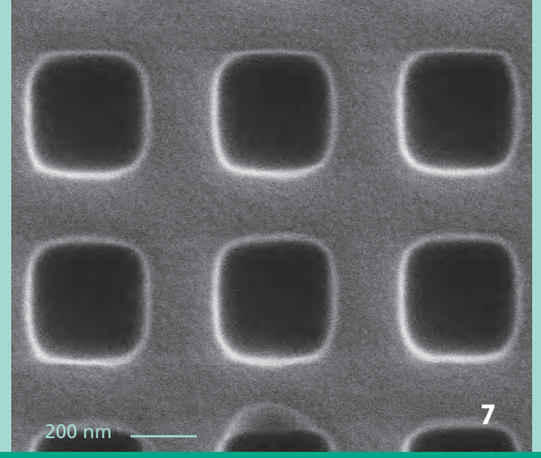
In addition to the integration at wafer level and hybrid integration on chip level, integration technologies in the third dimension are developed. 3D integration has clear advantages. For one, it can reduce the size of a chip and for another it can improve the signal quality. In vertical stacks it is of significant importance to pay attention to the influence of each bonding technology on materials, but also on the electrical and thermal behavior of the whole system. To characterize and evaluate these technologies in terms of their tightness and strength, different measuring tools and valuation guidelines are available at the department System Packaging.

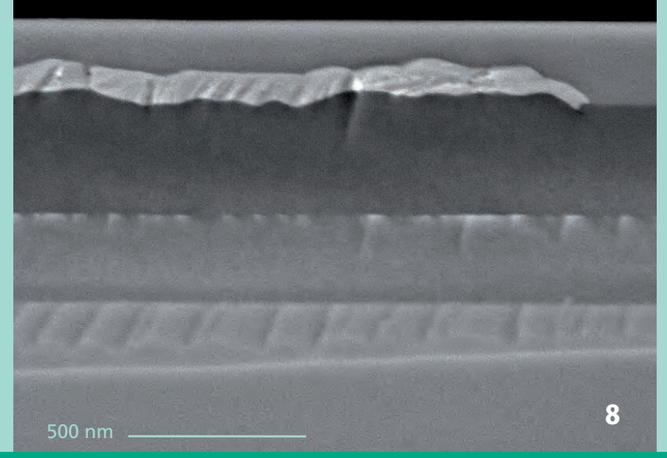
The following key aspects outline the department's work in the field of MEMS packaging:

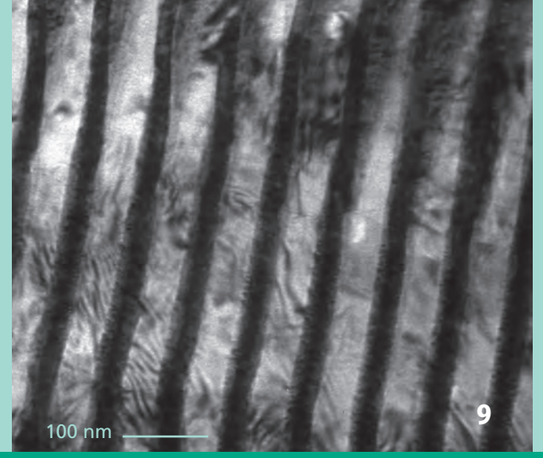
- Wafer level packaging and MEMS packaging
- 3D integration with feedthroughs (Through Silicon Via – TSV)
- Wafer, chip, and wire bonding
- Nano imprint lithography and hot embossing
- Aerosol-jet printing and screen printing
- Spray-coating and spin-on
- Layer deposition using PLD, PVD, and ECD
- Surface activation using CMP and plasma
- Die separation
- Electrical, mechanical, and thermal connecting
- Non-standard electronic substrates and interposer
- Characterization (hermiticity, strength, ultrasonic and IR microscopy)

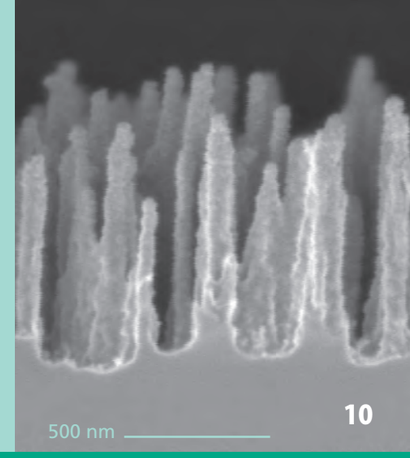
Fig. 1: Pressure sensor bonded at wafer level (in cooperation with Aktiv Sensor GmbH)
Fig. 2: MOEMS packaging (in cooperation with RICOH, Ltd.)
Fig. 3: Hybrid integration using a flexible substrate
Fig. 4: Silicon Interposer with redistribution at wafer level
Fig. 5: Capacitive, micromechanical ultrasonic transducer array











Wafer Bonding

The term wafer bonding describes all techniques for joining two or more wafers with and without interlayers. Standard methods, such as silicon direct bonding, anodic, eutectic, adhesive, and glass frit bonding are used, and adapted for specific requirements. Actual research focuses on low-temperature bonding with process temperatures below 200 °C. Another important field of research for these low-temperature procedures is the usage of nano scale effects and new materials. Examples for nano scale effects are reactive bonding with nano scaled multilayers or the reduction of the melting temperature with only a few nanometer thick interlayers. Moreover, the laser assisted bonding allows selective bonding without any temperature influence on the functional elements. Therefore a Thulium fiber laser with a wavelength of 1908 nm enables the bonding within a transparent range for Silicon using special absorbing interlayers.

Other methods for the technological developments are constituted by the increasing diversity of materials used in micro-systems technology. Materials, in particular plastics, metals, and ceramics are currently analyzed to embrace aspects such as temperature and media resistance and low costs during the product development. One example for this is the polymer bonding, which aims a tight bonding of plastics, covering the whole surface. Moreover, research is done in the fields of thermo-compression bonding and the direct integration of functional ceramics.

The bonding techniques mentioned above are used for wafer level integration of electronic, micromechanical or optical components and are constantly optimized regarding their process parameters for example yield and strength. A complete clean room production line for processing 4 to 8 inch wafers including automatic bond processing as well as characterization equipment is available for wafer level bonding.

Nano Scale Effects

In order to make use of nano effects in MEMS packaging, the department System Packaging analyzes nano scale intermediate layers and layer systems that are deposited with PLD, PVD, and Aerosol jet technologies. Next to PLD and PVD, where nano layers and multi layer systems like metallic, ceramic, oxide, organic or semiconductor-like materials could be deposited on large areas, the Aerosol jet enables the selective printing of metallic nano particles or dielectric inks for conductive paths, insulating layers, bonding frames, material combinations, or layer stacks. Furthermore, surface and material effects are investigated and characterized based on metallic nano structures. These nano structures are applied to new bonding techniques at chip and wafer level. The aim of this procedure is to achieve a permanent and hermetic sealed joint between two wafers, using the lowest temperature influence into the system.

Imprint Technologies

One of the most emerging technologies for transferring nano patterns with single nanometer dimensions is Nano Imprint Lithography realized by imprinting and UV or thermal curing. Molding micro and nano structures by embossing or imprinting them respectively, enables a precise formation of optical and fluidic structures using a master tool. The basic distinction is made between hot and cold embossing processes. Here, the process temperature when hot embossing glass, unsintered ceramics and thermoplastics is above the glass transition temperature of the respective material. The research work of the department does not only include the development of embossing processes, but also the design and production of silicon master tools, optional equipped with anti-sticking layers, as well as tools with patterned photo resist or soft tools and electroplated molded nickel tools (UV-LIGA).

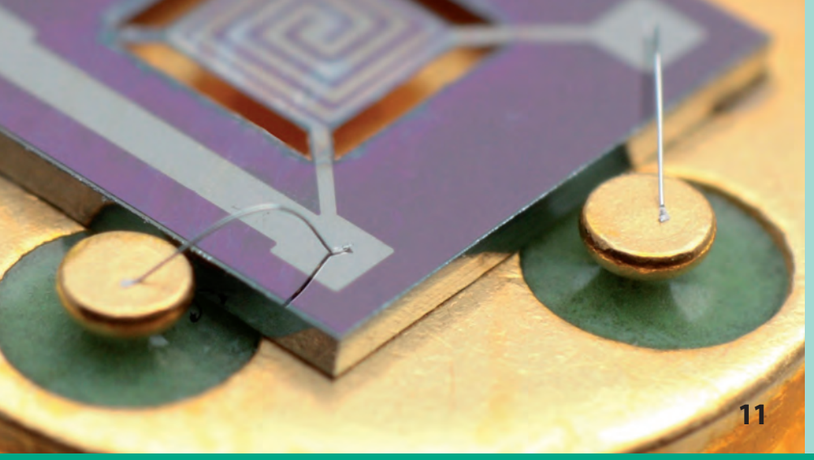
Surface Modification

One aspect that is of great importance when bonding substrates is their surface quality. Whereas, the substrate surface roughness using relatively thick intermediate layers, such as glass paste or epoxy, plays a more or less subordinated role. It is the atomic contact between bonding partners in technologies without intermediate layers that is of great significance. Direct and anodic bonding techniques require surfaces with a roughness of R_a <1 nm. For such techniques a pretreatment through specific processes, like chemical mechanical polishing or plasma activation with special gases, is of importance in order to reach smooth hydrophilic or hydrophobic surfaces.

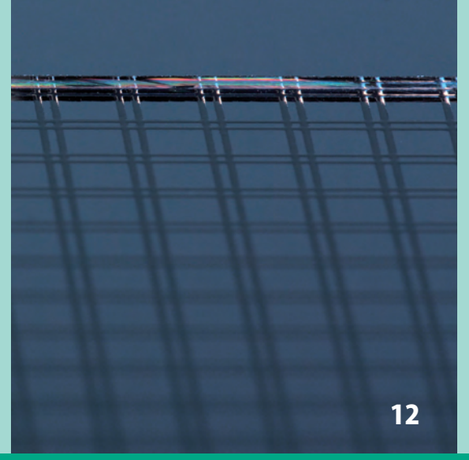
CMP (chemical mechanical polishing) is implemented and developed for microsystems technology as well as in the field of 3D integration. The challenges and subjects of investigation for CMP is the extreme aspect ratio between the structure dimension and the structure distance as well as versatile materials. In addition to the CMP of aluminum, copper, and germanium, which are investigated for 3D integration processes, silicon and silicon dioxide can be polished. This, for instance, is of significance, when producing innovative SOI-substrates with buried silicide layers, which are needed for devices of the BiCMOS-technology.

Besides a wet-chemical pretreatment of the wafer, it is possible to increase the bond strength of direct bonded materials via chemical-reactive plasma discharge. This pretreatment can be applied to the whole area or to local points. Here, similar stable bonds as in high-temperature bonding can be realized, even at curing temperatures of only 200 °C. According to this, new materials and heterogeneous materials with very different coefficients of thermal expansion like Lithium Tantalate and Silicon can be bonded using the activation and the following low-temperature bonding.

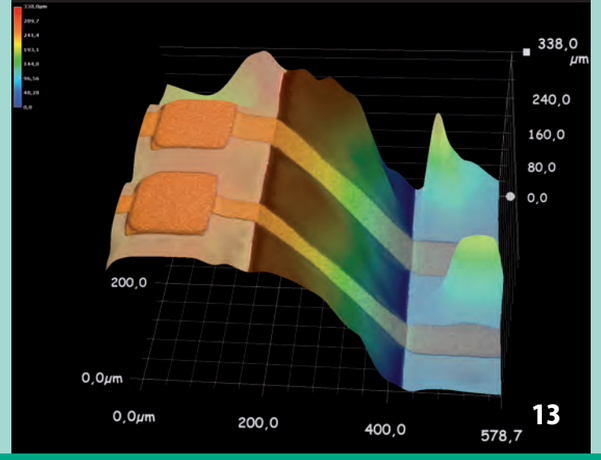
Fig. 6: Sub-micron patterned surface via micro embossing
Fig. 7: Sub-micron patterned resist via nano imprint lithography
Fig. 8: Planarized SOMI-substrate (silicon on metal and isolator) with buried silicide layer
Fig. 9: Nano scale reactive multilayer for wafer bonding
Fig. 10: Nano surface patterning for wafer bonding



11



12



13

14

Aerosol Jet and Screen Printing

Aerosol jet printing enables the selective printing of manifold materials onto different substrates without conventional mask lithography or thin film processes. Additional to the printing of organic materials, adhesives, and biological relevant materials the aerosol-jet process allows the printing of conductive structures and other functional materials. The layers could be printed within a range between 10 µm and 300 µm width. An integrated laser source performs the direct sintering of the deposited inks or particles to increase the conductivity of electrical lines or to optimize the layer properties. Using two atomizers and two deposition heads the printing of two different materials on one substrate is possible.

Screen printing is used for selective patterning of interlayers for wafer bonding. Different paste like materials can be coated over a flexible screen. Here, the structure size mainly depends on the stencil openings given by the wire thickness and the mesh size of the stencil as well as on the composition of the pastes. Current research is done to analyze the minimal printable feature sizes. Glass frit pastes for wafer bonding, but also other materials, like solder pastes or ceramic adhesives, can be printed on up to 250 mm x 250 mm substrates using the equipment under clean room conditions.

Chip Bonding

At packaging level I, chip bonding techniques are used to assemble prefabricated chips on a substrate carrier or in a package. For this bonding, materials such as epoxies, ceramic adhesives, and pastes as well as eutectic solder and other solder compounds are used. In addition to these conventional techniques, a new method is performed. This technique is called reactive bonding and makes chip bonding at room temperature possible using an internal heat source. The main application area is the fabrication of prototype sensors of heat-sensitive micromechanical sensor and actuator systems. The equipment available at Fraunhofer ENAS enables a flexible implementation of all modern packaging technologies, such as flip-chip (FC) and surface mounted devices (SMD). A precise X-Y adjustment for all substrates facilitates an accurate placement of the chips and thus allows a high integration level.

Characterization

Accompanying to current technological developments the packaging technologies are characterized and evaluated. For this reason tensile, pressure and shear tests, electrical tests as well as climate and temperature tests are available in cooperation with other departments of the Fraunhofer ENAS. Wafer bond techniques are in particular characterized in terms of their electrical and mechanical bonding quality, tightness and hermiticity. Here, research methods, such as infrared, ultrasonic and scanning electron microscopy, including FIB and EDX analyses, are applied. Maszara Blade test, Micro-Chevron test and shear test are used to evaluate the bond strength. The hermiticity of bonded wafers or chips is characterized by leakage tests (helium, nitrous oxide) up to a resolution of 1×10^{-11} mbar l/s or they are electrically characterized with integrated resonant structures.

Services and Equipment

The department System Packaging carries out services for industry and research institutions. All research topics and standard processes described above as well as the following equipment are available for service offers whether it would be research or prototyping. One advantage of our institute is that all technologies and processes could be chosen individual and customer-specific.

We offer the following services:

- Research and development orders
- Funded research projects and consulting
- Process and technology transfer
- Patterned and bonded substrates (customer-specific)
- Feasibility and market studies
- Seminars and trainings
- Technology consulting.

Equipment:

- CMP IPEC 472
- Cleaner Suss CL 200
- Bond aligner Suss BA8 and EVG6200NT (NIL)
- Substrate bonder EVG 540, Suss SB 6 and Suss SB 8
- Screen printer R29 Spectrum and MV 100
- Aerosol Jet System 300 CE
- Spin and spray coater
- Creamet 600 S/PLD
- Chip bonder Tresky T-3002-FC3
- Wire bonder FEK delvotec 5450
- High-temperature tube furnace Centrotherm
- Plasma and laser tools
- Wafer saw Disco DFD 6340
- Microscopes (VIS, IR, US, REM)
- Micro-Chevron tester
- Tira Test 2805 (pull, shear tester)
- GOM Aramis optical measurement analytics.

Fig. 11: Packaging of an IR emitter (in cooperation with Siegert TFT GmbH)
Fig. 12: Screen printed glass paste structures
Fig. 13: Analysis of a redistribution line over a 300 µm deep etch cavity
Fig. 14: MHz ultra sonic cleaning for wafer bonding

Contact:

Fraunhofer Institute for Electronic Nano Systems ENAS
Department System Packaging

Technologie-Campus 3
09126 Chemnitz
Germany

Head of the department System Packaging
Dr. Maik Wiemer
Phone: +49 371 45001-160
Fax: +49 371 45001-333
Email: maik.wiemer@enas.fraunhofer.de
Internet: http://www.enas.fraunhofer.de/EN

Front page:
Quasi-monolithic integration of ASIC and MEMS

Photos:
Fraunhofer ENAS, Andreas Morschhauser