



AI-Powered Reliability

RETE Project for  
Semiconductor  
Excellence



ELES S.p.A.

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# ELES Group - Overview



35+ years of continuous innovation in the semiconductor  
Reliability



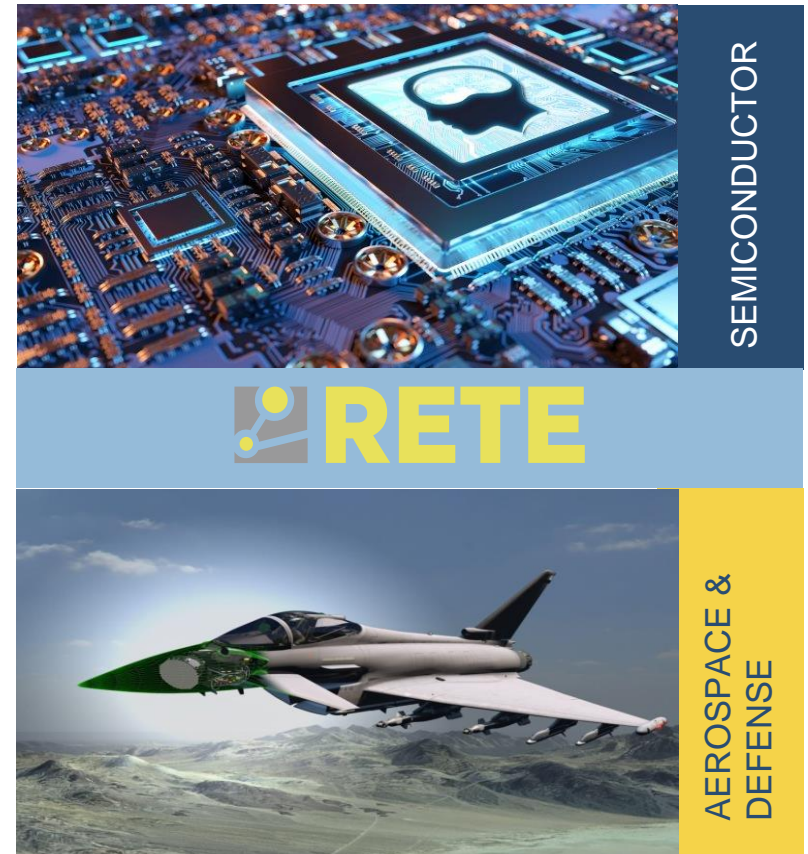
Listed on the stock market in June 2019 to strengthen the  
financial position to support the growth plan



Strategic acquisitions in 2022 to expand the offer in the  
semiconductor market to the testing and strengthen position  
in the aerospace and defense market



Focus on services to support the Customers on the Silicon  
Lifecycle Management and Electronic Module Lifecycle  
Management compliant with the mission critical markets  
needs



# ELES Group - Worldwide installed base



# Reliability Test Vs Technology - Limits

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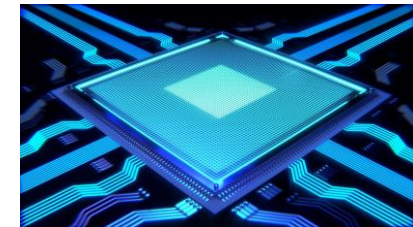
Standard timing for new IC product introduction does not meet market needs

Increasingly limited tests coverage Vs. technology evolution

Failure to take advantage of long Q&R times

PASS/FAIL results with limited sentence

Critical parameters drifts within the tolerance are not reflected for the purposes of the result



Stress Loop  
500 hrs



**Q&R Trial**

**Stress  
w/ limited monitor**

# Ripe times - Why now?

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Case studies confirming the need for an update

ELES - thirty years' experience in semiconductor reliability test



AI advent and data availability

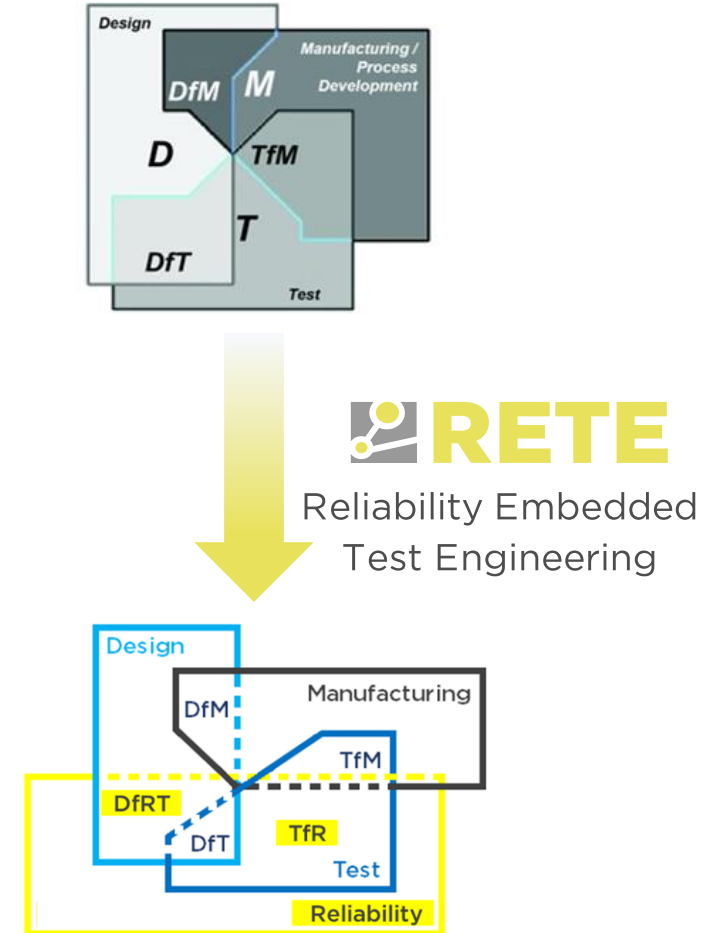


ELES partnership with Fraunhofer to accelerate AI introduction

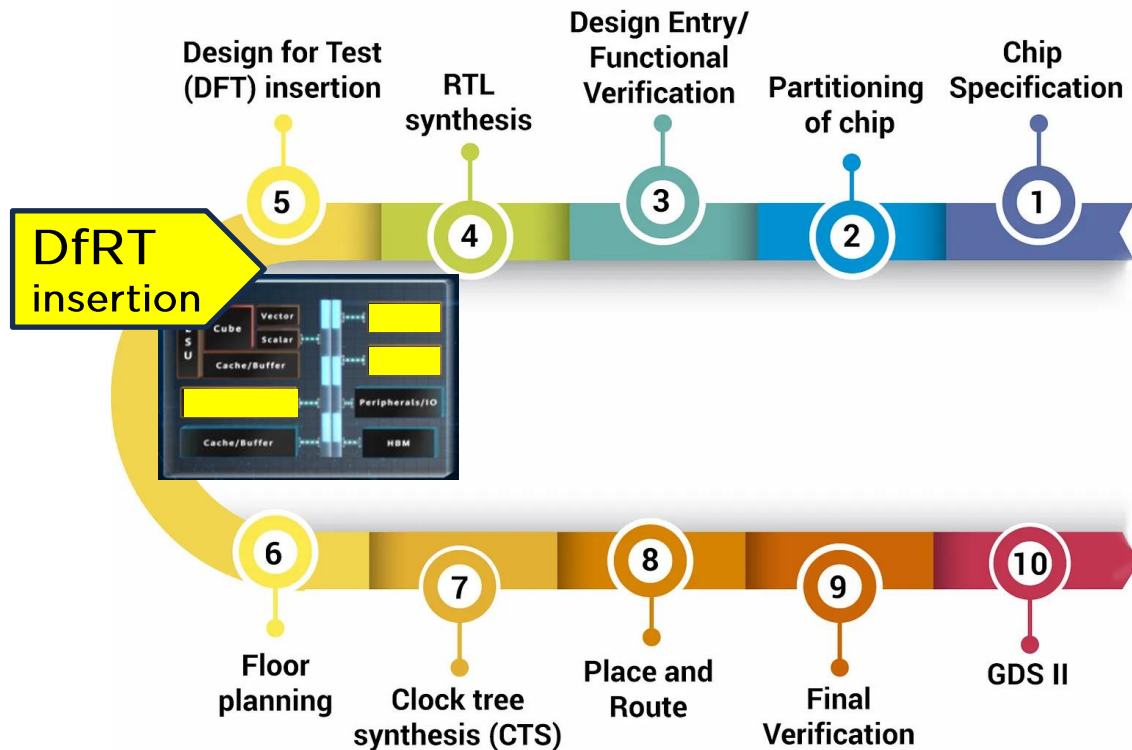
# WHY ELES RETE can improve ICs Reliability ?

Key elements to move from PASS/FAIL to effective Learn from Fail:

- Design for Reliability Test (DfRT) at IC Design stage for enhanced fault triggering and detection
- Testing for Reliability (TfR) on a Massive Parallel Tester
  - Test and stress in the same flow
  - Extend Reliability characterization beyond Standard Mission profiles
- Automated Data Analysis Tools – supported by AI technologies - enabling a smart Failure Analysis Flow

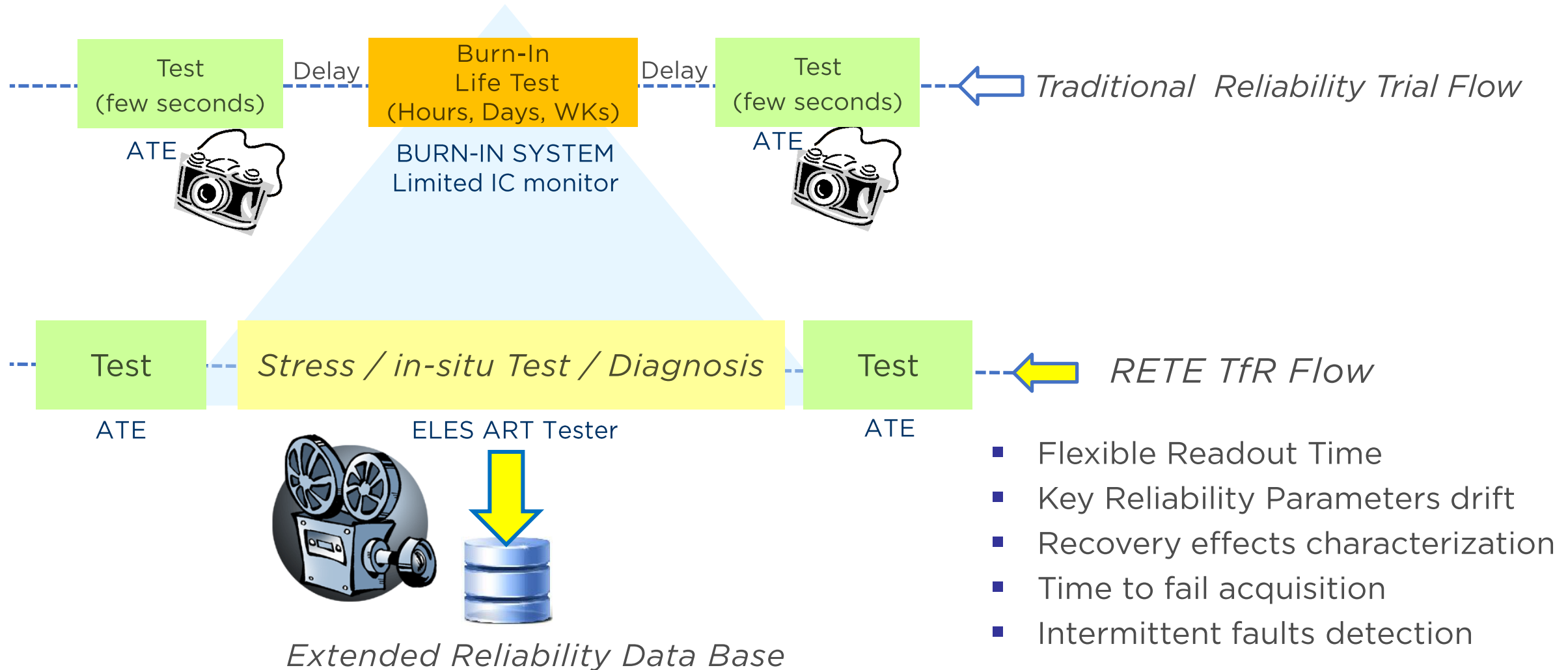


# RETE Methodology - DfRT insertion step



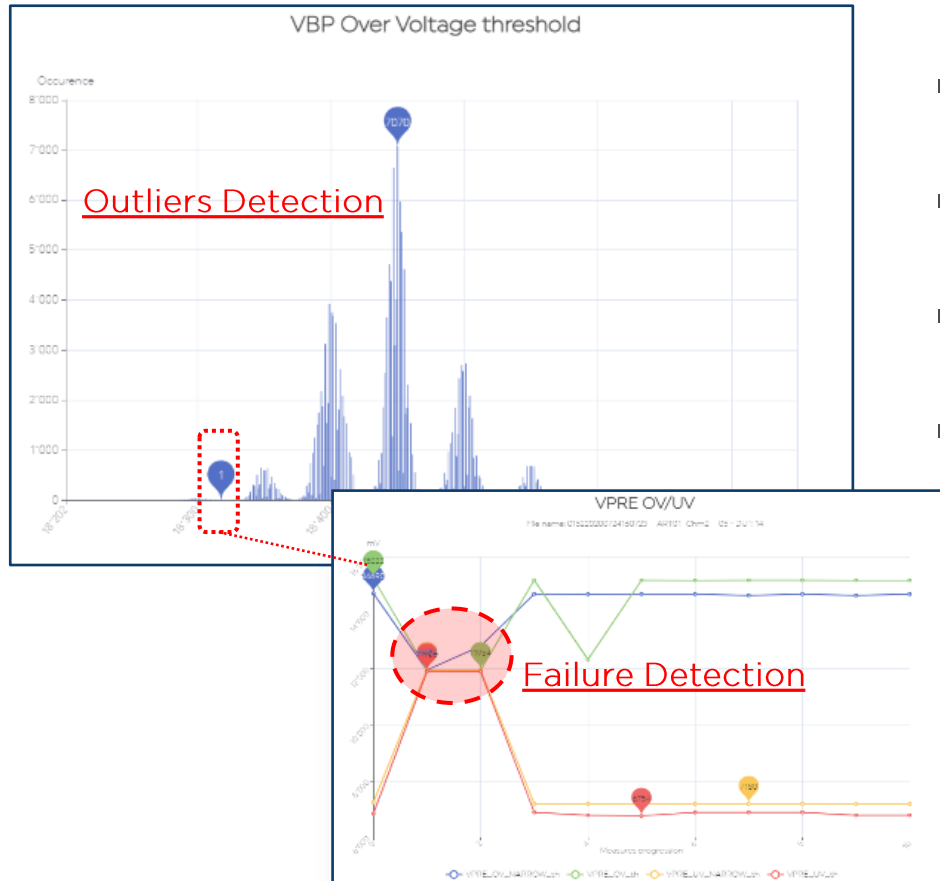
- DfRT Methodology Guide available for IC Design Teams
- Planning of test features “outside” the IC, on the Fixture or Tester side
- Maximize Stress/Test coverage during Q&R trials on a Massive Parallel Platform

# RETE Methodology - Test for Reliability flow

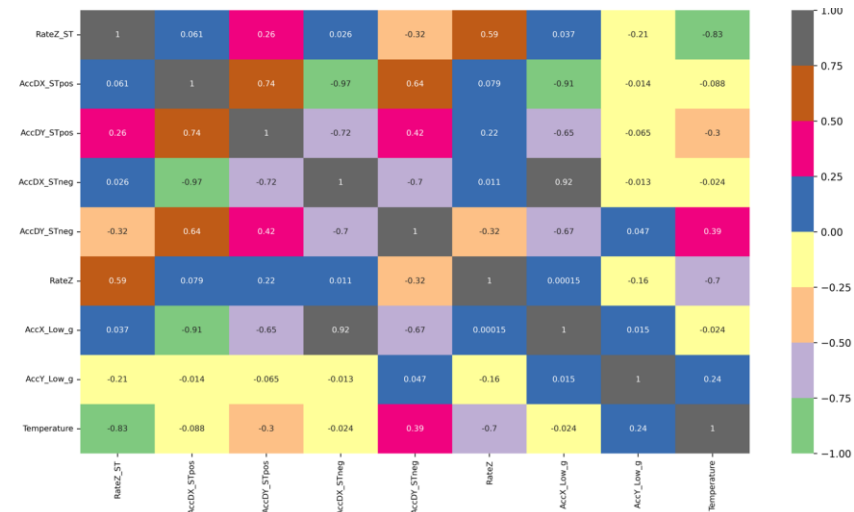




# Statistical Data Analysis - TfR Data Explorer Tool

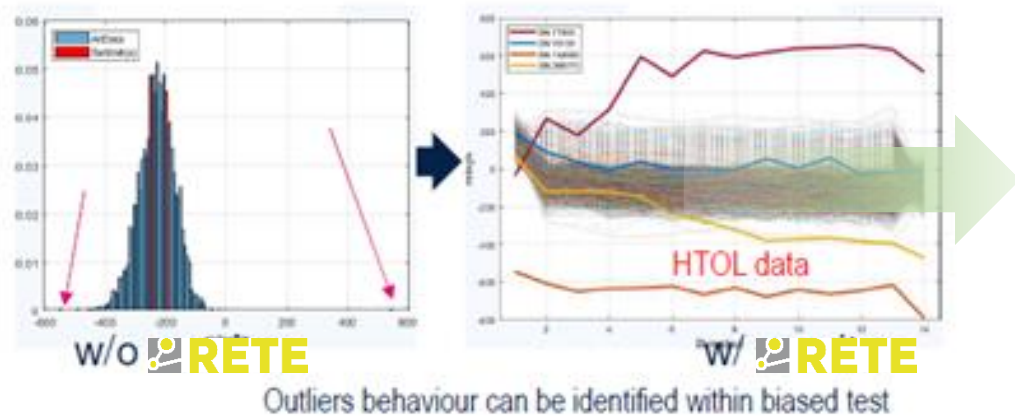
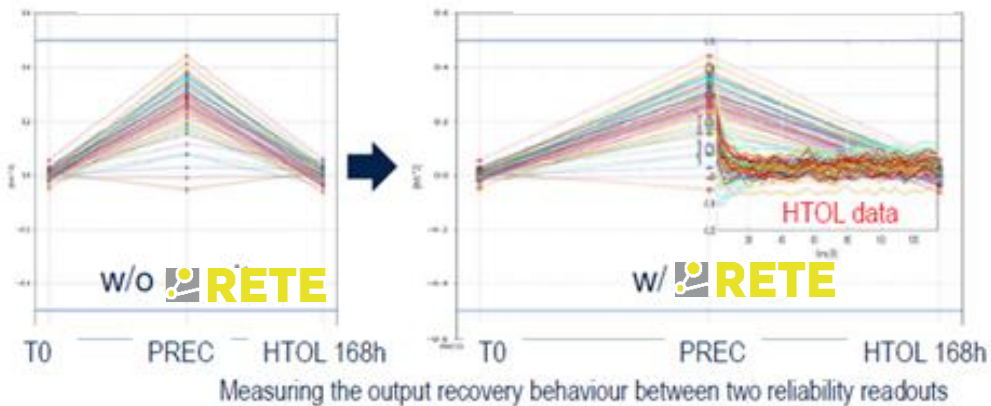


- Identify Outliers and Characterize IC Failures over time
- Drift analysis on the main Key Reliability indicators
- Heatmaps to quickly identify anomalies and IC weakness
- Failure ID-Card to connect Failure Analysis Tools



# Automotive MEMS - Test Case

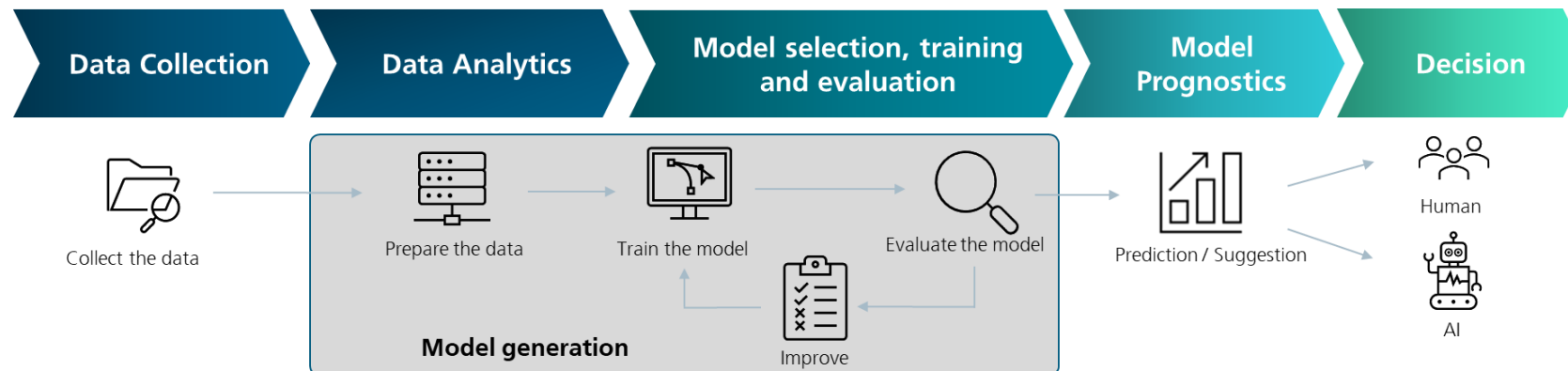
Use Case: Reliability drift behavior enhancement



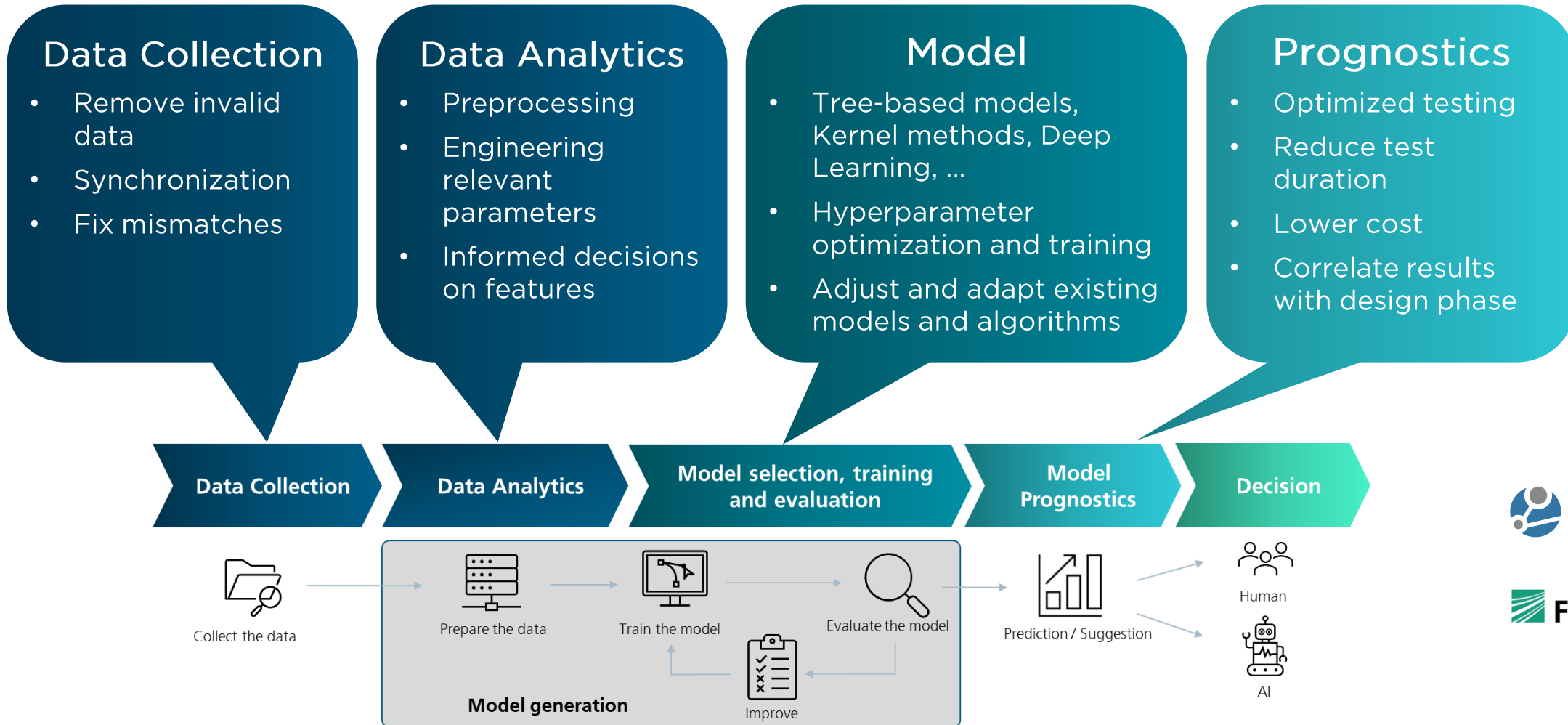
- Move from pre-post stress parametric assessment only on ATE to continuous measurement during HTOL
- Characterization of recovery pattern after preconditioning.
- Early detection of outliers during the test
- Saving Wks of FA activities
- Roadmap: Reliability Prediction supported by AI:
  - Enhanced ability to find critical paths
  - Reliability vs Extended Mission Profiles

# RETE project - partnership with Fraunhofer ENAS

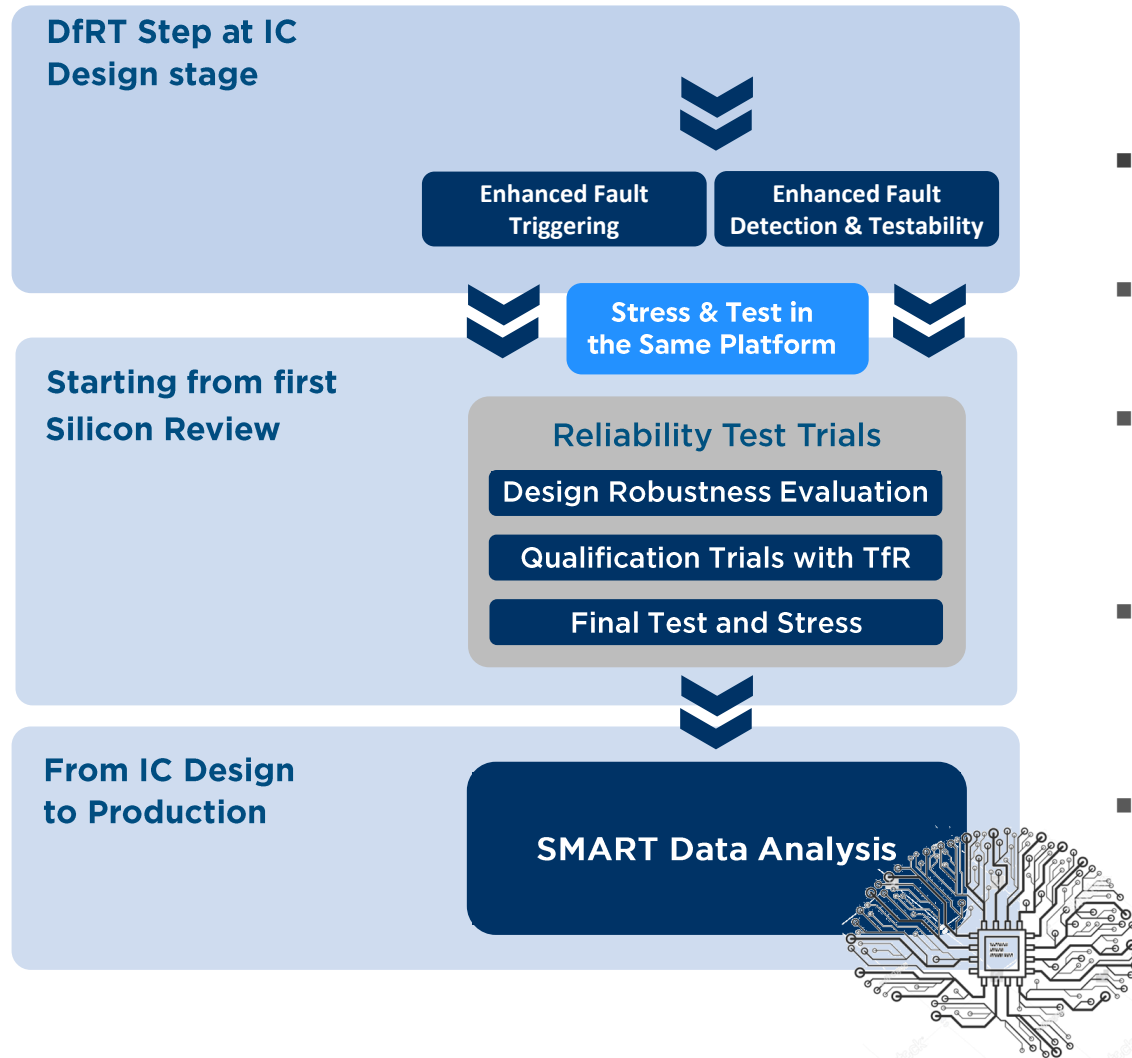
- Innovative Test Methods empowering TfR
- Test Reliability Center setup for qualification trials on different IC families: i.e. Low and High Power SOC, MEMS, Smart Power
- Development of improved IC reliability assessment tools and methods with AI / Machine Learning techniques



# RETE project - partnership with Fraunhofer ENAS



# Key Takeaways



- DfRT Step for augmented stress and test Coverage
- TfR flow for extended reliability data collection
- Emphasis on Reliability and Robustness Evaluation @ pre-qualification stage saving IC redesign steps
- Structured Feedback to Design and Production for reliability improvement towards Zero Defects
- Reduced NPI time and cost

*AI based Data Analytics Tool with the support of Fraunhofer Enas*



*Thanks for your attention*

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