Enabling EU Leadership in automotive ECU for future Autonomous Driving – Reliability Challenges

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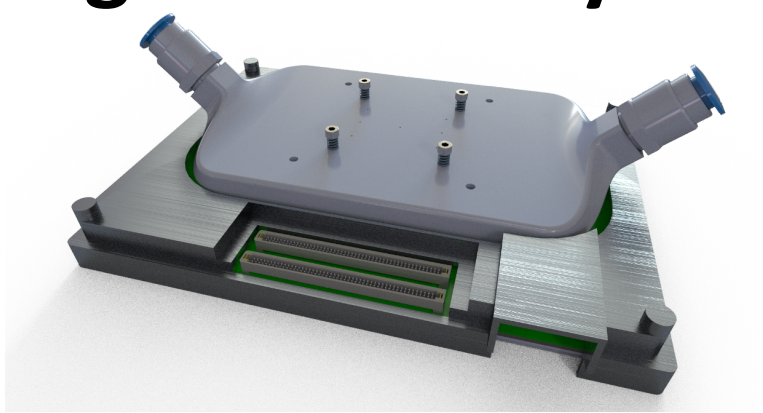
ME-PE/ENG



e²LEAD

BOSCH ILFA TECHNISCHE UNIVERSITÄT BERLIN NANOTEST CARIAD CADFEM nexperia TUDelft IWO TECHNISCHE UNIVERSITÄT CHEMNITZ JIACO INSTRUMENTS Fraunhofer ENAS Xecs GEFÖRDERT VOM Bundesministerium für Bildung und Forschung Rijksdienst voor Ondernemend Nederland boschman advanced packaging technology BOSCH

e²LEAD – reliability challenges

Agenda

- Introduction
- What is e²LEAD about
- Chiplets for automotive – has the time come?
- Cooling path
- How to tackle Dfx challenges
- Compact digital twin
- Virtual Release Through Referencing
- Summary

e²LEAD – reliability challenges

Challenges

- 6 high performance ECUs in a premium car and more than 90 other ECUs
- HCP1 … HCP5
- ECUs are used for:
  - Autonomous driving in future level 5
  - Infotainment, body control, communication and energy management, …
- Chiplets can make a great difference, but are they ready for automotive application?

e²LEAD – reliability challenges
Requirements and Specifications

Creation of specifications based on the VW80000

- Component description
- Requirement due to vehicle use (mission profile)
- Requirements and test
- Electrical
- Mechanical
- Climatic
- Chemical
- Lifetime


VOLKSWAGEN

CONFIDENTIAL
VERTRAULICH

Lastenheft Erprobung

Biggest challenge for future control units

- Operating time so far 8000 h -> now up to always on 131400 h
- Increasing mileage
- High computing power of the semiconductors -> water cooling
- Reliability and Safety for level 5 standards

e²LEAD – reliability challenges

ENABLING EU LEADERSHIP IN AUTOMOTIVE ECU FOR FUTURE AUTONOMOUS DRIVING

e²LEAD – enabling smooth and efficient realization of the supercomputers for highly automated & autonomous cars

- Connectivity
  - Optical, electrical and thermal interfaces
    - Reliability of optical interfaces
    - Enhanced heat-sink with insets and two-phase components
- Technology
  - Automotive chiplets, packaging and integration
    - Chiplet incl. smart stress monitoring
    - Smart power stage for supercomputers for automotive application
- Reliability
  - Accelerate development time of complex ECUs
    - Compact digital twin for high performance GPU, CPU including housing
    - Virtual release through referencing

2 countries

13 Partners
Bosch – Consortium lead

03.2023-02.2026

9240 k€

e²LEAD Innovations

↓ Level	Connectivity	Technology	Reliability & Safety
	High-Performance **Data** and **Thermal** Interfacing	Automotive **Chiplet** & **SPS** Packaging & Integration	New **Tests** and Validated **Compact** Digital Twins
Component	Innovative Interface Elements * **Inhernently secure** & ultra-fast optical data interface * Compliant TIM-1 (PCM & silicone) ⇒ **min R_{th} to chiplets** I * Precision BLT chiplet cap	Supercomputing Components * **Chiplets - Org.Interposer** * Thermal test vehicles (TTV) * **SPS /w sensors & monitors** * Slim Pack. f.multi-dies, high R power-density & I/O counts	Automated Digital Twining * **Modular set of digit. twins** → th-mech.check f.all designs * Lower **Level of Redundancy** * **Thermo-fluidic digital twin** A/I f.'chiplet to system'cooling
Module / Board	High-performance Interfaces * **Reliable optical data link** * Comprehensive thermal co-design: Chips-BGA-PCB-ECU * ***'CoolStar'*: Low-stress Thermal Interconnect**	Supercomputing Modules * **Undermolding** for most robust chiplet-BGA modules * **Multi-die dual-side sintering** for max. power density R * Chiplet-TTV & SPS testing	Design for Trustable Board * New **Reliab. Test Strategy** * **Non-cloneable** HW Feature * **Compact** digital twin (**CDT**) * **CDT use for ECU design** R * CDT-FMU for 2000 I/O BGA
System (HW+SW)	3D co-optimized Connectivity * Heat pipes in the cold plate * 3D printed pin-fin cooler * 2nd heat path through PCB * **Digital Master & 3D Master** I f. ECU housing & interfaces	Optimum System Integration * SW implementation in the system-HW + **functional tests** * Verification of the **chiplet-based supercomputing system** I by automotive stress tests	CDT for Dyn. Perf. Adjmnt. * **CDT integr. in the system:** field data+expectation values * **RUL extension** through dyn. performance adjustment ⇒ R mission fulfillment all time

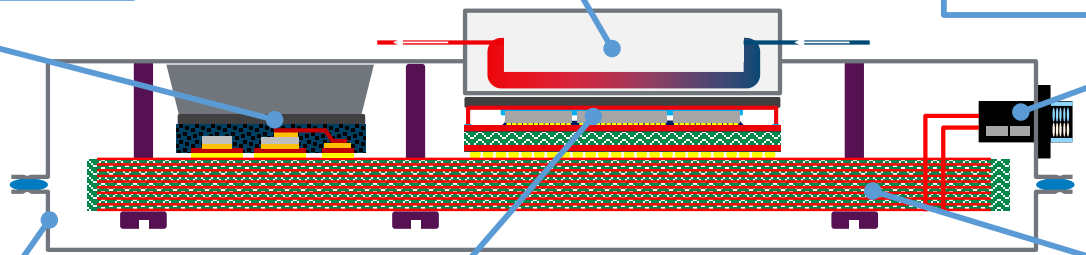
Innovation Level: R Research & Innovation I Innovation A SoA Adoption **Highlight**

e²LEAD – reliability challenges
Demonstrator

II Smart Power stage
From data center to harsh environment

I Thermal interfacing
Innovative low stress cooling solution

I Connectivity beyond state of the art
Plastic optical fiber for autonomous driving



Novel data-driven business models
Compact digital twin

III

Advanced packaging enabling autonomous driving
Chiplets technology with undermolding

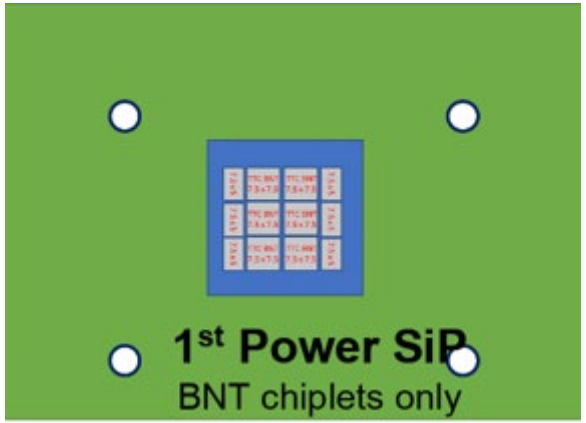
II

III Reduction of the time to market
Virtual release through referencing

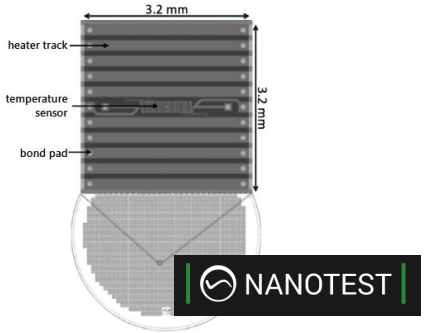
e²LEAD – reliability challenges

Chiplets for automotive – the time has come

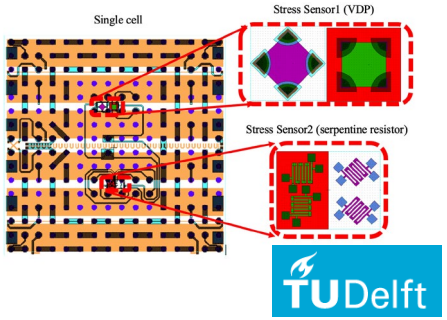
- **Chiplets** is part of a packaging architecture.
- An integrated circuit block designed to communicate with other chiplets to form more complex ICs.
- For large and complex chip designs → the design is subdivided into functional circuit blocks (often reusable IP blocks)
- These blocs are called "chiplets"



BNT Thermal Test Chip



TUD Thermal Test Chip



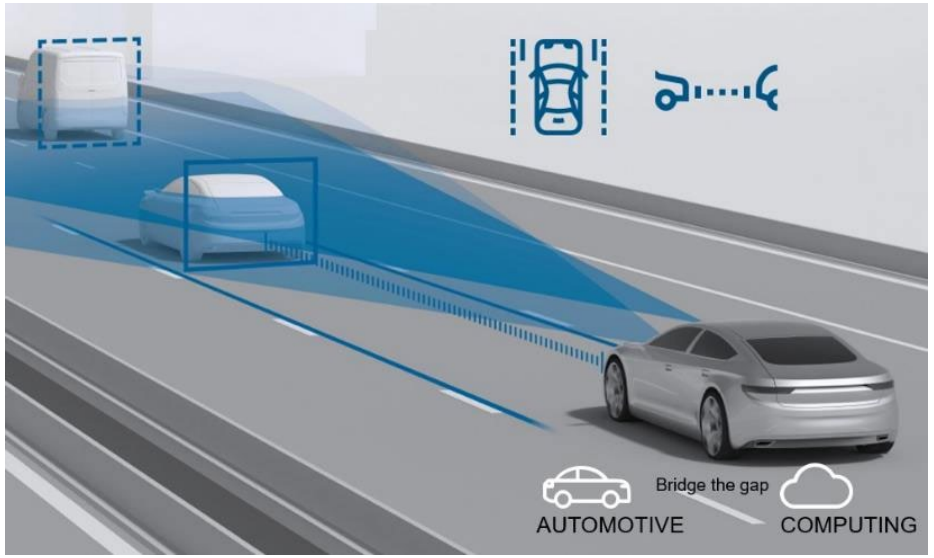
e²LEAD focuses on reliability assessment of future chiplets for harsh environment

e²LEAD – reliability challenges

Smart Power Stage for Automotive Computing

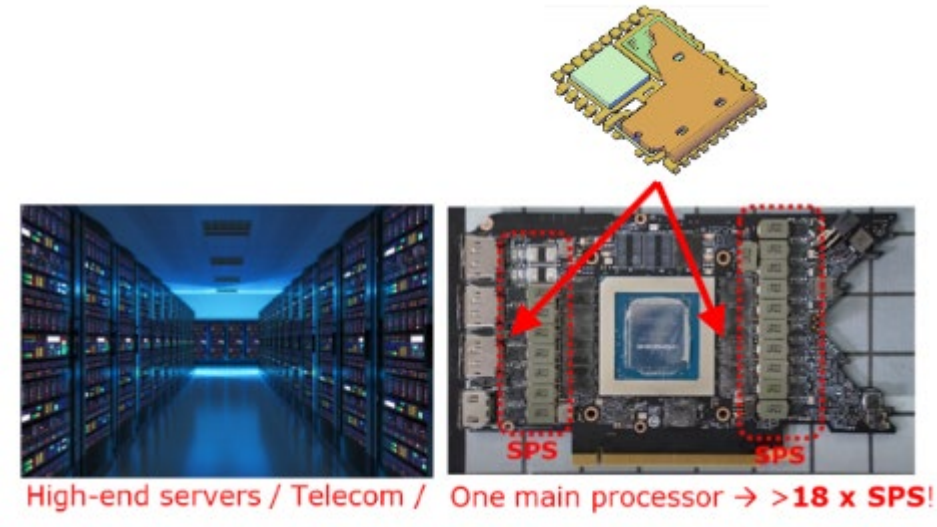
Motivation & Use-Case

- Self driving cars require significant computing power.
- Advanced CPU/GPUs 18 x SPS (Smart power stages).
- Nexperia solutions for future automotive applications.



Objective

- Nexperia smart power stages for Next Gen. automotive computing platform ECU –> From Server to Auto
- New heat management solutions, DACA interconnects, new monitoring concepts for Digital Twin input

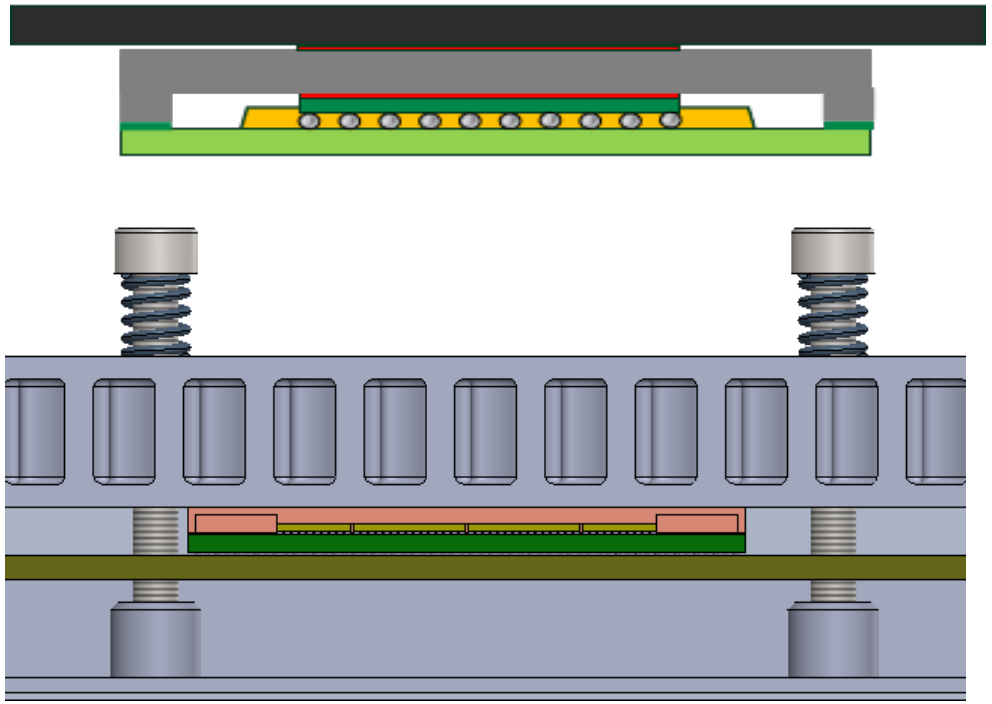


e²LEAD – reliability challenges

Cooling path – two versions

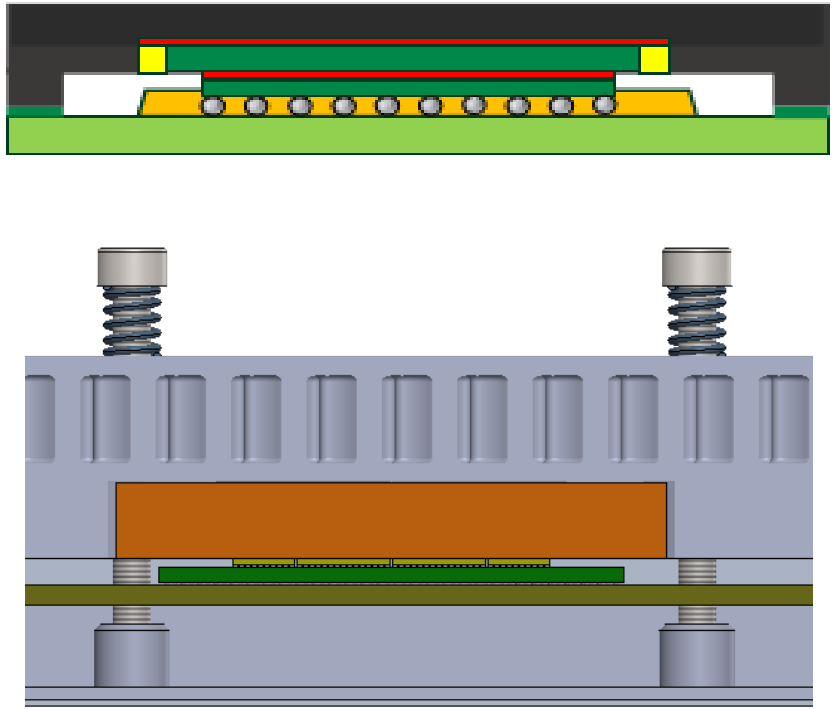
Reference case

PowerSiP with chiplets and lid



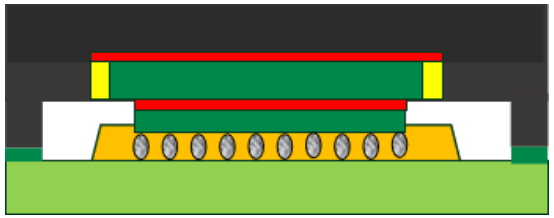
CoolStar

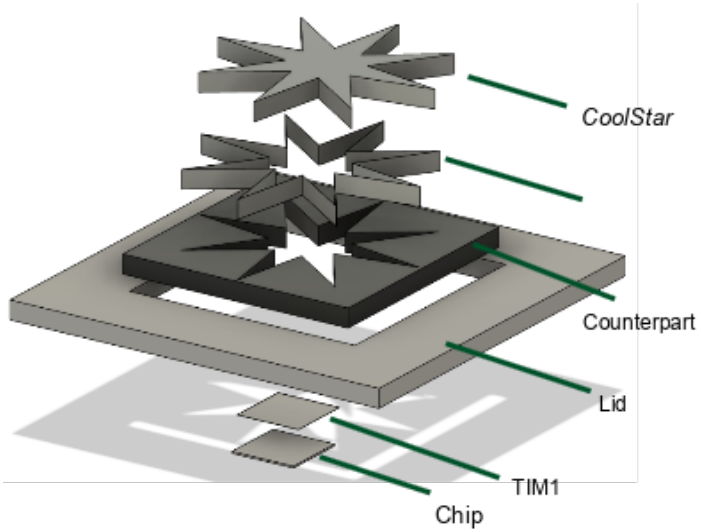
PowerSiP with chiplets and stiffener

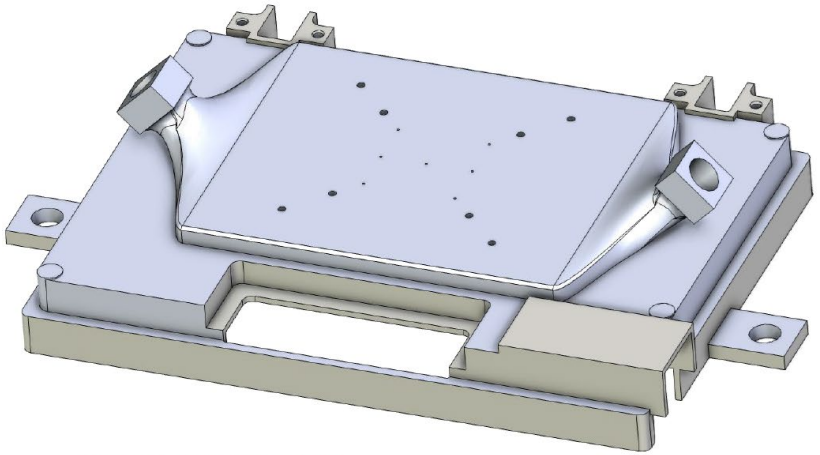


e²LEAD – reliability challenges

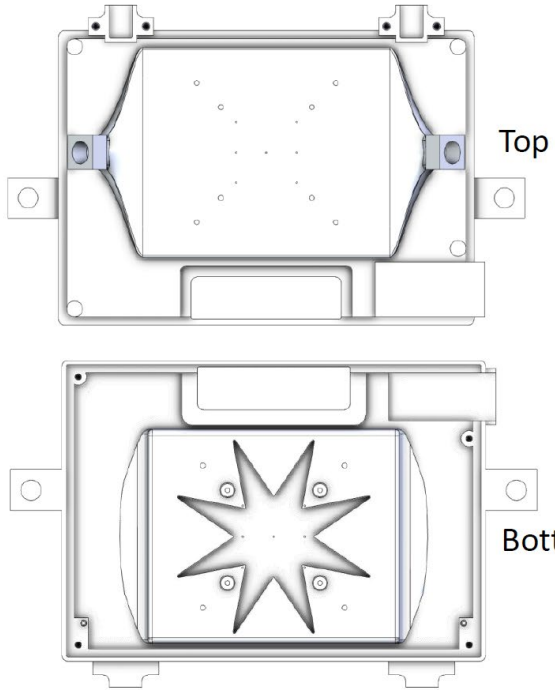
Housing with integrated cooler (e.g. CoolStar)







Fused CaseCooler
V=223.43 cm³

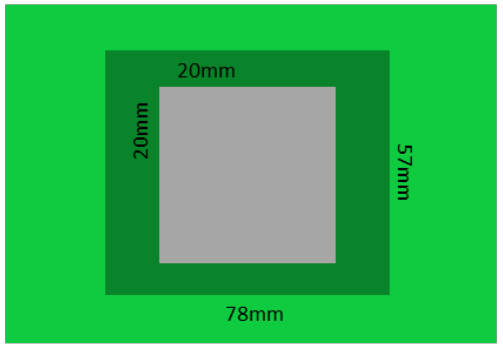


Low stress cooling solution for automotive chiplets

e²LEAD – Reliability challenges

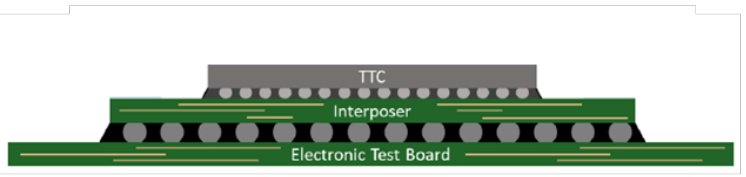
Building FEM models

Single Chip



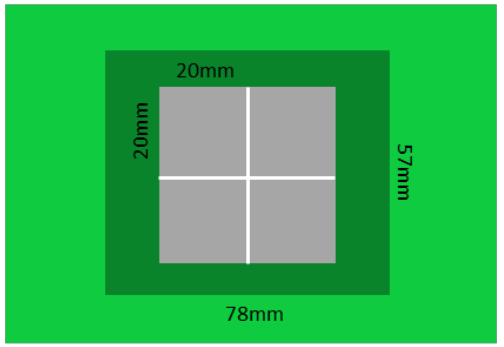
78x57x1.52 mm Interposer, 120x100x2 mm PCB assumed

40x40mm2 chip area



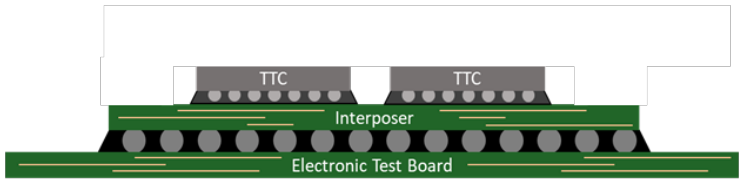
Nanotest TTV3: Single Chip

4 Chiplets



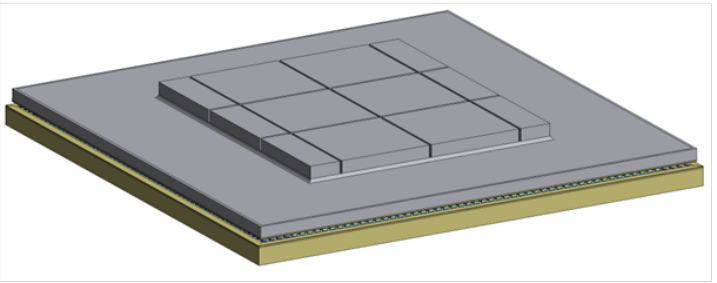
78x57x1.52 mm Interposer, 120x100x2 mm PCB assumed

≈ 40x40mm2 chiplets area



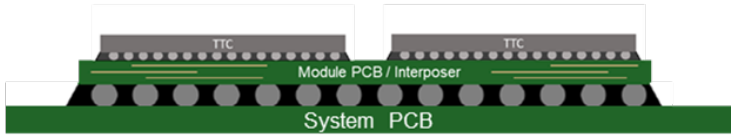
Nanotest TTV1: 4 Chiplets

e²Lead Power SiP module: 12 Chiplets



37x37x1.2 mm Interposer, 80x80x2mm PCB assumed

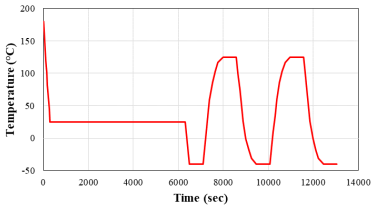
≈ 25x25mm2 chiplets area



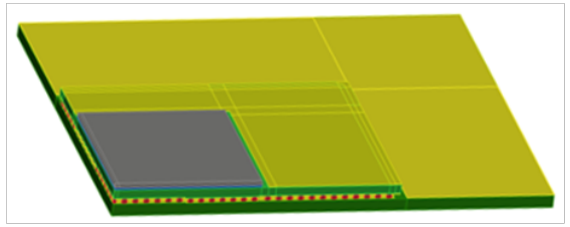
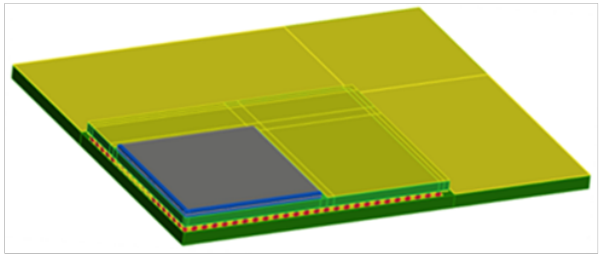
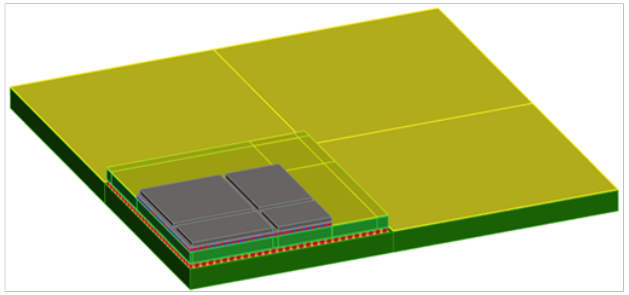
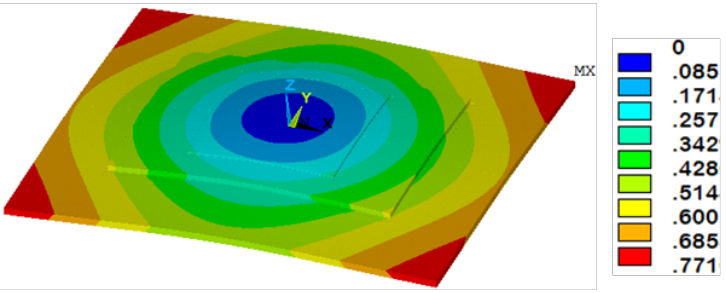
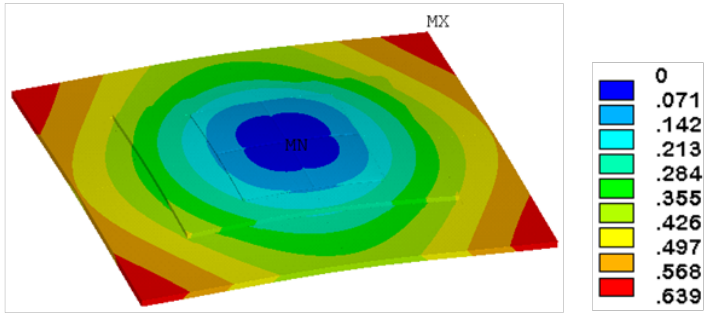
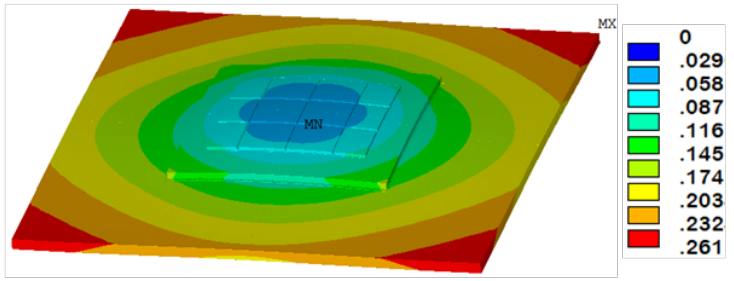
LID, TIM, seal ring not considered

e²LEAD – Reliability challenges

First results

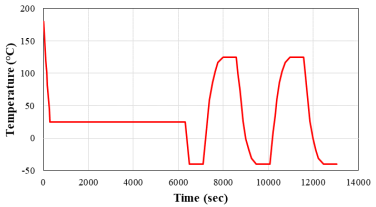


T @-40°C after 2cycles

Single Chip	4 Chiplets	e²Lead SiP module: 12 Chiplets
		
Total deformation (mm)	Total deformation (mm)	Total deformation (mm)
		
771 µm	639 µm	261 µm

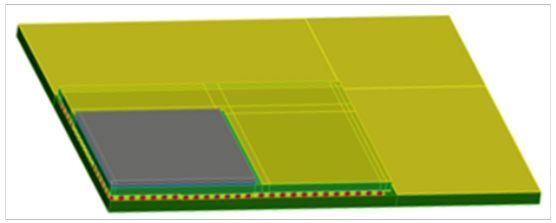
e²LEAD – Reliability challenges

Degradation of solder

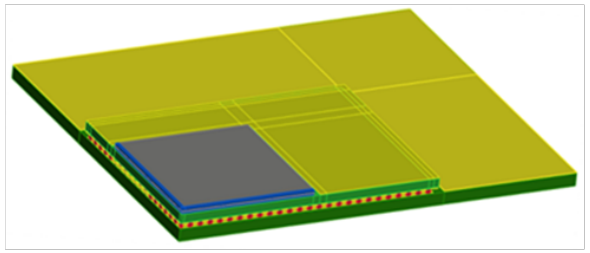


T @-40°C after 2cycles

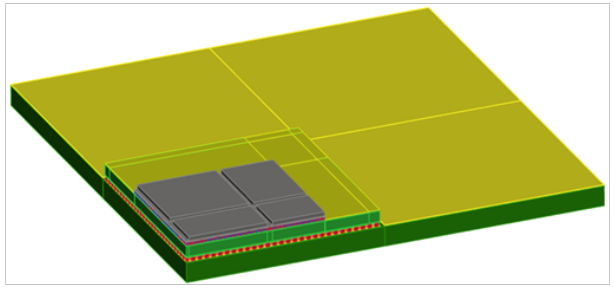
Single Chip



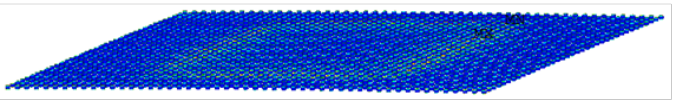
4 Chiplets

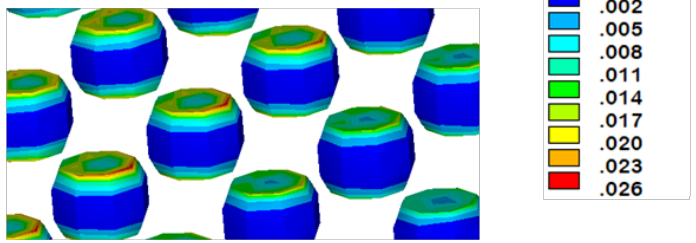


e²Lead SiP module: 12 Chiplets



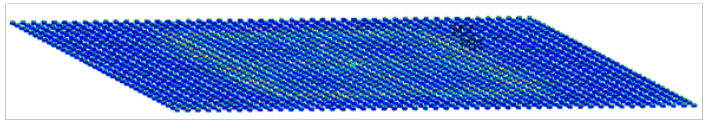
Accumulated Equivalent Plastic Strain in Board level solder balls

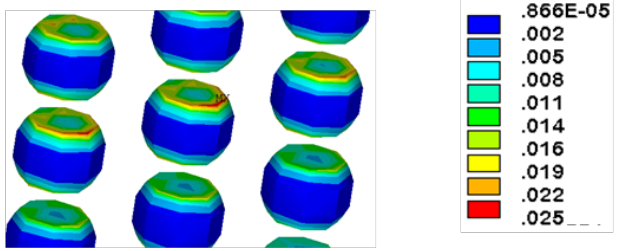




Maximum strain at solder ball at die edges

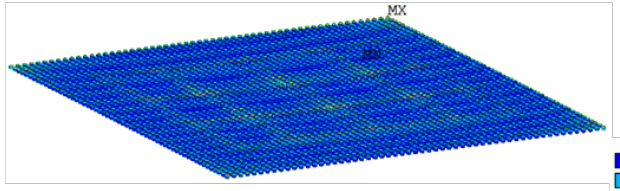
Accumulated Equivalent Plastic Strain in Board level solder balls

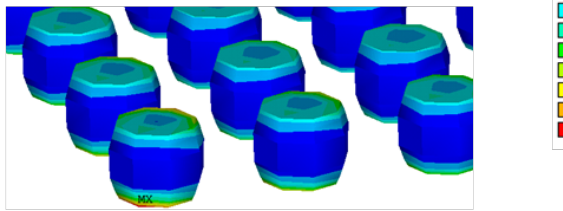




Maximum strain at solder ball at die edges

Accumulated Equivalent Plastic Strain in Board level solder balls



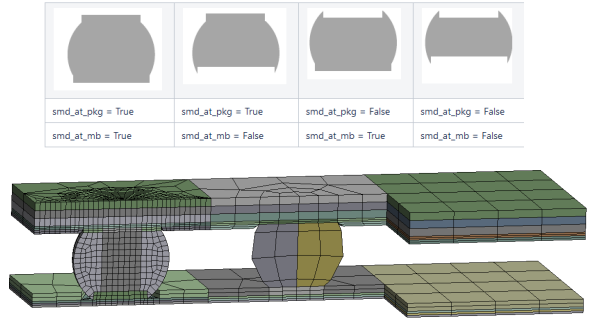


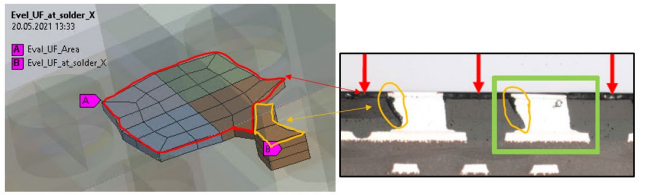
Maximum strain at die and interposer corners solder ball

e²LEAD – Reliability challenges

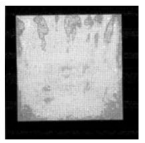
Virtual DoE – selection of underfill

- **V**irtual **D**esign **o**f **E**xperiment is a technique to select most optimum material based through the sensitivity parameters
- **VDoE** – does provide qualitatively correct reliability prediction about product we develop
- Method verified and validated in the HiPer project
  - Mesh sensitivity study
  - Global vs. stripe model
  - Code sensitivity
  - Warpage and in-plane deformation
  - Successfully reduces stress for large GPU die (20x20 mm²)



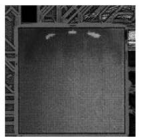


HIPER



Simulation driven design – knowledge-based decision making

- Underfill → stress reduction by 17%
- Solder mask → stress reduction by 5%
- Results – no delamination

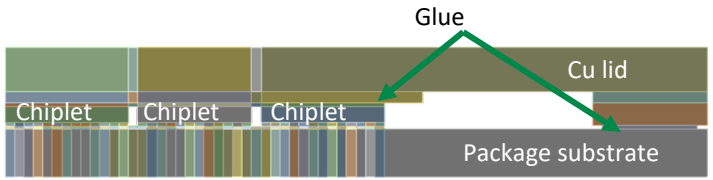


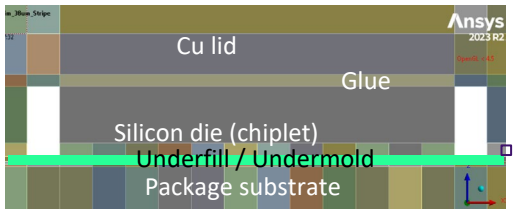
e²LEAD – Reliability challenges

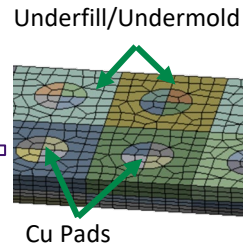
VDoE - selection of underfill for chiplets

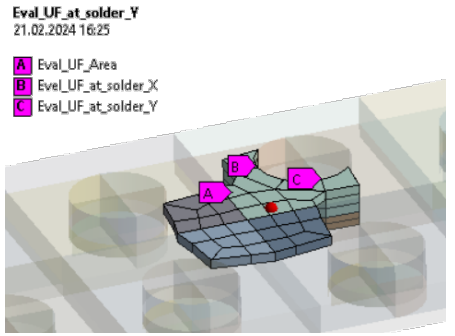
Parameters - undermold	Range
Modulus of elasticity [MPa]	**12000…30000**
Coefficient of thermal expansion below Tg [ppm/K]	**7…12**
Coefficient of thermal expansion above Tg [ppm/K]	**30…45**
Glass transition temperature [°C]	**100…170**

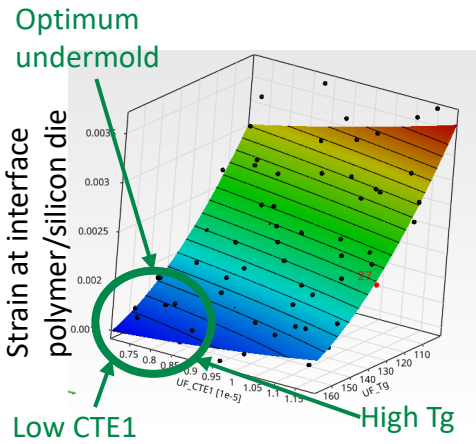
Parameters - underfill	Range
Modulus of elasticity [MPa]	**6500…12000**
Coefficient of thermal expansion below Tg [ppm/K]	**22…42**
Coefficient of thermal expansion above Tg [ppm/K]	**80…125**
Glass transition temperature [°C]	**90…145**

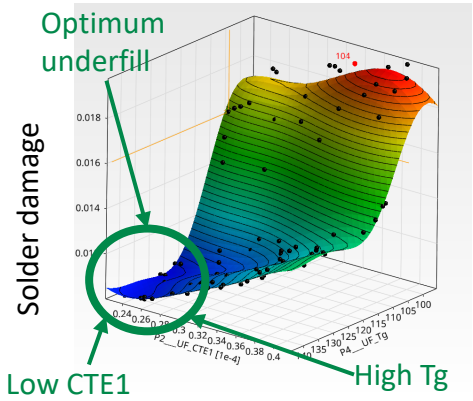






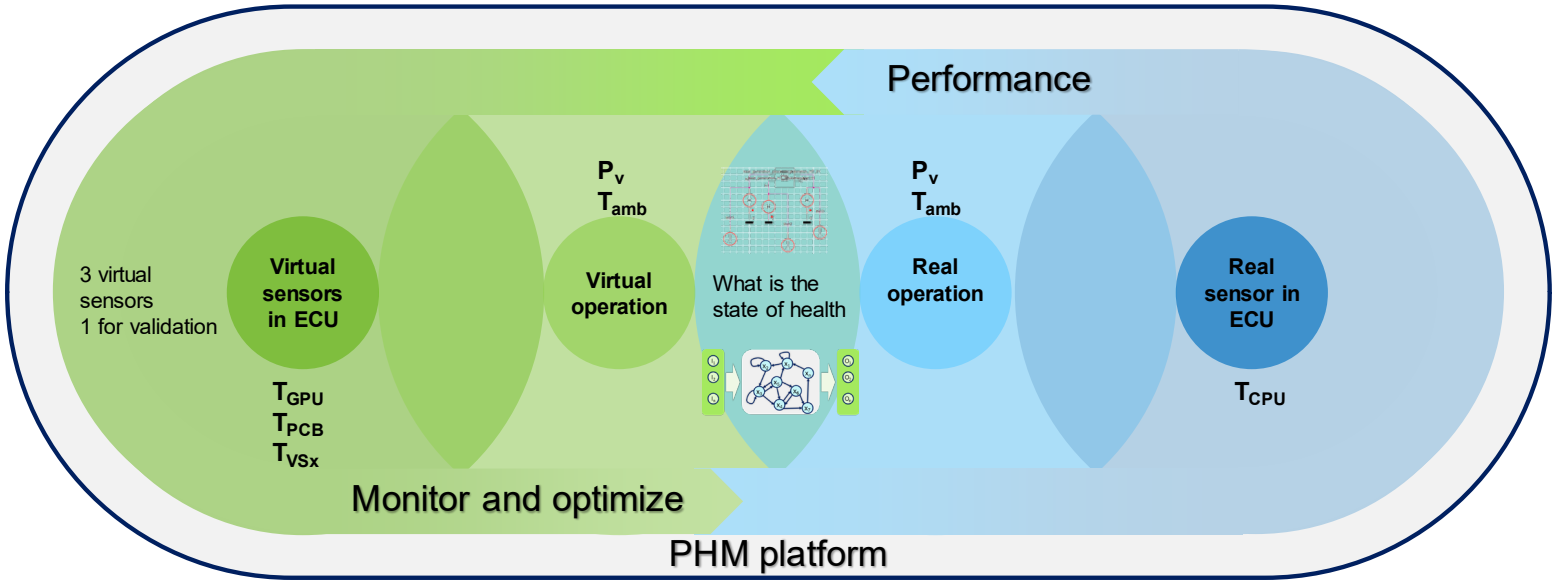






e²LEAD – Reliability challenges

Compact digital twin



IEEE EPS TWGs common definition:

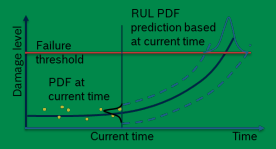
"*Digital Twin is a continuously updated multi-physics, multiscale, probabilistic simulation model of a physical entity (an object, a system, or a process) utilizing big data, bilateral connectivity, and advanced software analytics to provide product monitoring, diagnostics, prognostics, and optimization services*"

e²LEAD – Reliability challenges

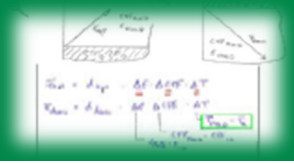
How to make digital twin

How to make a digital twin work?

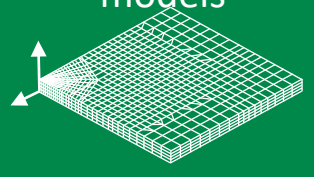
Empirical models



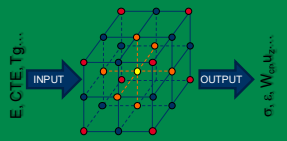
Analytical models



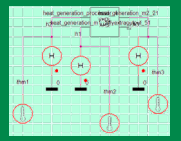
FEM based models



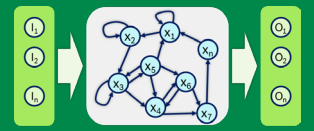
Regression based models



Model order reduction



Data driven models (AI/ML)



Fraunhofer ENAS

CADFEM

BOSCH

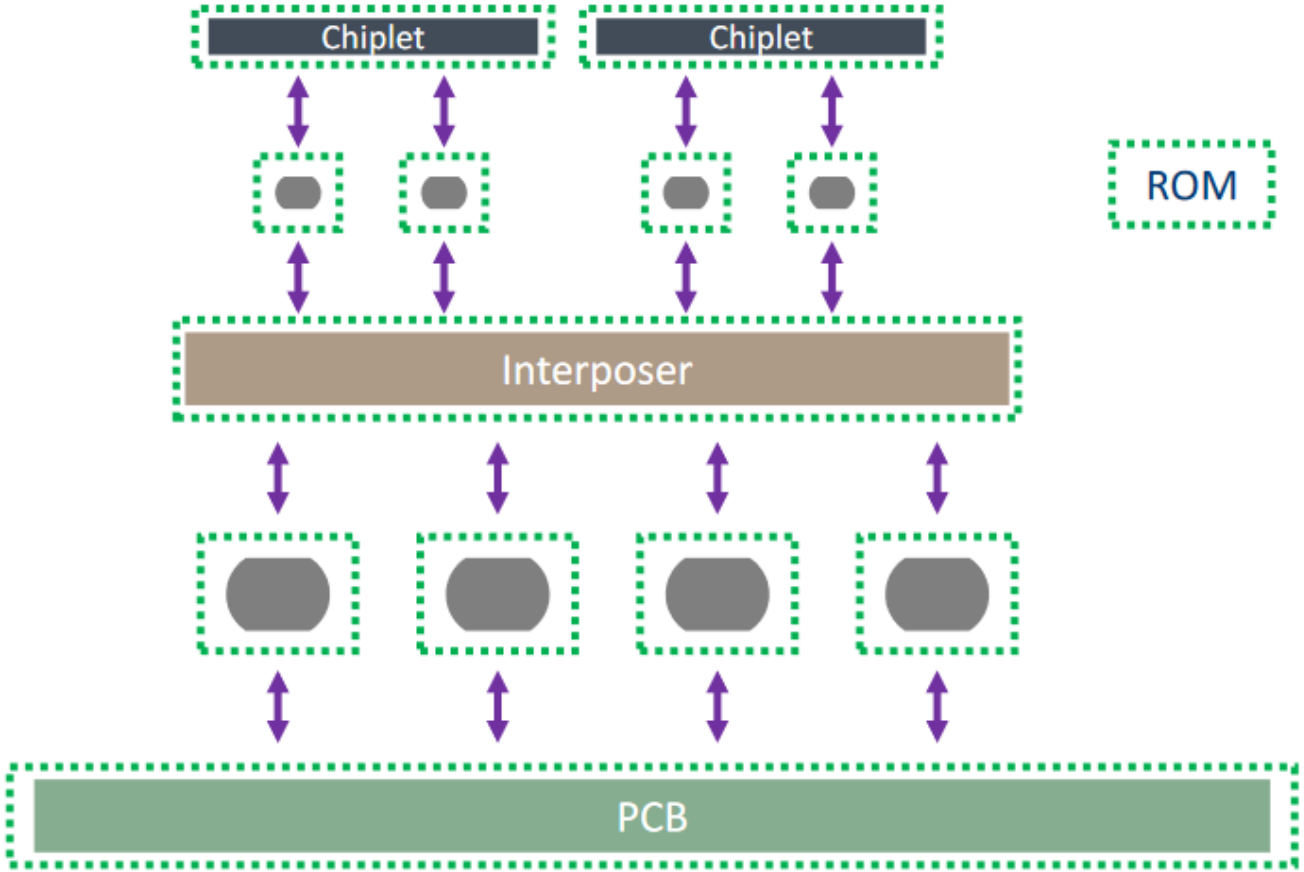
BOSCH

e²LEAD – Reliability challenges

MOR – modular approach for efficient design

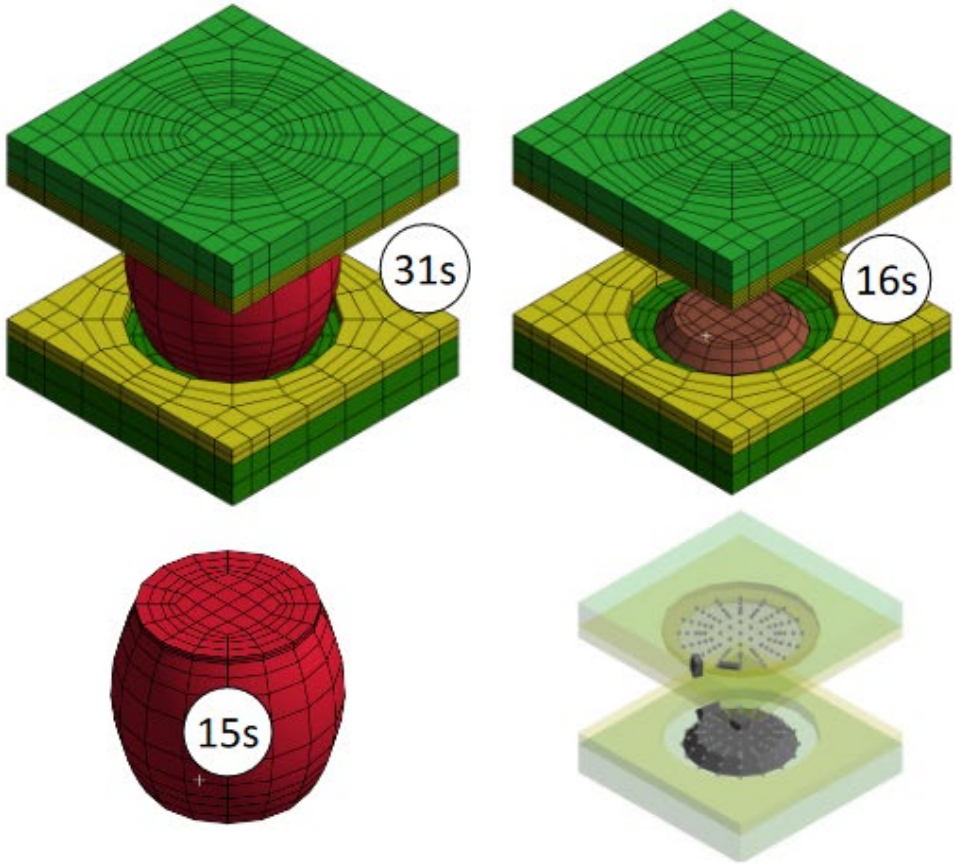
Modular Approach

- Replace components by Reduced Order Models



e²LEAD – Reliability challenges

First implementation



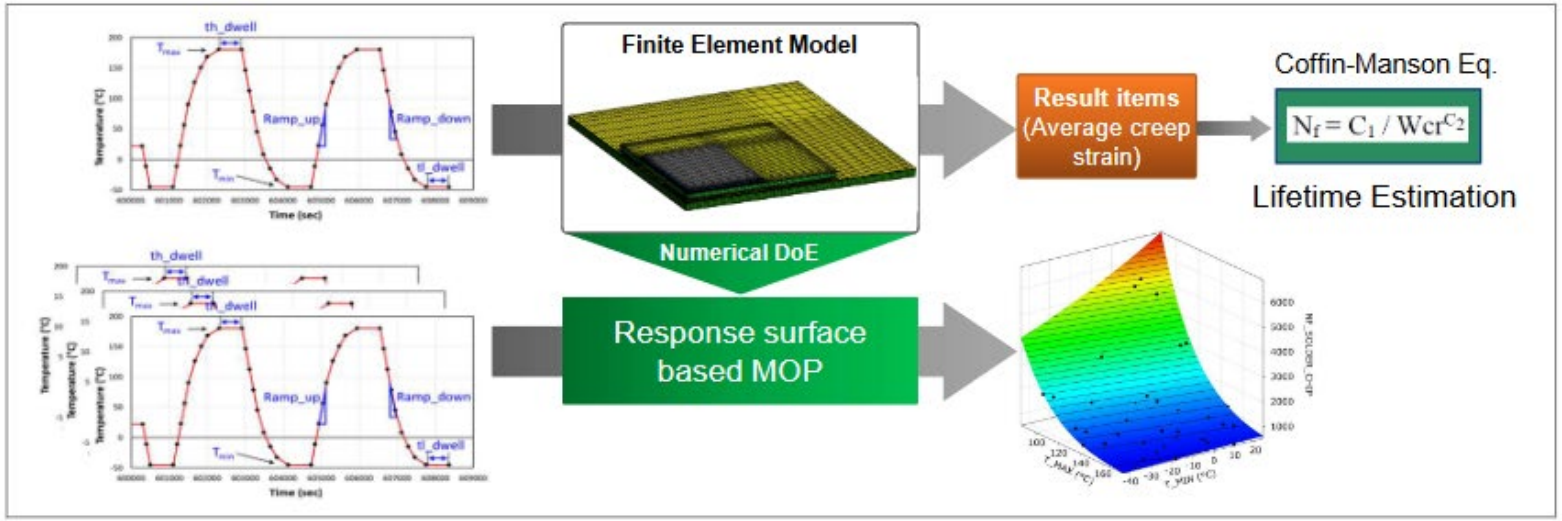
Number of Modes \ Number of Elements	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
7	1s	1s	1s	2s	1s	1s	1s	1s	1s	1s	2s	1s	1s	1s	1s	1s	1s	1s	1s	1s
8	1s	2s	2s	3s	3s	2s	2s	2s	2s	2s	2s	2s	2s	2s	2s	2s	2s	2s	2s	2s
9	2s	3s	2s	3s	4s	3s	4s	3s	4s	4s	4s	4s	4s	4s	5s	5s	5s	5s	5s	5s
10	2s	3s	3s	3s	4s	4s	4s	4s	5s	5s	5s	5s	5s	6s	6s	6s	6s	7s	7s	7s
11	2s	9s	9s	9s	8s	6s	6s	5s	7s	8s	7s	6s	6s	6s	6s	6s	7s	7s	7s	7s
12	2s	2s	2s	3s	5s	4s	6s	8s	9s	9s	8s	9s	8s	9s	10s	11s	10s	10s	9s	10s

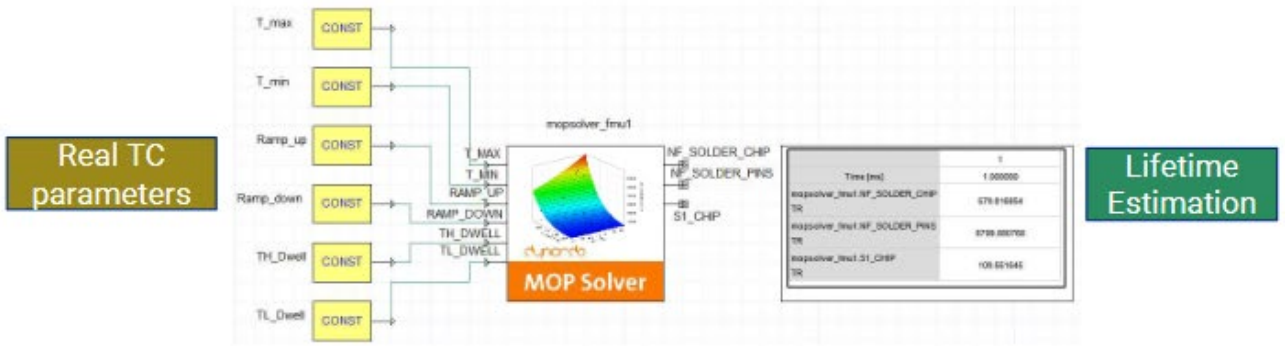
Speed Up

Number of Modes \ Number of Elements	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20
7	15	15	15	8	15	15	15	15	15	15	8	15	15	15	15	15	15	15	15	15
8	15	8	8	5	5	7	8	8	8	8	8	7	7	7	8	7	8	8	8	8
9	7	5	7	5	4	5	4	5	4	4	4	4	4	4	3	3	3	3	3	3
10	8	5	5	5	4	4	4	4	3	3	3	3	3	3	3	3	3	2	2	2
11	8	2	2	2	2	2	3	3	2	2	2	3	3	3	3	2	2	2	2	2
12	8	7	8	5	3	4	3	2	2	2	2	2	2	2	2	1	2	2	2	2

e²LEAD – Reliability challenges

Response surface based digital twin



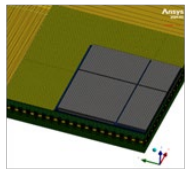


e²LEAD – Reliability challenges

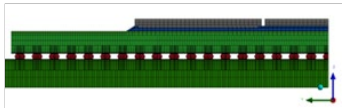
AI/ML based digital twin

Geometry

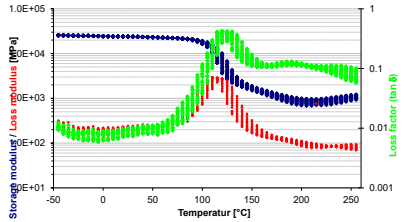
FE- model Chiplet



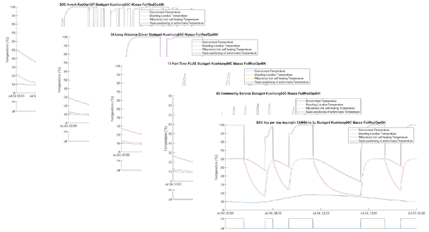
BGA-Quarter FE model



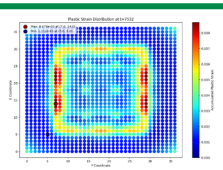
Materials

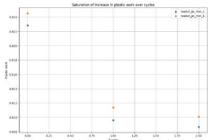


Loading conditions

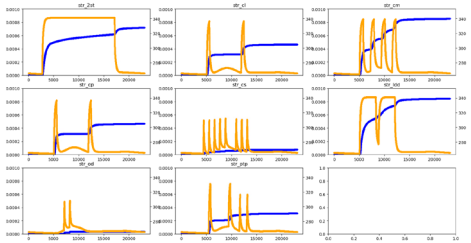


FEM based database

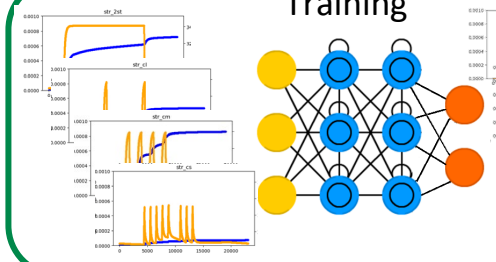




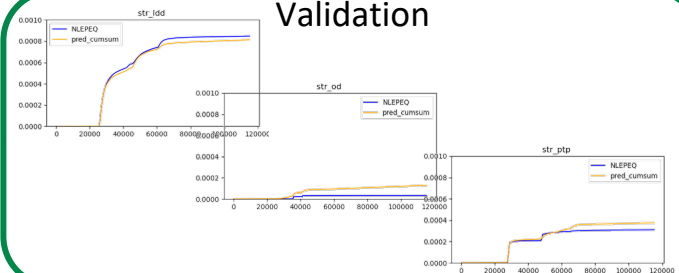
Use case scenarios



Training

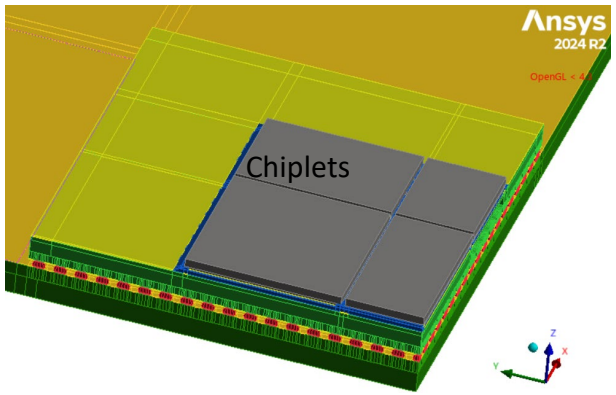


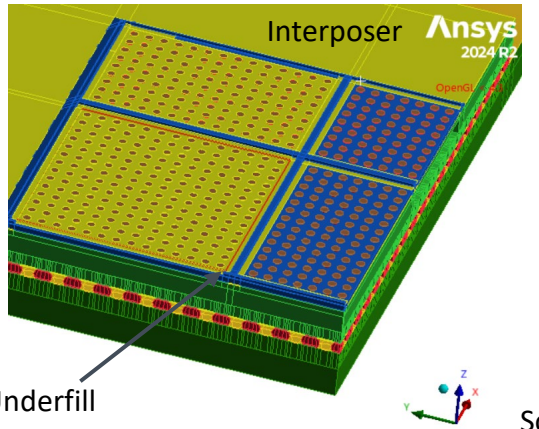
Validation

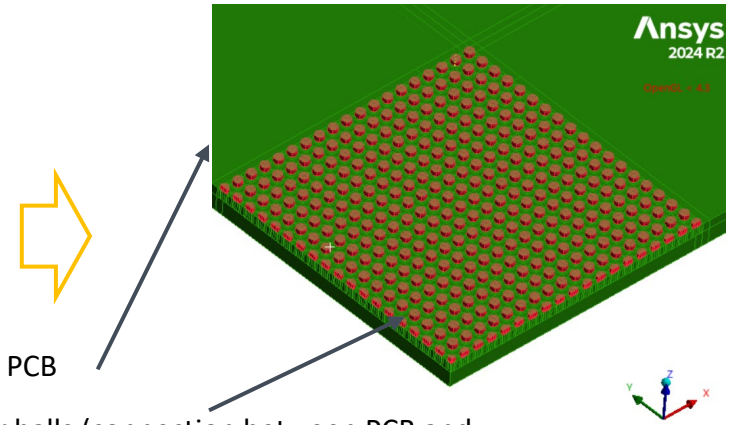


e²LEAD – Reliability challenges

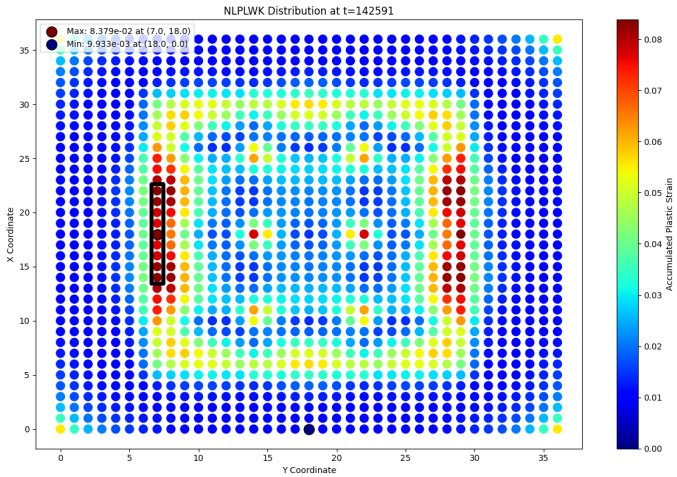
Device under investigation

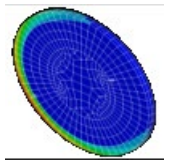




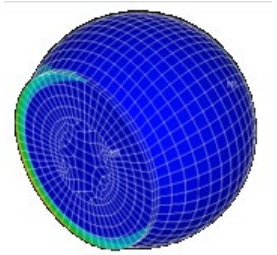


- 9 solder ball under investigation
- 2 evaluation areas under investigations





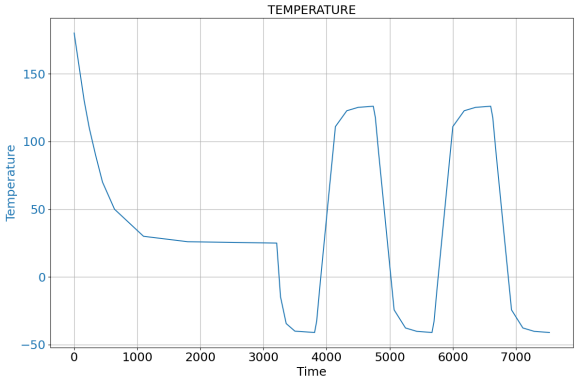
Neck

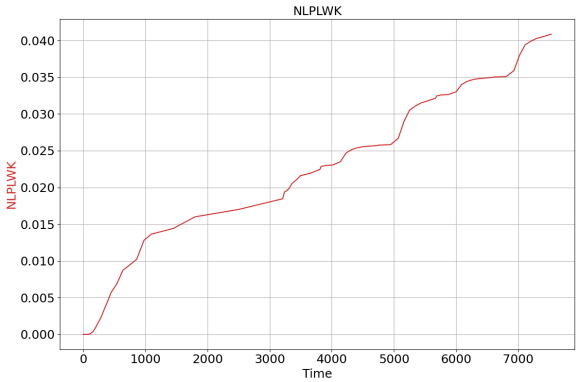


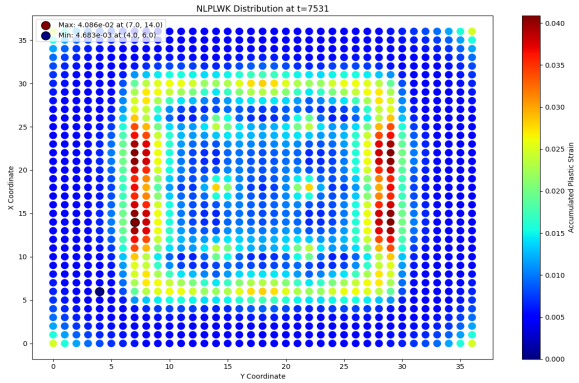
Solder ball

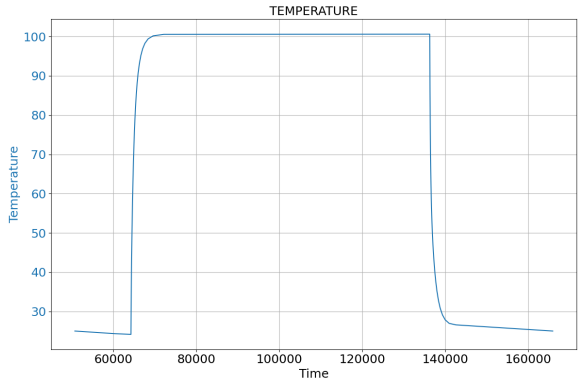
e²LEAD – Reliability challenges

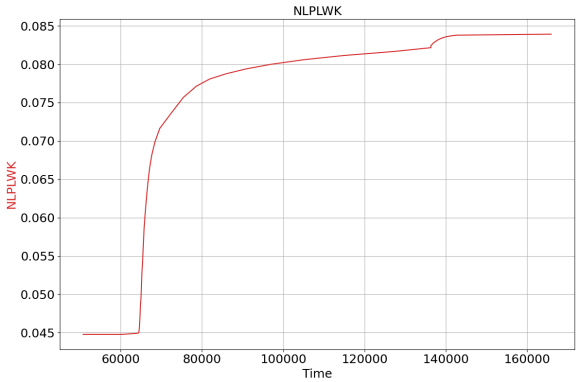
Results

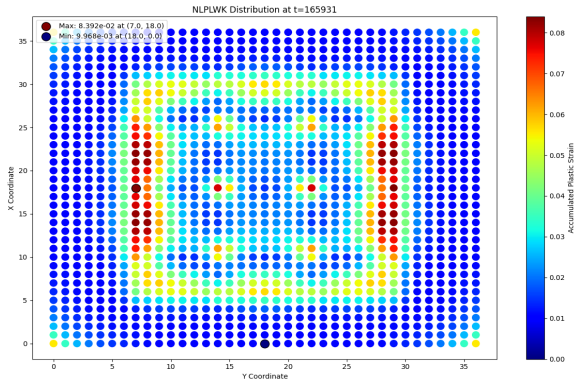






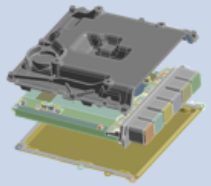
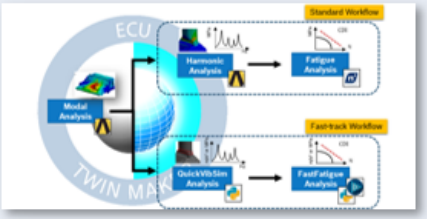






e²LEAD – Reliability challenges

Virtual release through referencing

Test Spec	Device under Test	Test Chamber	Test Results
			
▪ Hybrid approach, simulation data compared to already tested ECU ▪ Focus on endurance testing (thermal cycling, vibration, high temperature) ▪ Intended for variants of extensivly qualified platforms		Digital Testbench  Reference Data Results from available validations and simulations	▪ Method saves time and money

e²LEAD – Reliability challenges
Summary

- Supercomputing systems for highly automated and autonomous system face challenges regarding the packaging technologies for communication and signal processing units, as well as heat removal and power delivery.
- ***e²LEAD*** focuses on collaboration within European stakeholders on an advanced packaging for automotive supercomputing platforms withing three research domains:
  - **Connectivity** for high-performance data and thermal interfacing,
  - **Technology** for automotive chiplets and smart power stage (SPS) packaging and integration,
  - **Reliability** for new test strategies and digital twin-based design methods.

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