TECHNISCHE UNIVERSITÄT
CHEMNITZ

Faculty of Electrical Engineering & Information Technology

Chair of Power Electronics

Specific Reliability Aspects of SiC Power Semiconductors

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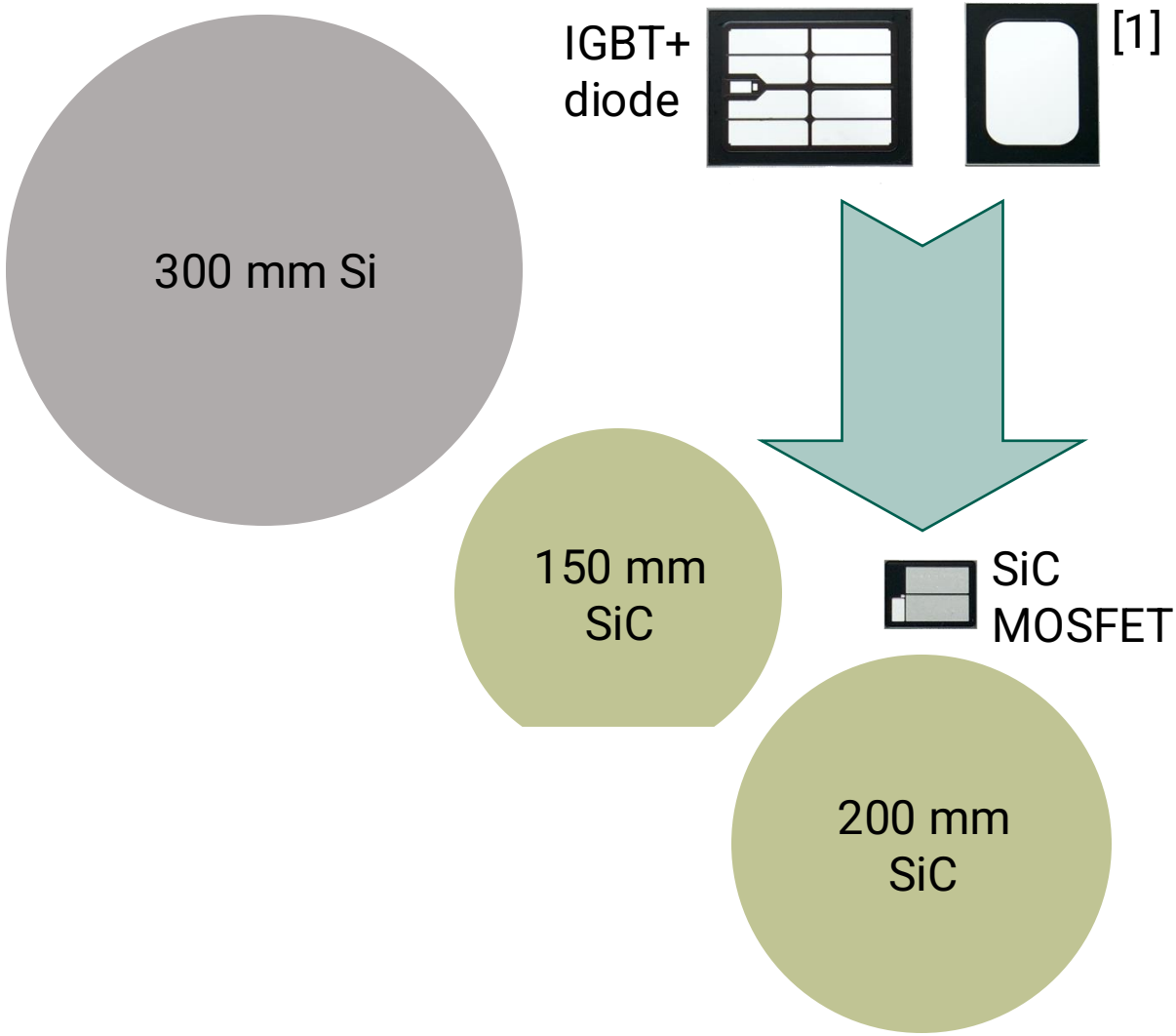
14th Februrary 2025

Cluster Leistungselektronik

Outline

1. Special material properties
   …and the need for new tests
2. Package related aspects
3. Gate oxide
4. Bipolar degradation



Special Material Properties

	Si		4H-SiC
band gap [eV]	1.124		3.23
critical field strength E_{BD} [V/cm]	2 x 10^5		3 x 10^6
MOS channel mobility [cm²/Vs]	500		< 70
thermal conductivity [W/mmK]	0.13		0.37
CTE [ppm/K]	2.6		4.3
Young's modulus (E-Modul) E [GPa]	162		501
crystal quality (base material)	++		+-

(300K)

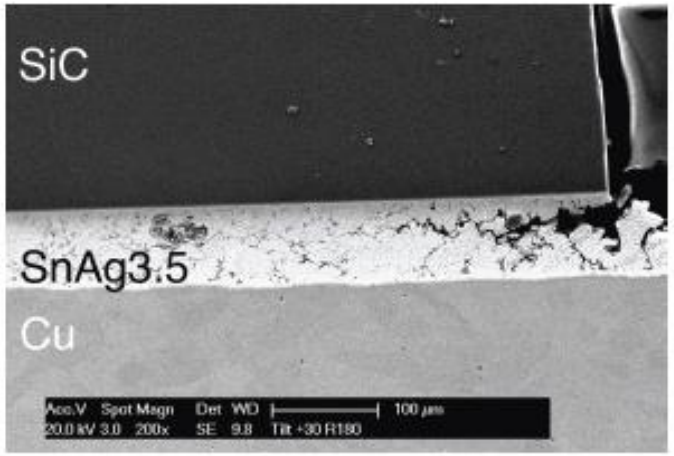
Pros and Cons

- low leakage currents (n_i), high temperatures
- thin/high-doped drift zones → low R_{on} x A
- more challenging oxidiation process (defects)
- high stress for joining layers (solder, bonds…)
- bipolar degradation (R_{on} drift over time)

Package Related Aspects

- higher current and power density
- stiffer material + high thermal conductivity

= chip edges are more stressed during power cycling

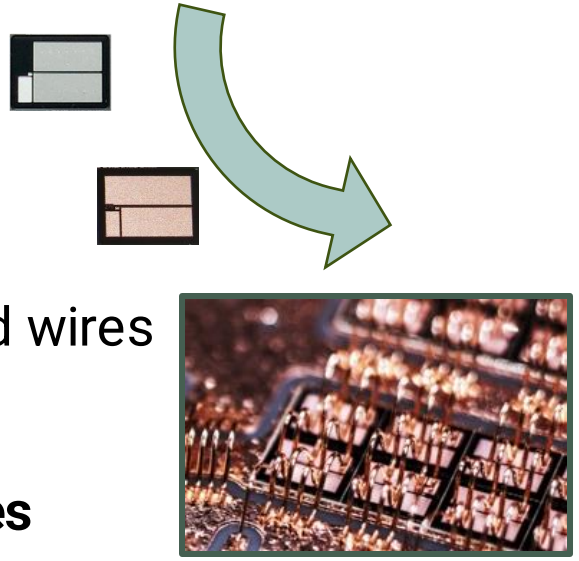


[2]

solder cracks at chip edges

- countermeasures:
  - sintering, diffusion solder
  - copper metallization + bond wires
  - improved bonding

= **similar lifetime of Si devices**



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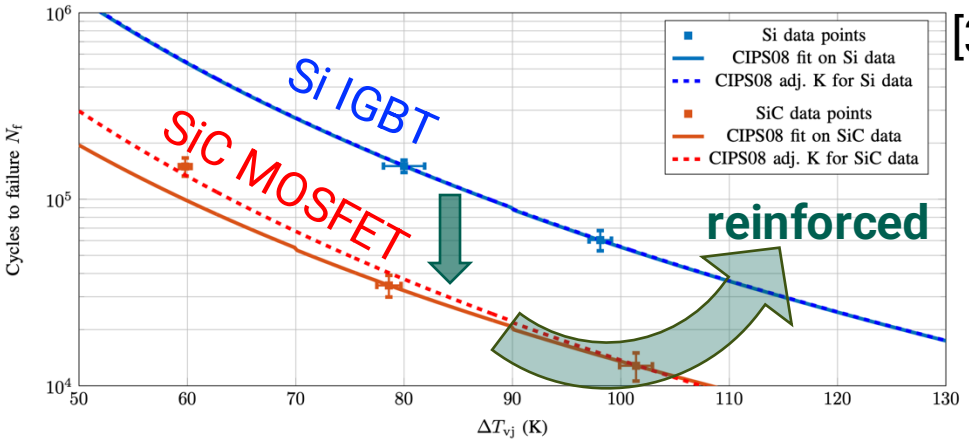
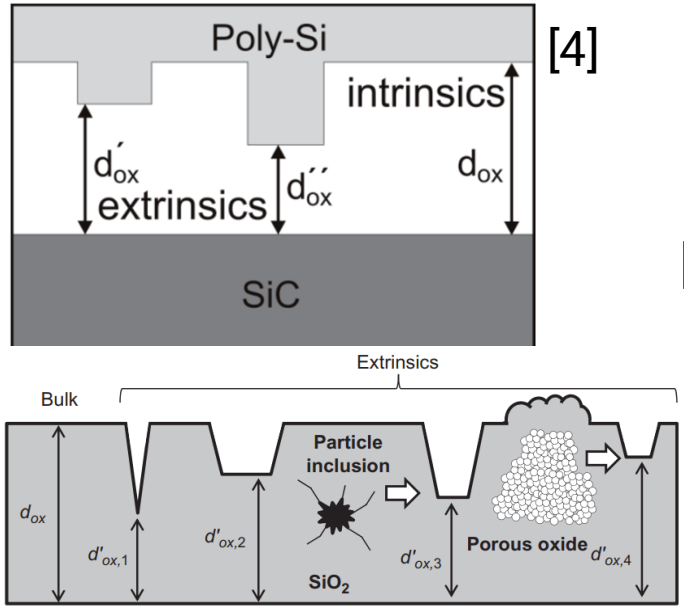


[3]

factor 3-4 less power cycling lifetime

Gate Oxide – The V_{GS} Step Test for Dielectric Stability

- SiC: larger number of gate-oxide defects = extrinsics → screening necessary!
- Beier-Möbius et al. 2016 → verification via new gate-voltage (V_{GS}) step test



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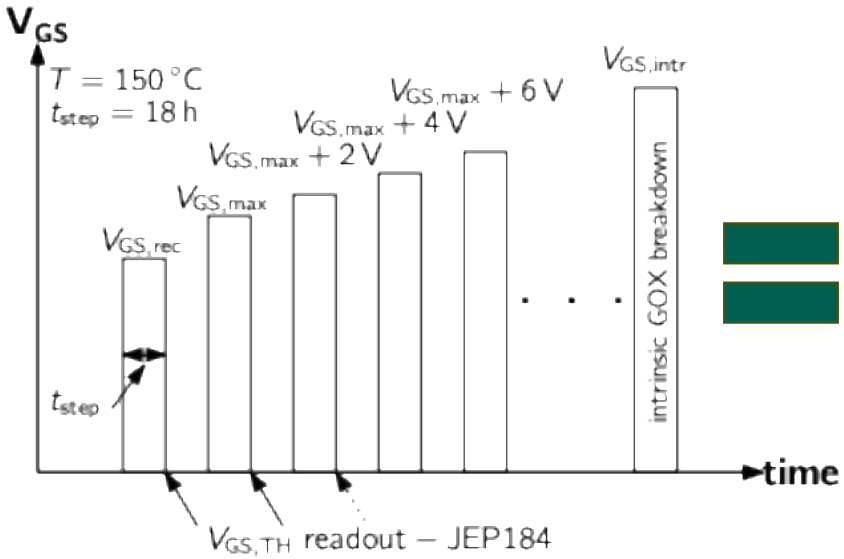
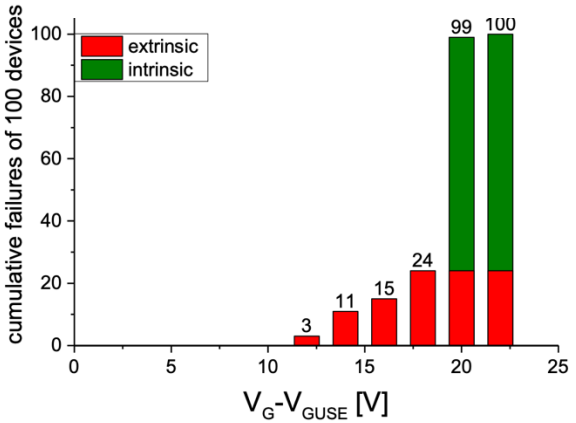
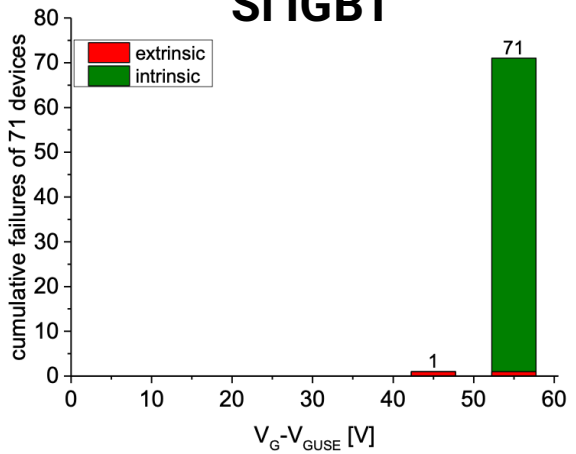


SiC MOSFET



Si IGBT



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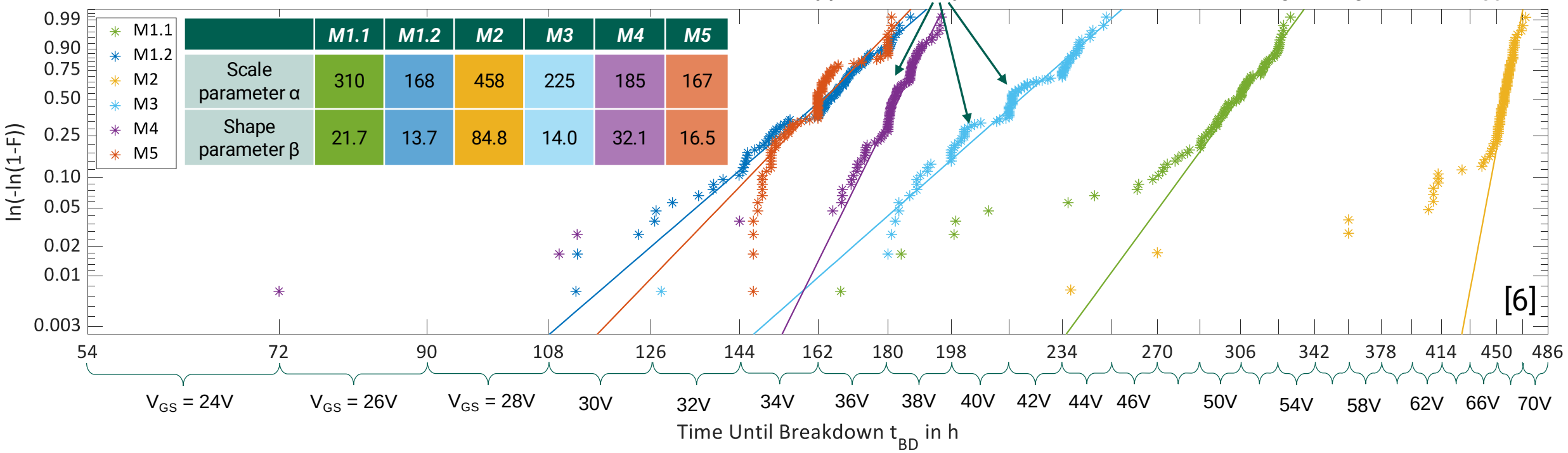
- 2/2023 step test in JEDEC JEP194

Gate Oxide – Actual Step Test Results

typical: many devices reach TDDB in beginning of new V_{GS} level

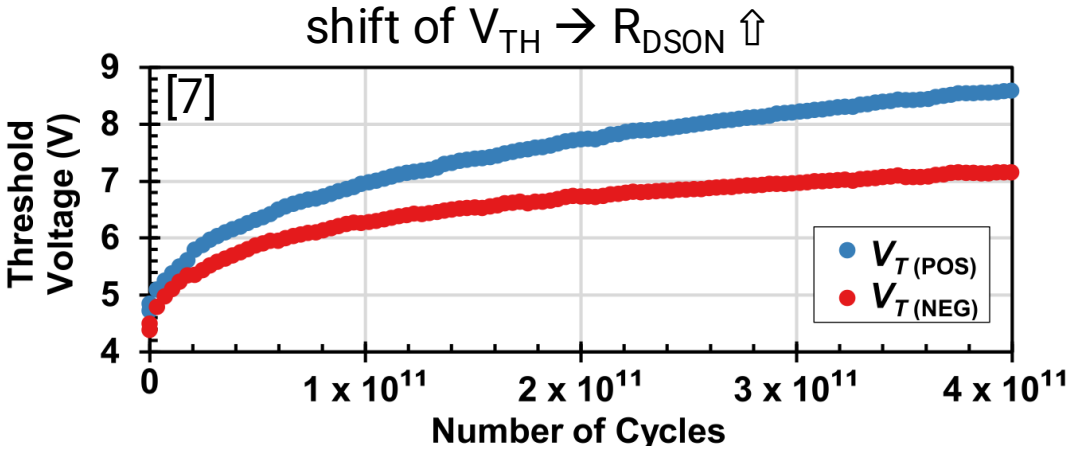


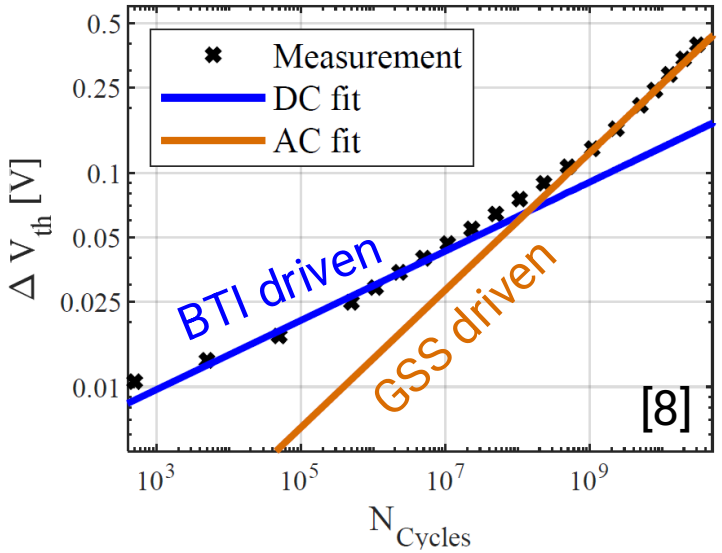
	M1.1	M1.2	M2	M3	M4	M5
Scale parameter α	310	168	458	225	185	167
Shape parameter β	21.7	13.7	84.8	14.0	32.1	16.5

- Strong deviation of intrinsic failures among tested groups
- Apparently, well defined screening procedure by many manufacturers
- Shape parameter describes process stability → β↑ = low oxide thickness variation
- Newer generations with reduced oxide thickness → $R_{on} * A \downarrow$ (M1.1 → M1.2)

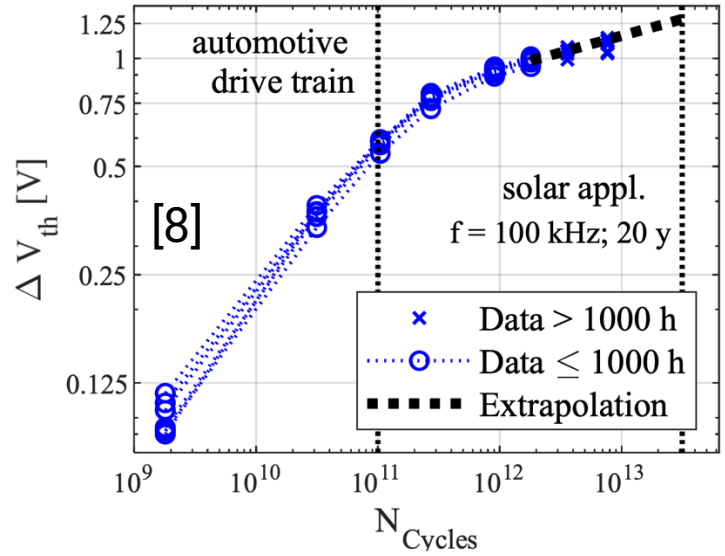
Gate Oxide – Dynamic Instability for SiC MOSFETs – GSS Test

- gate-switching stress (GSS) can lead to threshold voltage V_{TH} shift





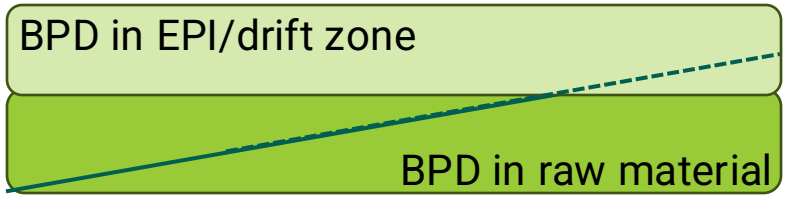
fit for application-near drift via power laws



- new test was introduced
- reason: charging and neutralization of interface traps between SiO_2/SiC leads to modification of interface (traps)

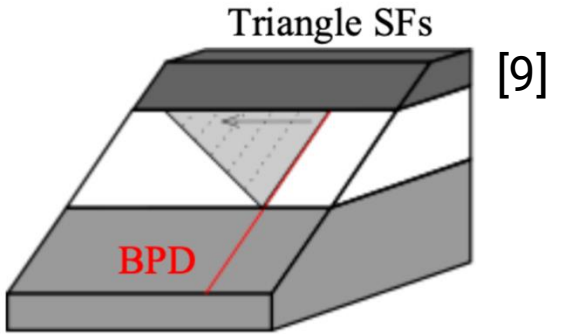
Bipolar Degradation at Initial Crystal Defects

- Basal plane dislocations (BPD) in SiC raw material (500-2000 cm^{-2})
- (4°) off-cut during boule dicing



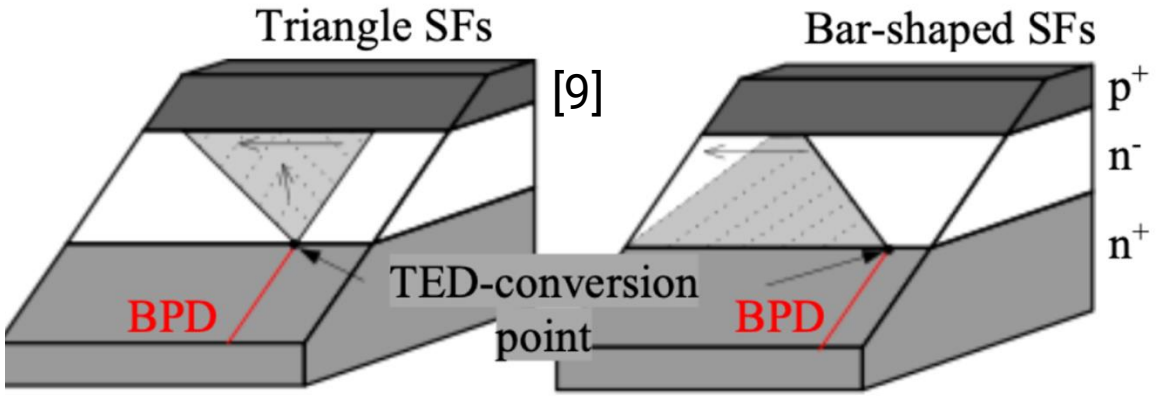
- EPI process should convert BPD in uncritical defects → but not 100%
- BPD can reach through drift zone and critical conversion points could remain

➢ stacking faults (SF) growth at BPDs during bipolar current conduction (e-h recombination)



[9]

= deactivation of active area (R_{DSON} ⇧)

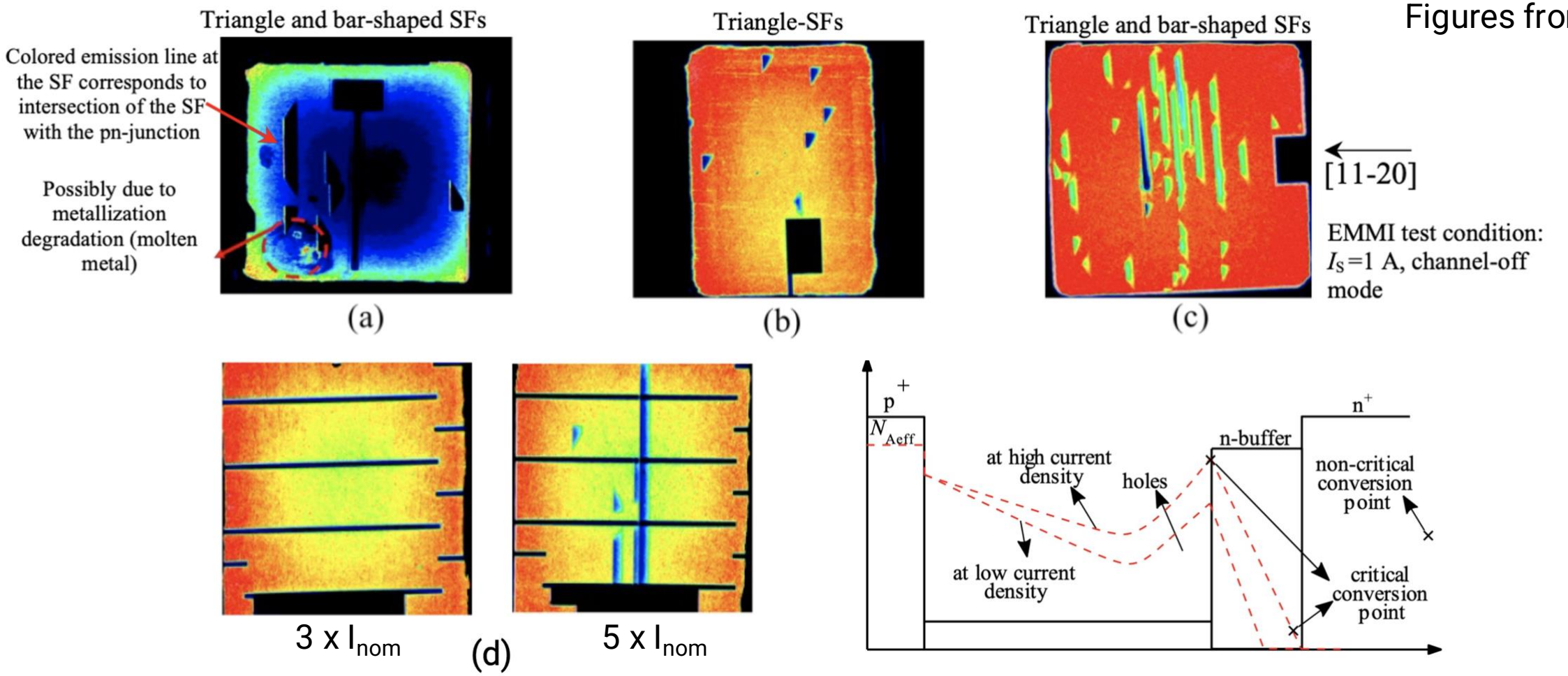


[9]

must be tested under application conditions
DC mode, dead-time mode = new reliability tests

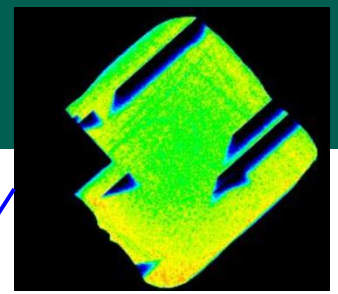
Bipolar Degradation under High Current (Repetitive Surge Current) Here: Electroluminescence Microscopy from the Drain Side

Figures from [9]

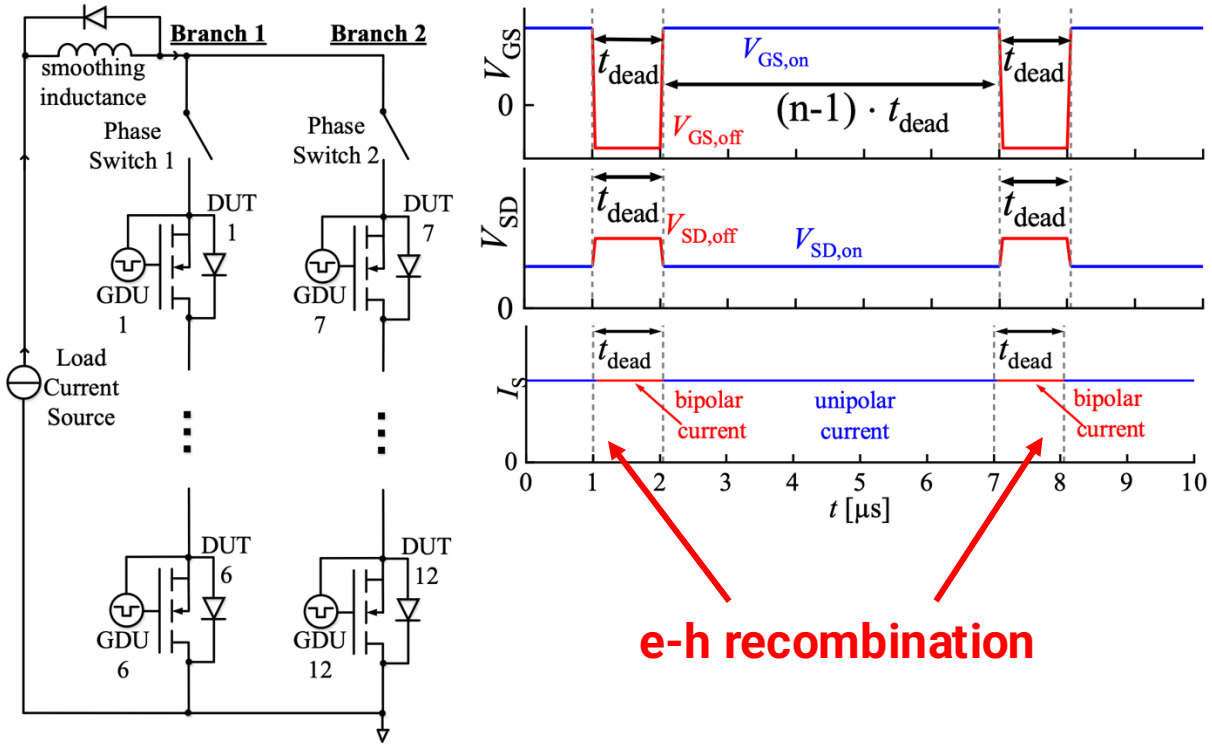


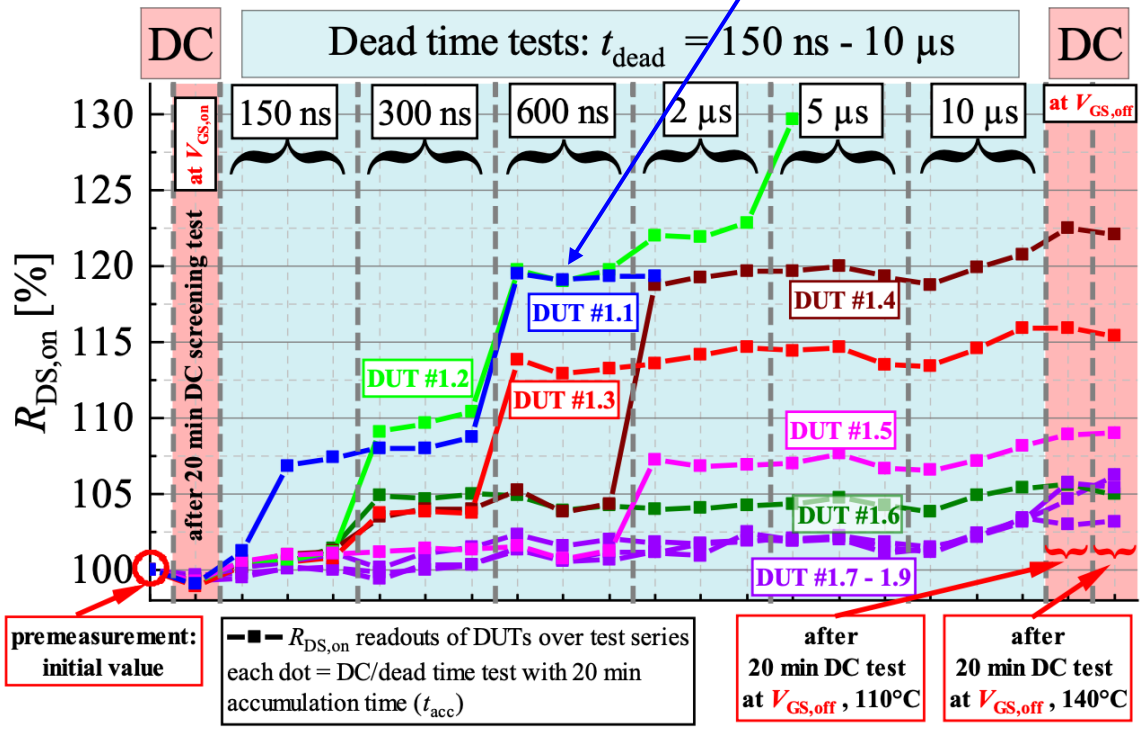
After stress pictures: For (high) currents stacking faults may grow…

Bipolar Degradation under Dead Time Mode



- development of new application-near test concept (TUC + Infineon)





Take-away: Small dead times may help to supress bipolar degradation in the application (one reason: built-up of electron-hole plasma needs some time)

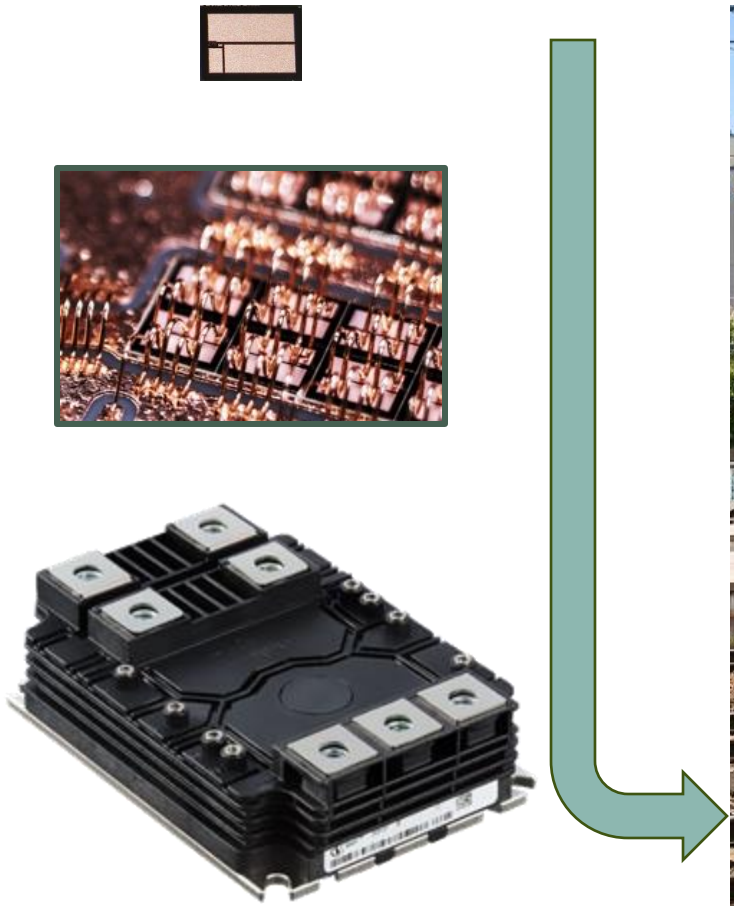
[10] Herrmann et. al. will be published at PCIM/ISPSD'25

Summary

- SiC power devices with specific (new) reliability aspects
- worse mechanical properties → check on **power-cycling** capability
- gate-oxide process more challenging → higher number of point-defects at SiC/SiO_2 interface and higher defect rate within oxide
  - V_{TH} drift due to switching, test stability with **GSS test**
  - enhanced screening, proof with **V_{GS} step test**
- higher amount of crystal defects can lead to bipolar degradation
  - improve crystal quality (supplier)
  - application-near testing with new methods **(“dead-time test”)** + improved physical understanding

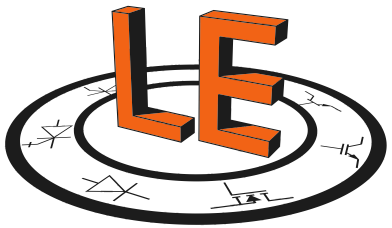
➢ **BUT**: great potential for SiC → much higher efficiency + new applications

High-Power Application Example



New S-Bahn in Munich with 3.3 kV SiC MOSFET with **10-13%** [11] higher overall efficiency

Thank you for your attention!



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