The Unique Role of Thermal Test Vehicles (TTV) for TIM Characterization and Reliability Investigation

41th Chemnitz Seminar
»Test and Reliability Solutions – New Opportunities for Electronic Components and Systems«

NANOTEST
simply measured

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14.02.2025

OUTLINE

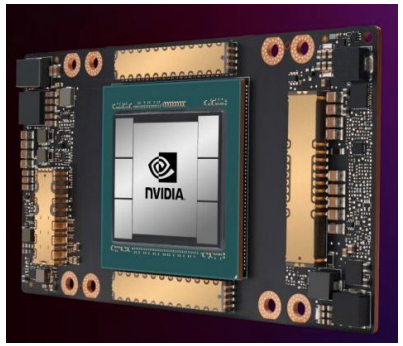
- Motivation
  - Advance packages, high performance computing
  - Challenges for TIMs in HPC packages
- Thermal Test Vehicle solution at NANOTEST
  - Customer specifics TTV solution, all-in-one service
  - Available thermal test chips (TTC)
  - Available thermal test vehicles (TTV)
  - Available TTV control units (TCUs)
- Case study: TTV design and assembly
- TIM Characterization using TTV
- Summary and outlook

Motivation - what are TTV and what are they useful for?

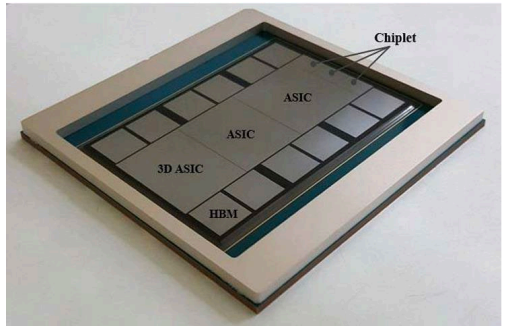
- **Thermal Test Vehicle (TTV)** is a thermal Twin of a package (e.g., CPU, GPU or NPU) to investigate thermal characteristics of these packages
- Simulation of **hot spots and power density variation** and their impact on the package
- Investigation of **Thermal Interface Materials** (TIM1, TIM1.5 and TIM2) under real applications
- Development and investigation of **advanced cooling solutions** (air cooling, liquid cooling, injection cooling etc.)
- **Reliability** investigation of packages
- Development and optimization of **assembly process**

Advance Packages for high performance computing (HPC)

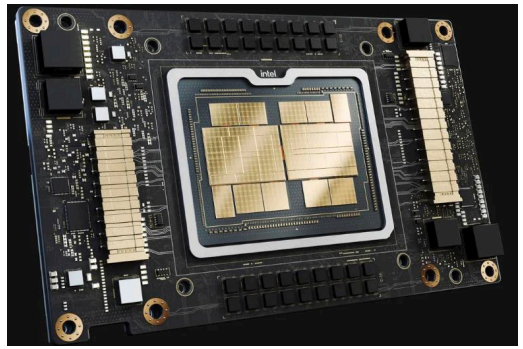
NVIDIA A100



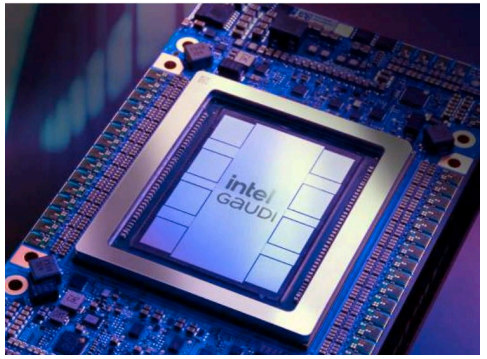
Samsung (ECTC 2024)



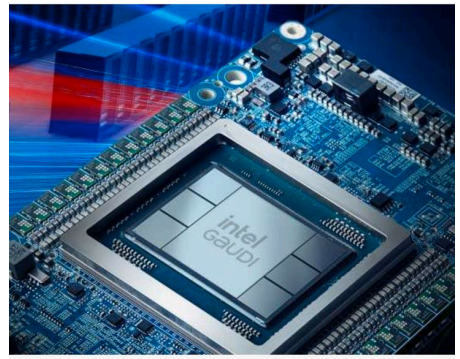
Intel: Ponte Vecchio GPU

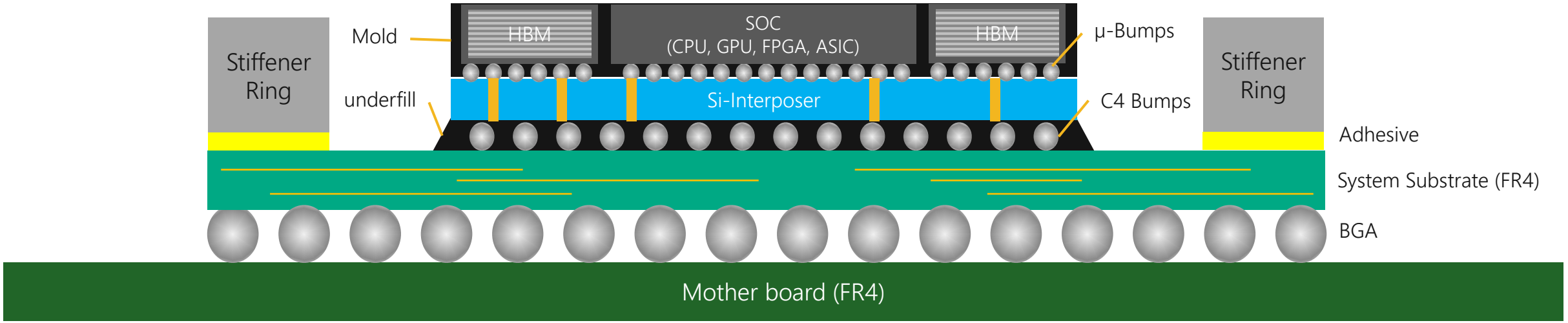


Intel® Gaudi® 3 accelerators



Intel® Gaudi® 2 accelerators

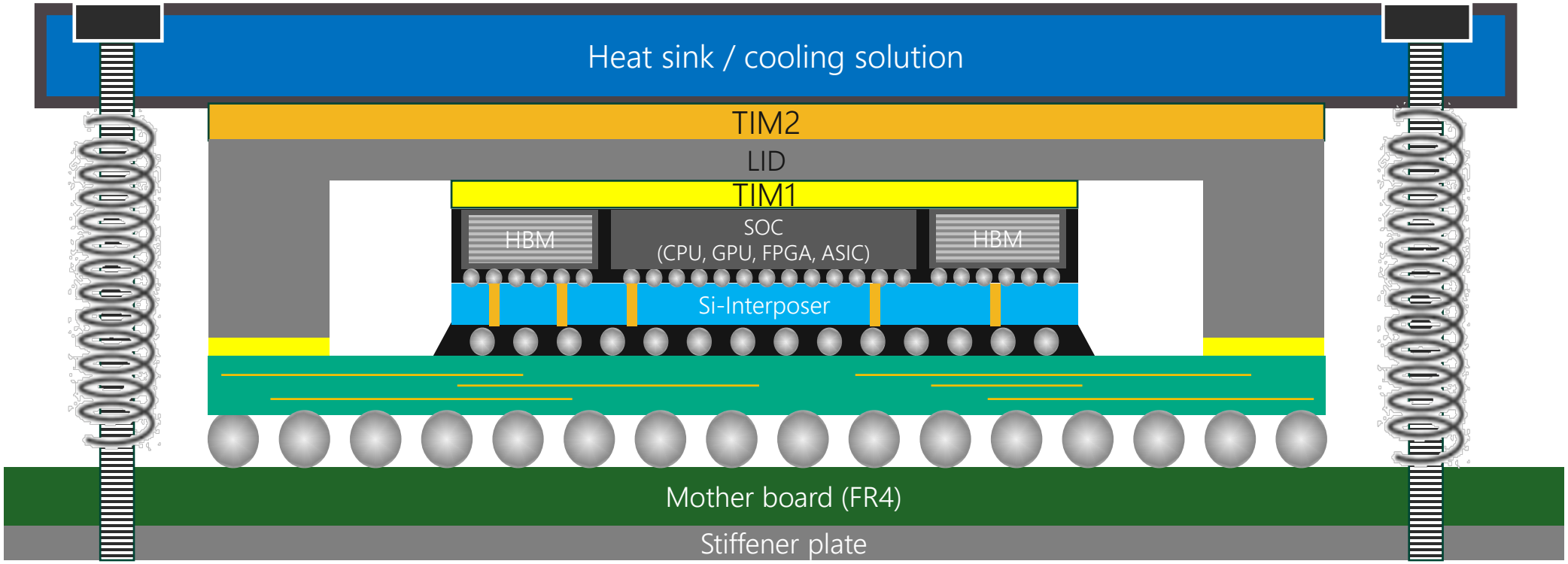




TIMs in advance packages (TIM1 and TIM2)

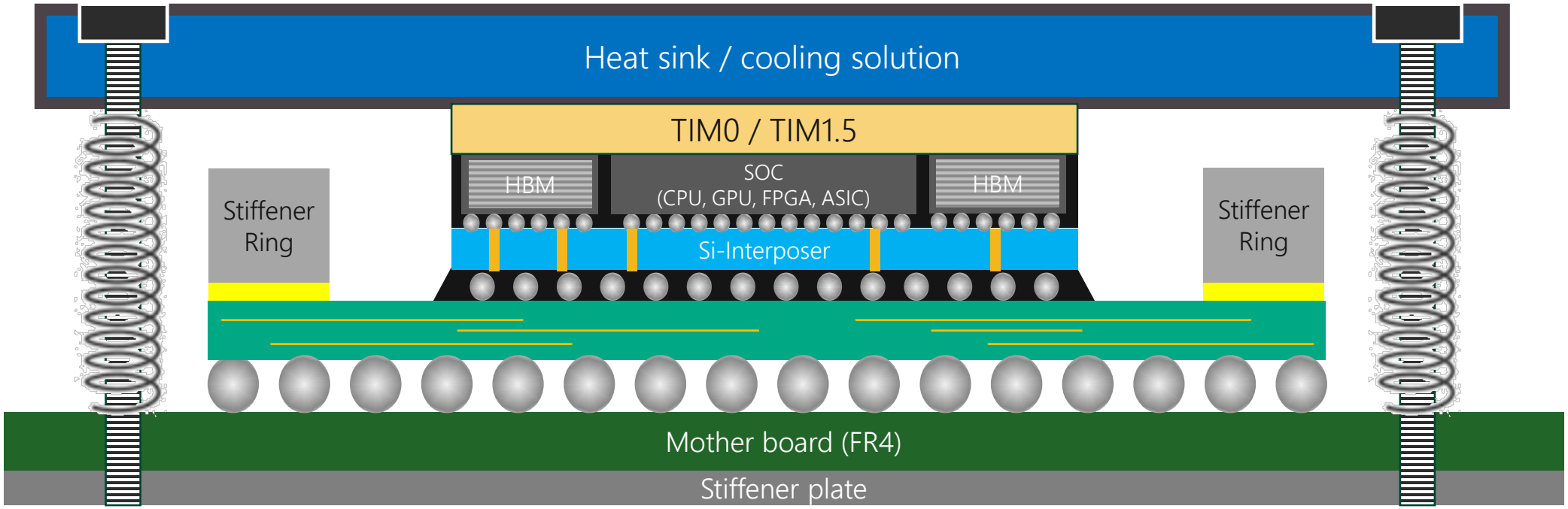
- TIM1 is applied between the silicon die and LID
- Typical TIM1 are PCM, Gel, Grease or metallic TIM
- Typical applications: Data centre, HPC.
- Typical BLT: 20-50µm

- TIM2 is applied between LID and heat sink
- Typical TIM2 are Grease, Pad, Graphite sheet, Gap filler
- Typical applications: Data centre, HPC.
- Typical BLT: 100 - 300µm



TIMs in advance packages (TIM1.5)

- TIM1.5 (sometime called TIM0) are applied directly between the silicon die and the external heat sink in lid-less packages.
- Typical TIM1.5 are PCM, Grease or metallic TIM
- Typical applications: Smart phones laptops or video graphics boards
- Typical BLT: 50-100µm



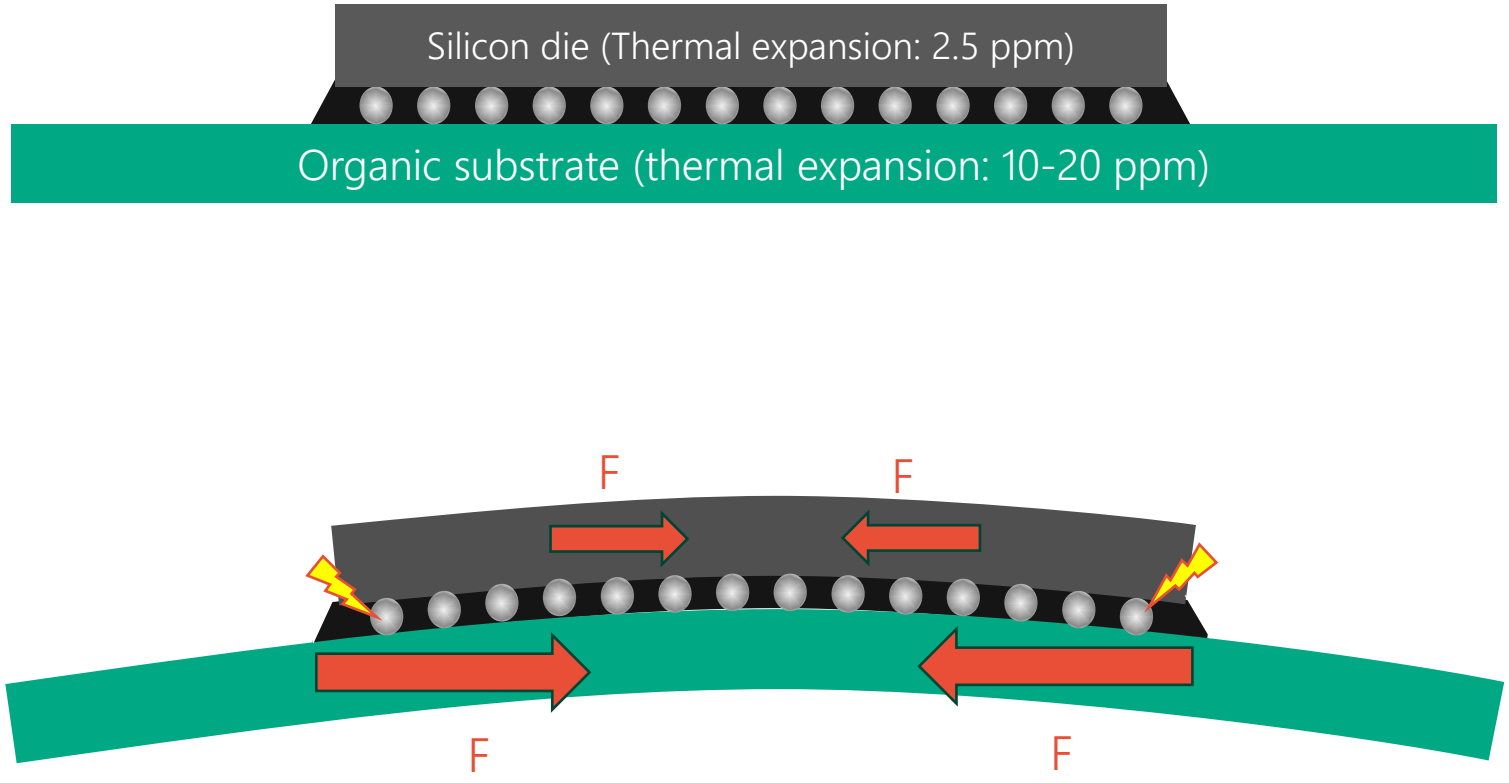
Challenges for TIMs in HPC packages

- **Warpage Challenge**: Increased warpage in chips complicates TIM development, especially for high-performance processors.
- **Increased Die Size:** Larger die areas and multiple dies (chiplet) make TIM application and warpage control more challenging.
- **Material Compatibility**: Ensuring TIM compatibility is crucial, especially for liquid and hybrid TIMs to maintain performance over time.
- **System Design Impact**: Larger TIMs may need thicker layers, affecting design, especially in liquid cooling systems.
- **Long-Term Reliability**: TIM reliability is vital for maintaining system thermal performance and longevity.

Package warpage, why does it occur?

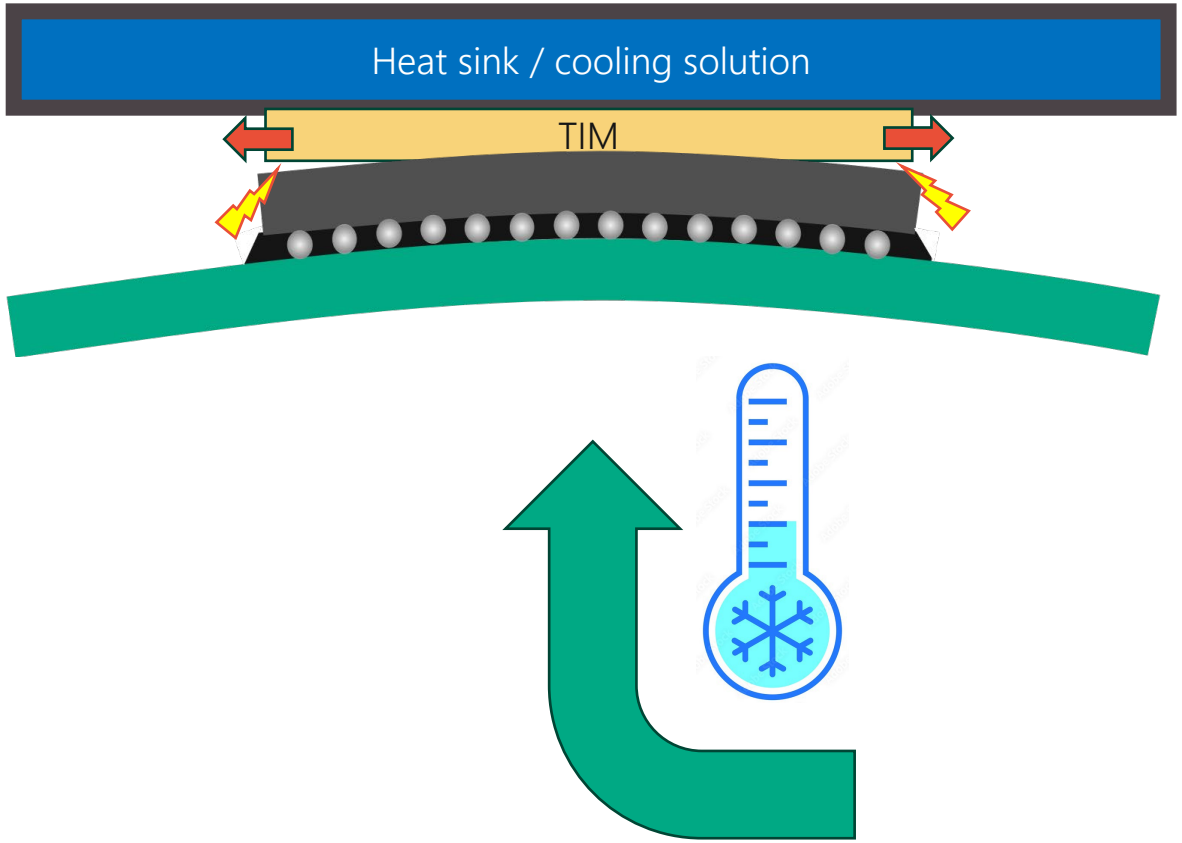
Assembled at higher temperature

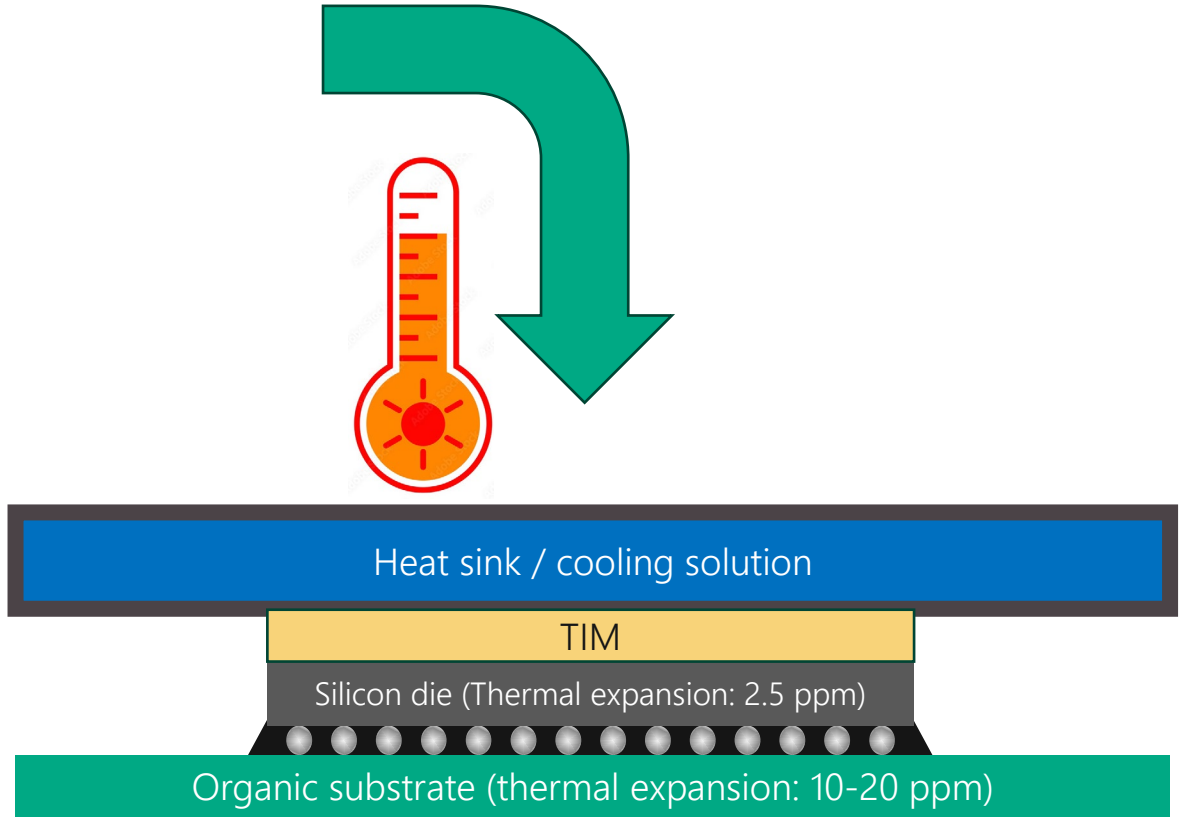
Cooled down to room temperature



Cooling from assembly temperature to room temperature creates stress and warpage due to the thermal expansion mismatch between the silicon die and organic substrate

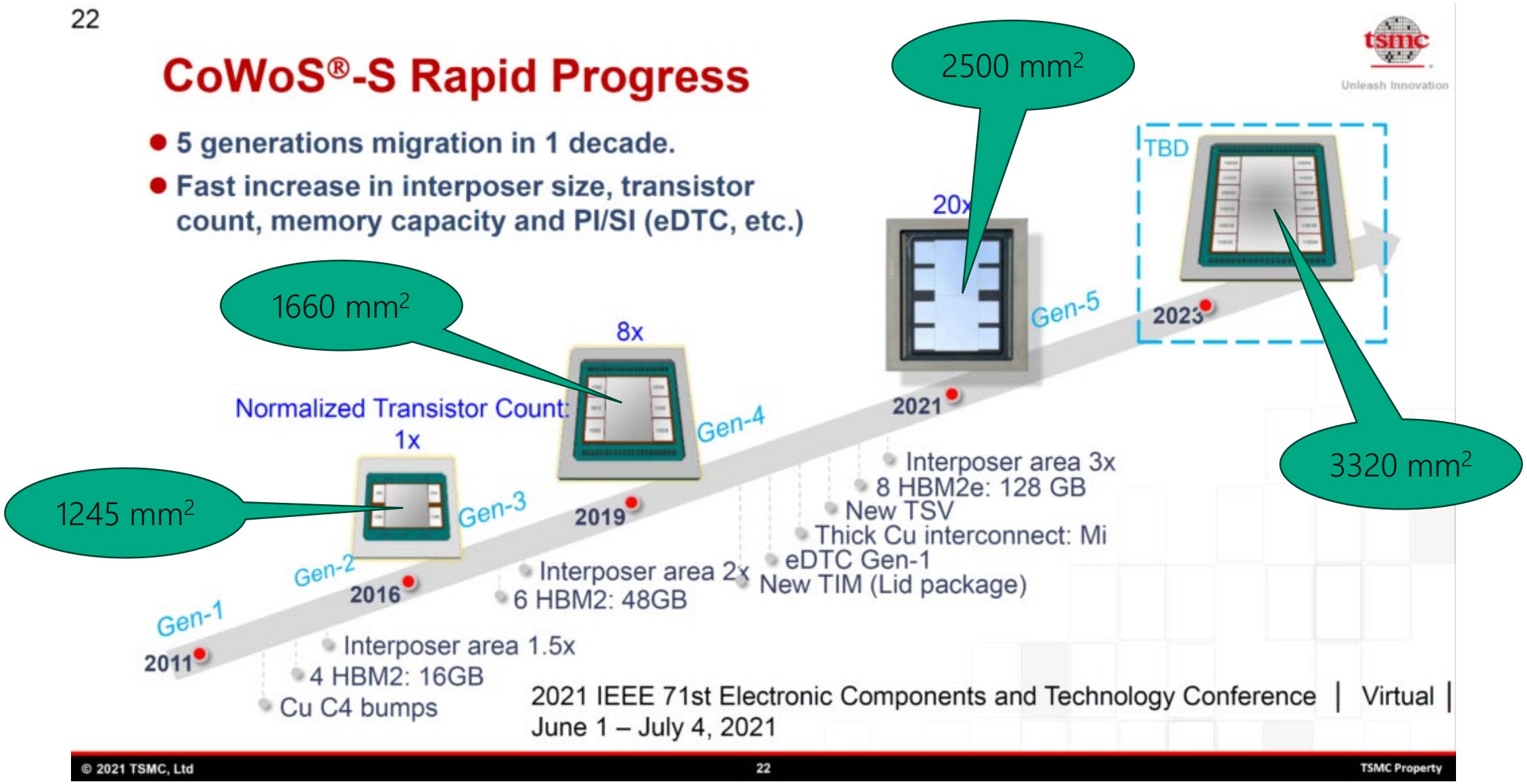
Package warpage and its impact on TIM





Due to the thermal discrepancy between substrate and die, the TIM is exposed to high loads during heating/cooling, which leads to degradation (pumpout, delemination).
The larger the die, the higher the warpage and thus the load from the TIM

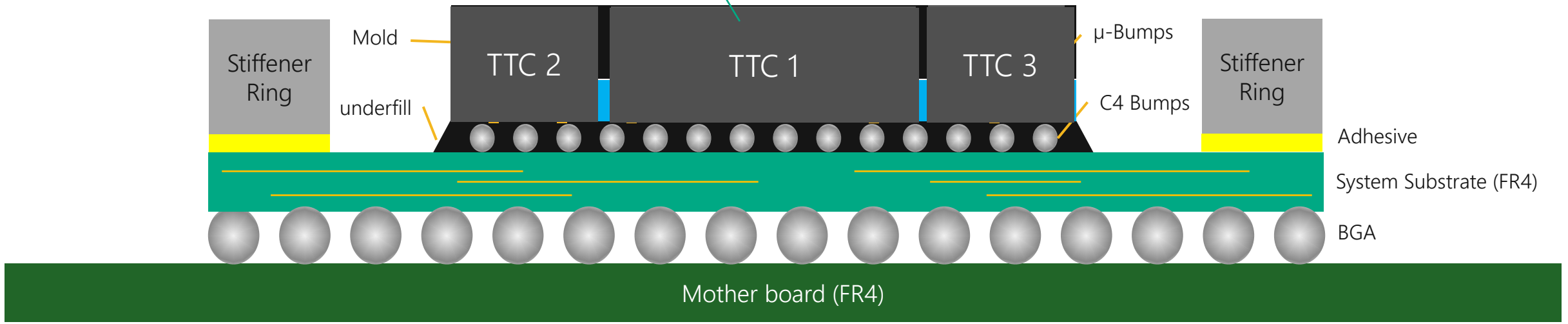
Trend of increasing of die size in HPC packages



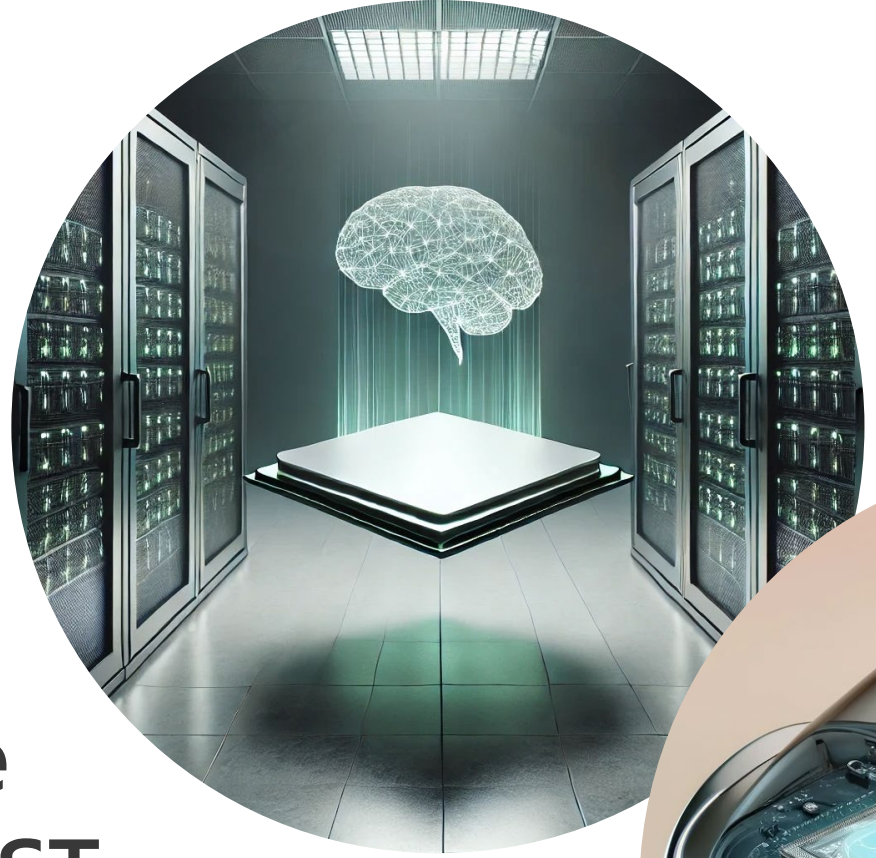
From real package to TTV

- TTCs have adjustable size, controllable heat loss in defined heating zones and localised temperature measurement.
- Real die does not have

TTV = Package simplification, cost-efficient testing and increasing of testability



TTC: Thermal Test Chip



Thermal Test Vehicle solution at NANOTEST

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14.02.2025

NANOTEST

Development steps of Thermal Test Vehicles (TTV)

Design the customized TTV

We support our customers to verify their prospective package, TIMs and cooling solutions by offering TTV solution

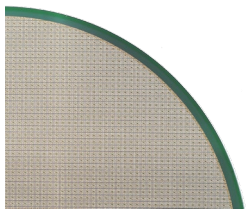
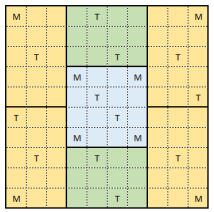
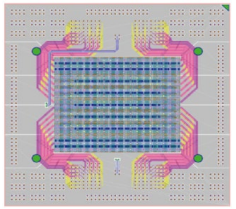
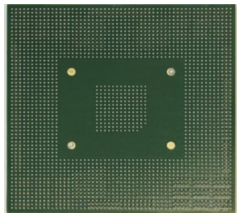
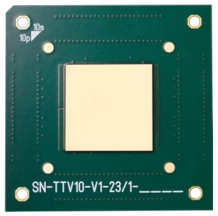
This includes:

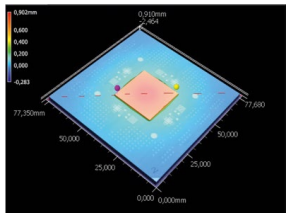
- Chip design and fabrication → Thermal test chips wafer
- Chip configuration → Concept and feasibility
- Design and manufacturing of substrate and ETB
- Assembly and quality assessment
- Measurement hardware
- Measurement and control software
- Calibration and qualification
- Performance and reliability tests

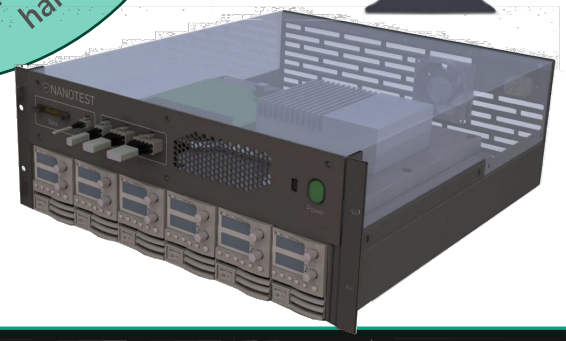
All-in-One Service: From Chip to TTV, with full Equipment and Testing Support

Thermal test chip wafer | Concept and feasibility | Substrate design | Substrate manufacturing | Chip and Board assembly | Quality control and test | Calibration

Measurement hardware | Measurement Software | Performance and reliability tests

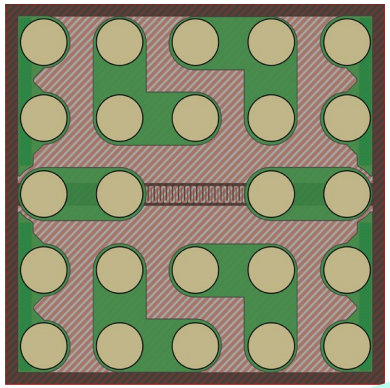








Available Thermal Test Chip (as 8” wafer)

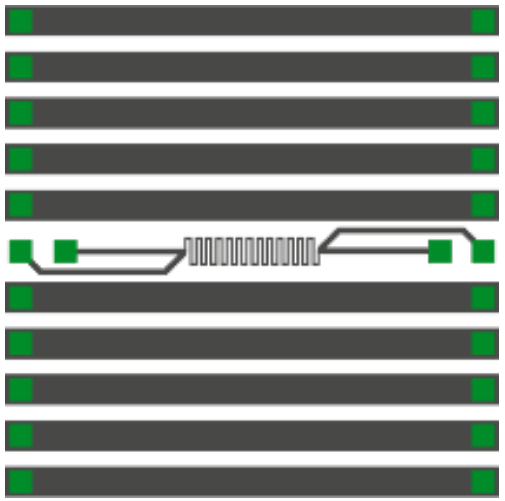
NT20-3k FC



Bumps

- 2.4 x 2.4 mm² unit cells
- 2 heaters, one RTD and 4 monitoring bumps
- 8” wafer / > 4000 cells per wafer
- Power Density: 10 W/mm²
- Wafer thickness: 500 µm or 725 µm undoped silicon
- Flip-chip assembly
- 300 µm SAC bumps with 500 µm pitch
- BSM
  - Ti-NiV-Au (100nm-300nm-200nm)
  - NiV-Pt-Au (300nm-100nm-200nm)
  - Pure silicon

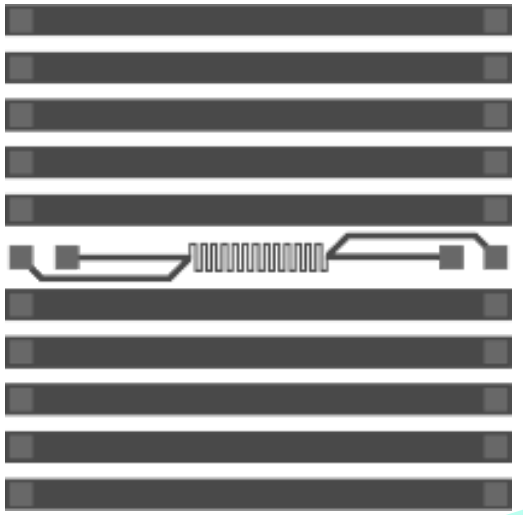
NT16-3k FC



Cu-Pilar

- 3.2 x 3.2 mm² unit cells
- 10 heaters and one RTD
- 8” wafer / > 2400 cells per wafer
- Power Density: 10 W/mm²
- Wafer thickness: 620 µm undoped silicon
- Flip-chip assembly
- 80 µm Cu-pillars with 300 µm pitch
- without BSM

NT16-3k WB

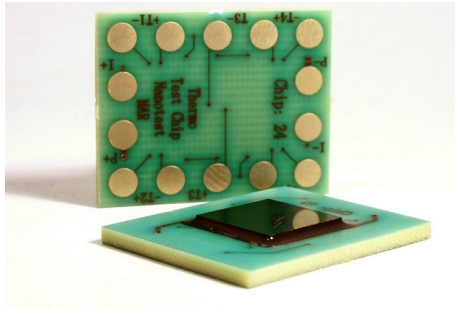


Wire bond

- 3.2 x 3.2 mm² unit cells
- 10 heaters and one RTD
- 8” wafer / > 2400 cells per wafer
- Power Density: 10 W/mm²
- Wafer thickness: 400 µm undoped silicon
- Wire-bond assembly
- 150µm Aluminum pads
- BSM: Ti-NiV-Au (100nm-300nm-200nm)

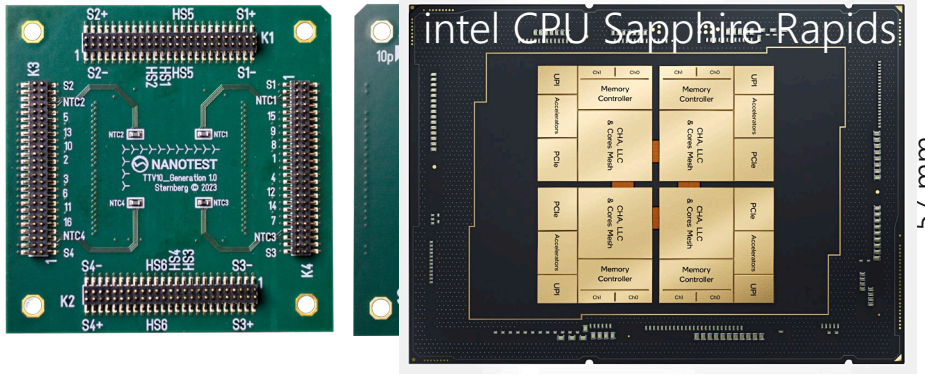
Off-the-shelf Thermal Test Vehicles (small – large – larger)

TTV5



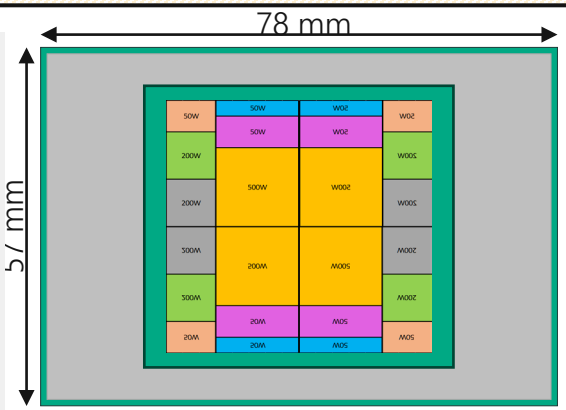
- Based on the NT16-3k-FC
- Chip size: 9.8 × 9.8 mm²
- Substrate Size: 25 × 20 mm²
- Blank silicon surface
- 5 Temperature sensors (RTDs)
- Uniform resistor heater
- **Total power: 140W**

TTV10



- Based on the NT20-3k-FC
- Chip size: 24.9 × 24.9 mm²
- Substrate size: 60 × 60 mm²
- Chip BSM: NiV-Pt-Au
- 16 Temperature sensors (RTDs)
- 4 Independent heater zones
- **Total package power: 2000 W**

TTV16 (coming soon)*

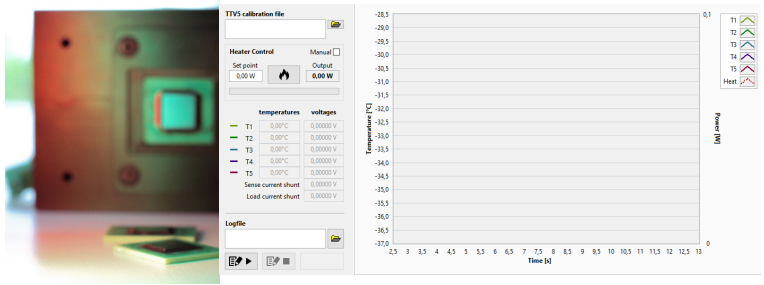


- Based on the NT20-3k-FC
- Chip size: 39.9 × 39.9 mm²
- Available as single die or 4-dies chiplet
- Substrate Size: 78 × 57 mm²
- Chip BSM: Ti-NiV-Au
- 56 Temperature sensors (RTDs)
- 24 Independent heater zones
- **Total package power: 4000 W**

* Available from Q2 2025

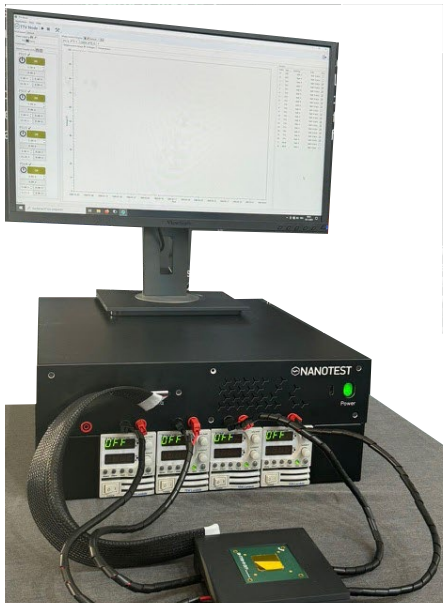
Control and measurement system for off-the-shelf TTVs

Control unit for TTV5



- Hardware-software combination
- Designed for NT16-TTV5
- Features:
  - Heater control (automatic / manual)
  - Temperature monitoring
  - Data Logging

Control unit for TTV10



- Controlling of power suppliers
- Measurement and visualisation of RTDs
- Scheduling for active power and temperature cycles
- 19” case (stand-alone and integrable)
- 4 Programmable PSU
- DAQ with 8 Analog channels

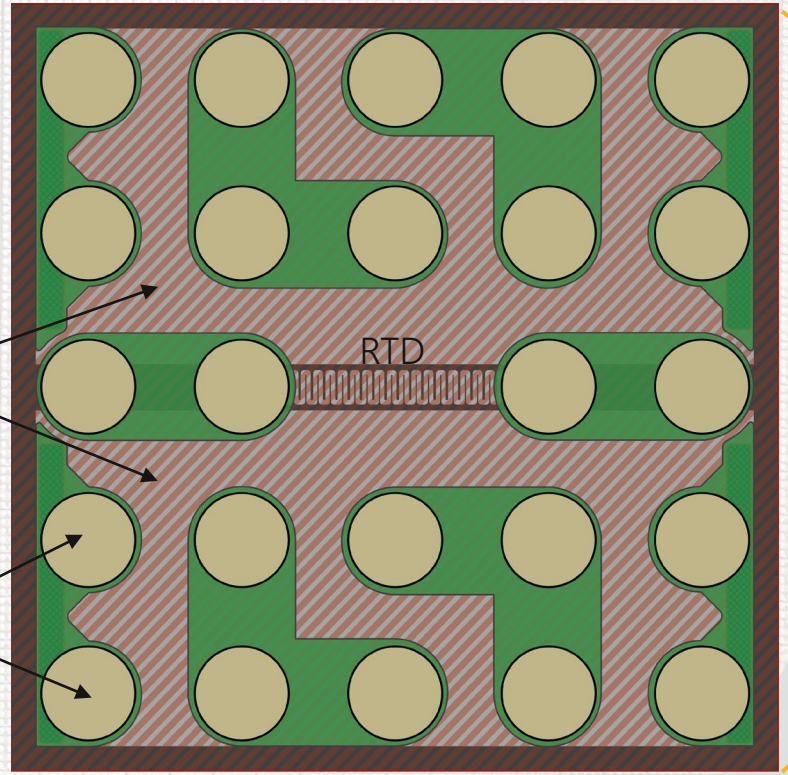
Control unit for TTV16*

* Available from Q2 2025

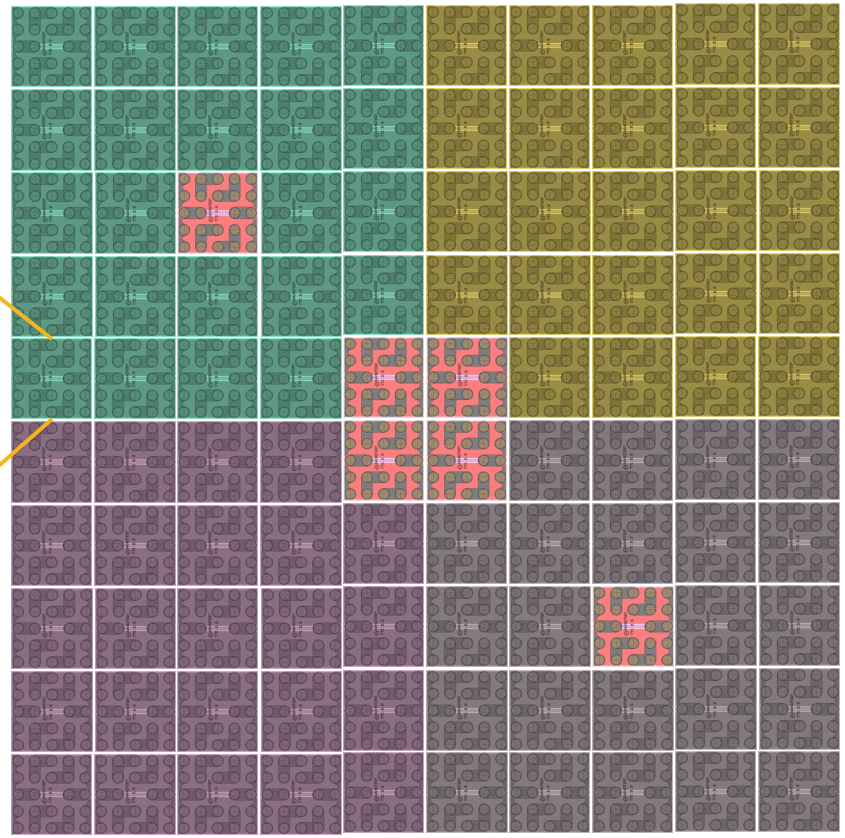
Case Study: TTV design and assembly

Chip configuration

Unit cell



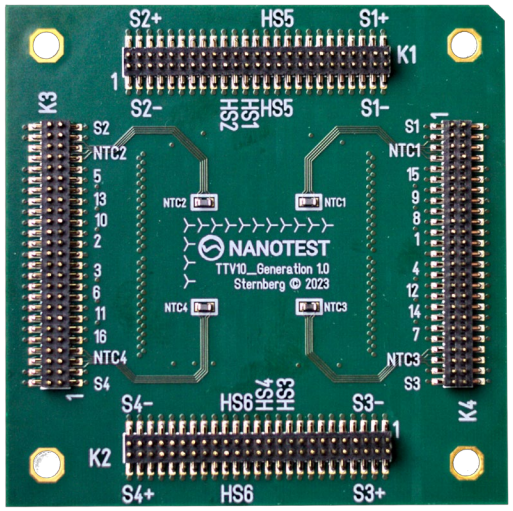
Cell array

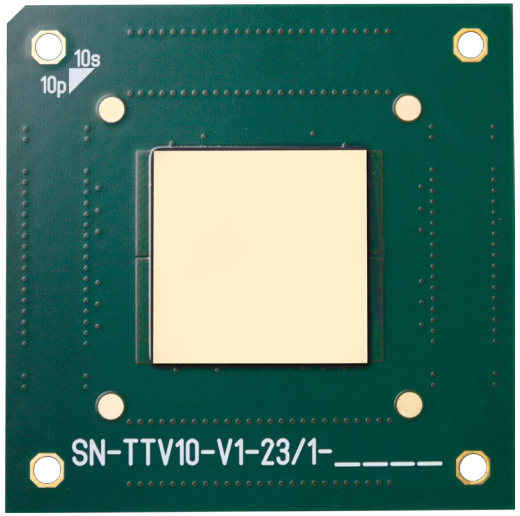


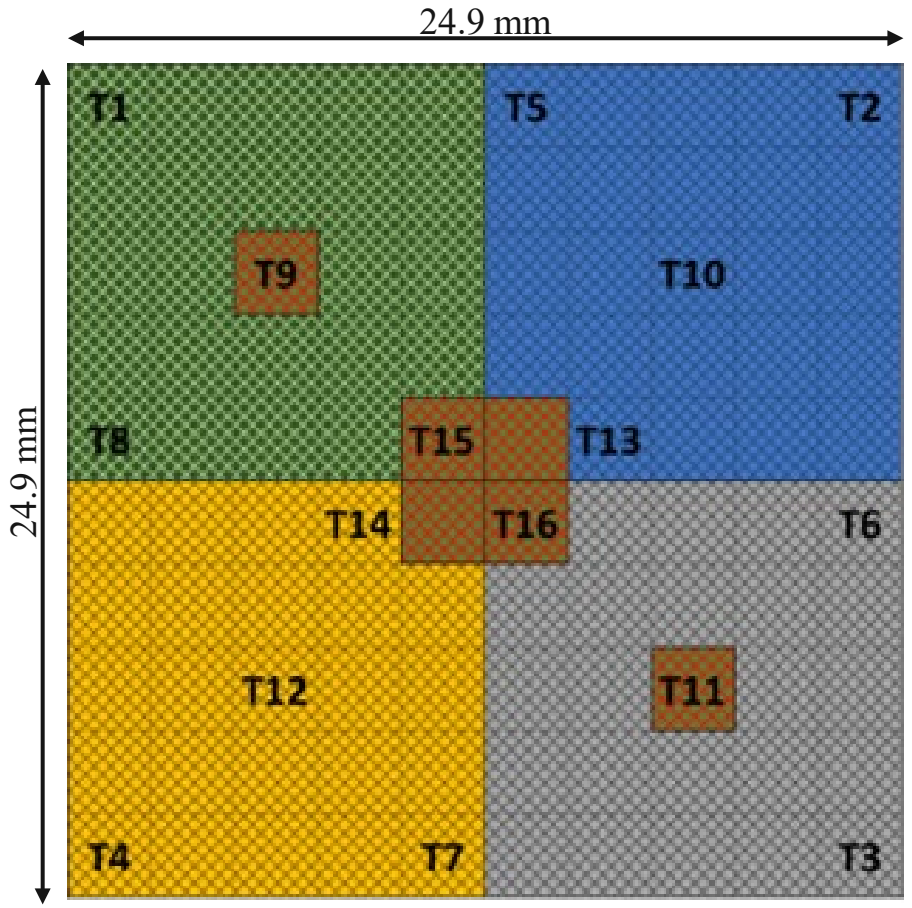
- 10 x 10 cells | 24.9 x 24.9 mm² chip size
- 4 heater zones | 6 hotspots | 16 RTDs
- 10W/mm² => P=2000 W

Thermal Test Vehicle (TTV)

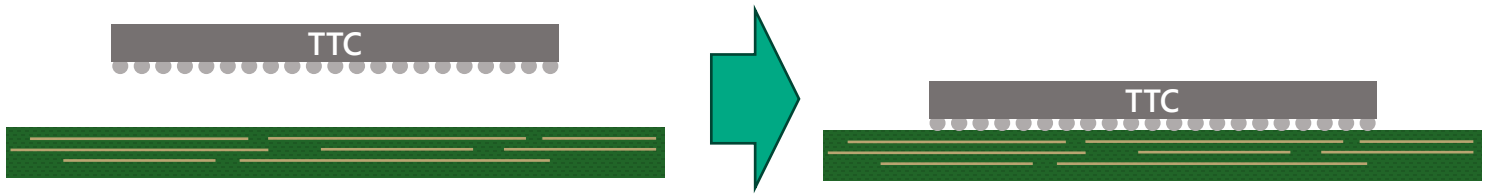
- Die area of 620 mm² (10x10 unit cells)
- Substrate 60x60 mm²
- Four quadrant power zones of 12.4 x 12.4 mm²
- Single cell hotspots
- 16 RTD (corner, edge, center and more)

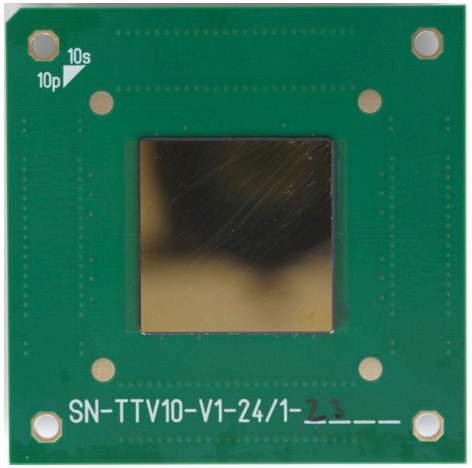


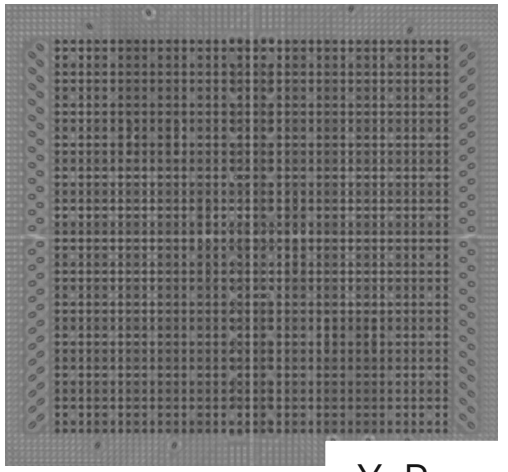




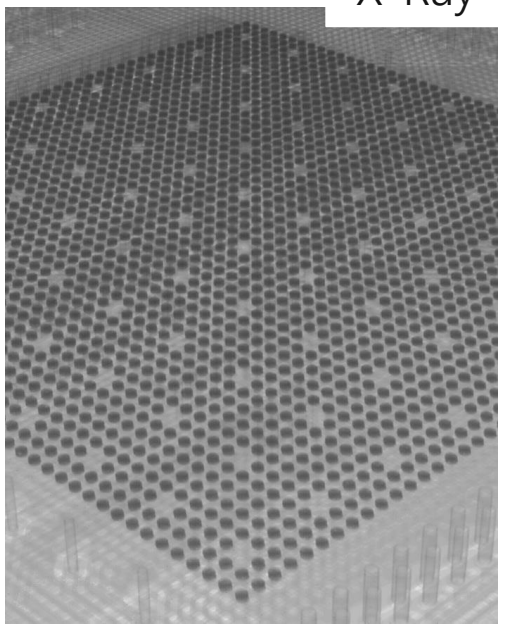
TTV assembly 1 (Reflow process)



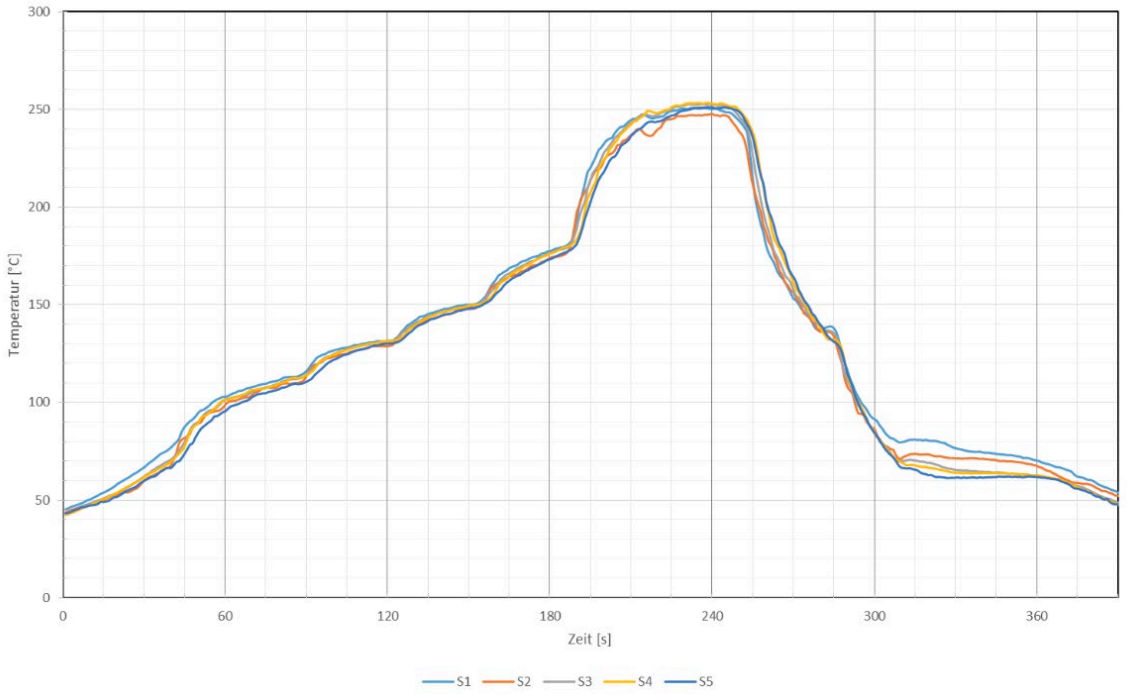




X-Ray



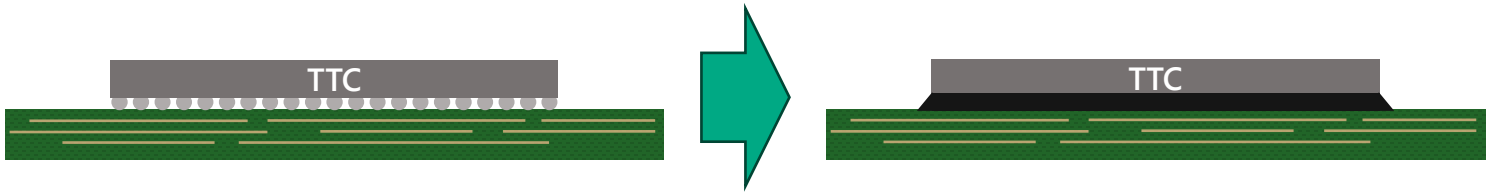
Solder profile for SAC 305 solder

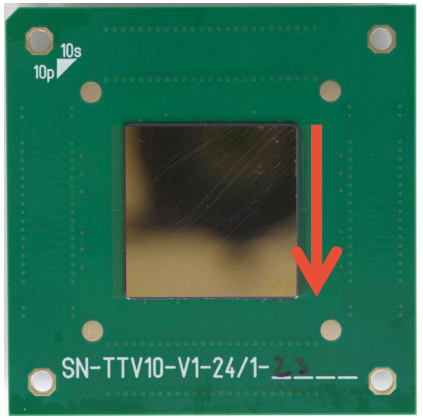


Reflow parameters:

- Transport speed: 650 mm/min
- Peak temperature: 254,5 °C
- Heating rate: 1.8 K/s
- cooling rate: 2.6 K/s

TTV assembly 2 (underfill process)





4 TYPICAL PROPERTIES *

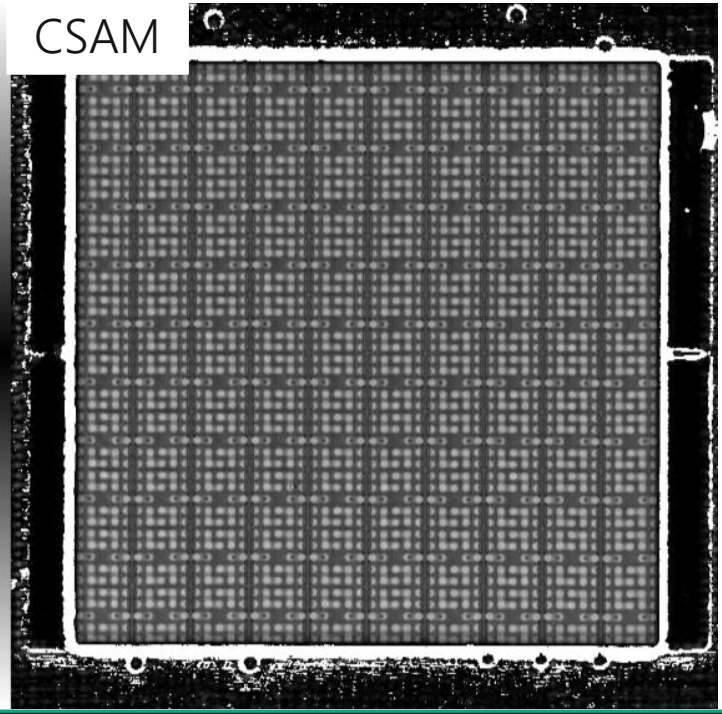
Parameter		Unit	Note / Condition
U8410-377			
Filler Content	55	wt%	
Filler Size Mean Max	0.5 0.6	μm	Measured by laser diffraction
Color	Black		
Viscosity	15	Pa·s	@25°C
Thermal Conductivity	0.40	W/mK	
Tg DMA TMA	160 128	°C	Dual Cantilever Beam Compression
Coefficient of Thermal Expansion (CTE) <Tg >Tg	30 105	ppm/°C	TMA
Bending Modulus	8.6	GPa	
Bending Strength	145	MPa	
Storage Modulus (DMA) <Tg >Tg	8.6 0.20	GPa	Dual Cantilever Beam
Volume Resistivity Initial Afer PCT	>1.0x10¹⁵ >1.0x10¹²	Ω·cm	DC 500V PCT: 121°C, 2atm, 20 hours
Impurities Concentration Cl^- Na K	< 20 < 5 < 1	ppm	PCT: 121°C, 2atm, 20 hours

* This data is for reference and is not guaranteed.

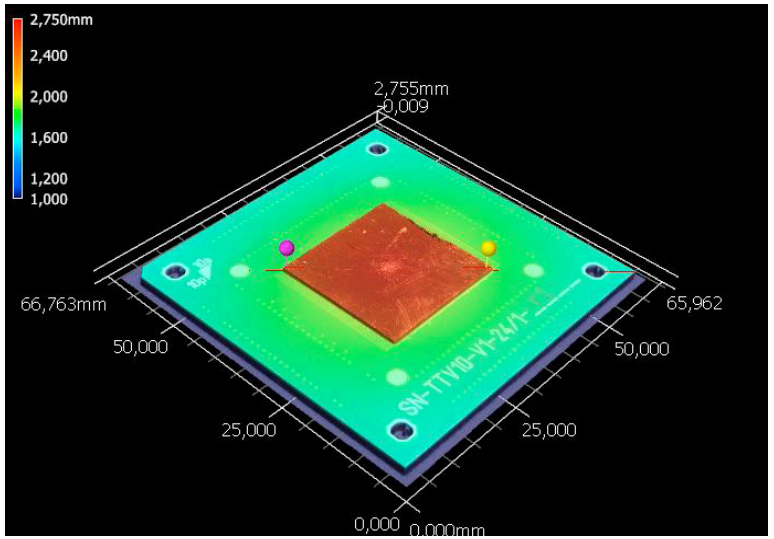
Underfill parameters:

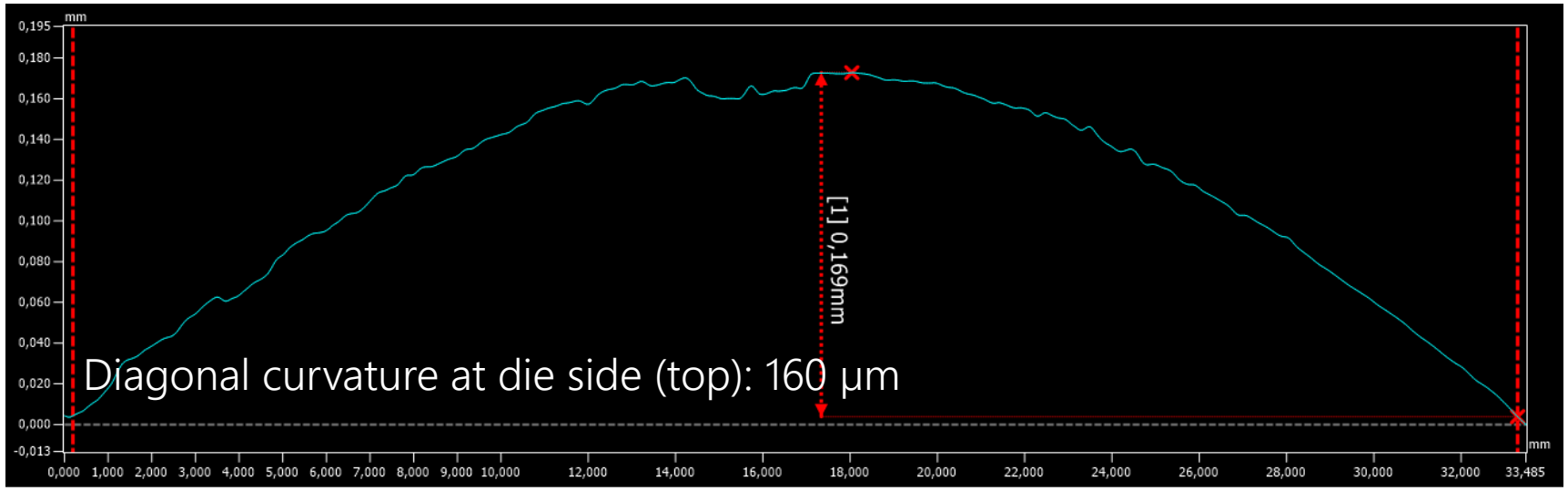
- Used Underfiller: Namics U8410-377
- Curing condition: 120 min @ 165°C
- Substrate temperature: 80°C
- Flow time: 3 min

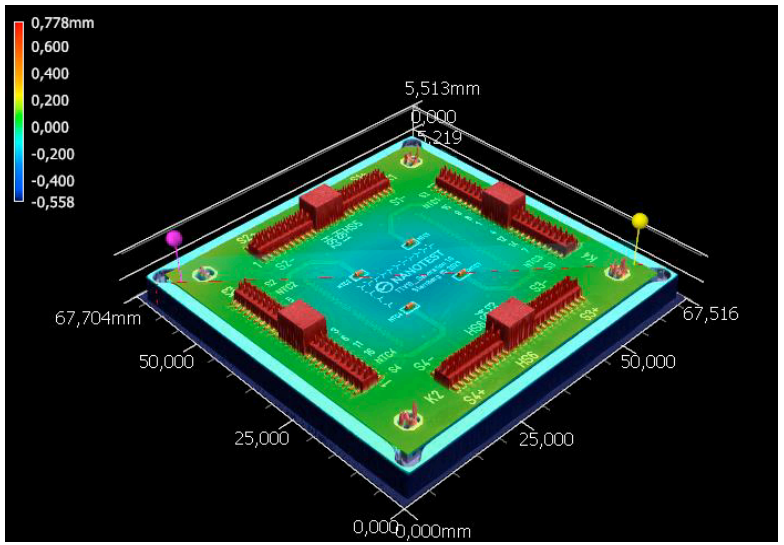
Underfill results:
No voids
No delamination

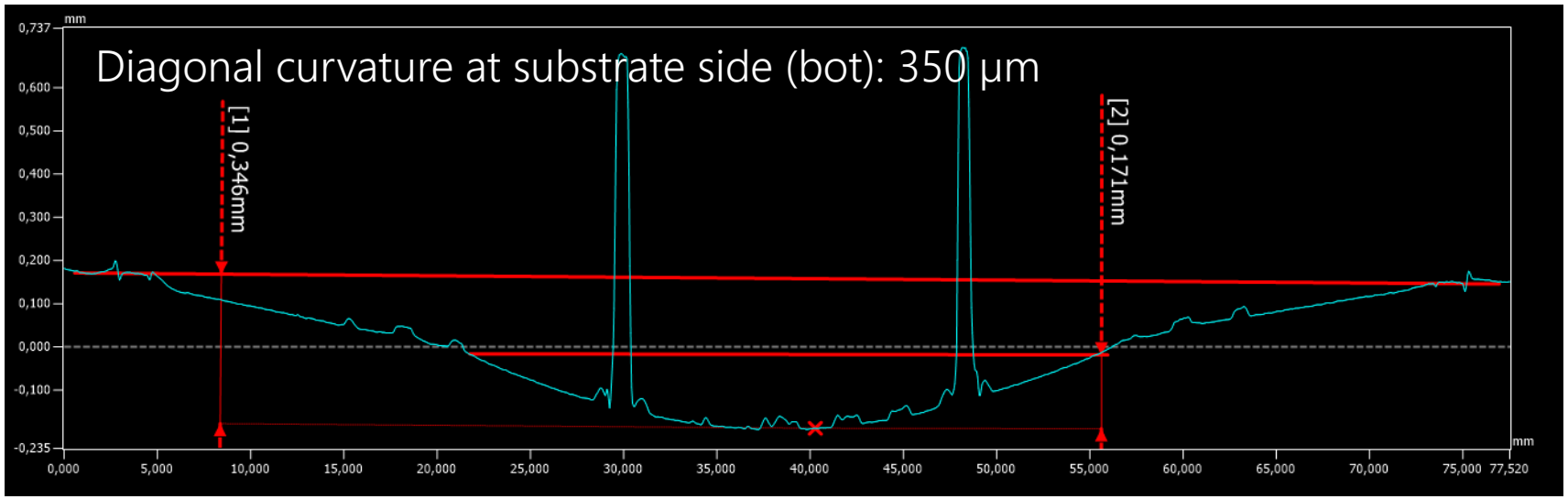


Warpage measurement of both sides (at room temperature)



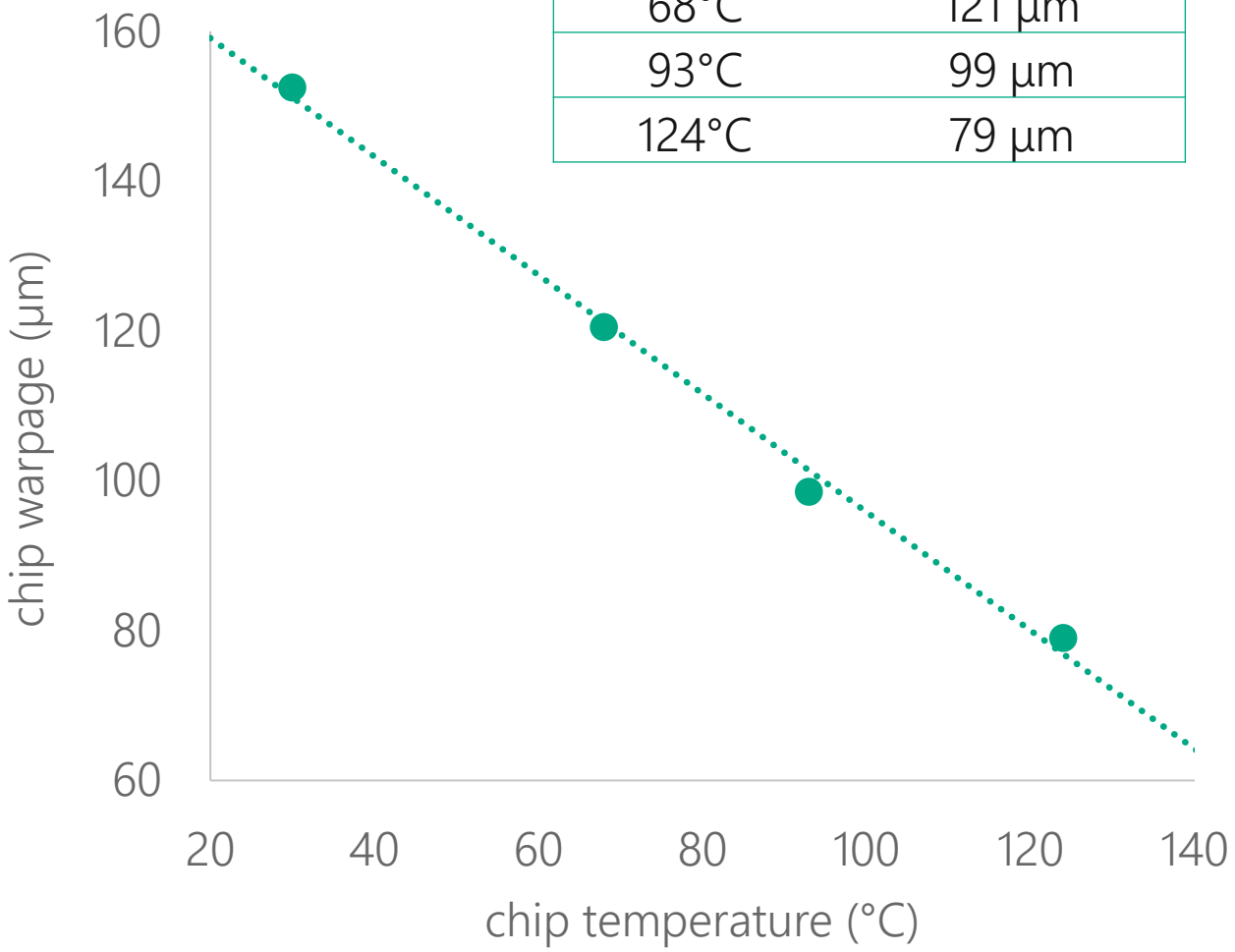


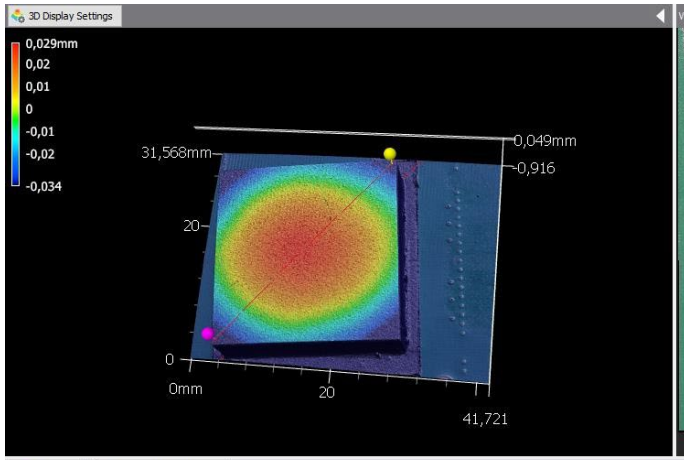


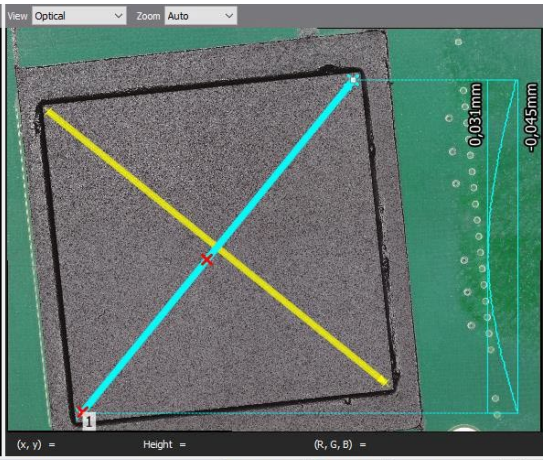


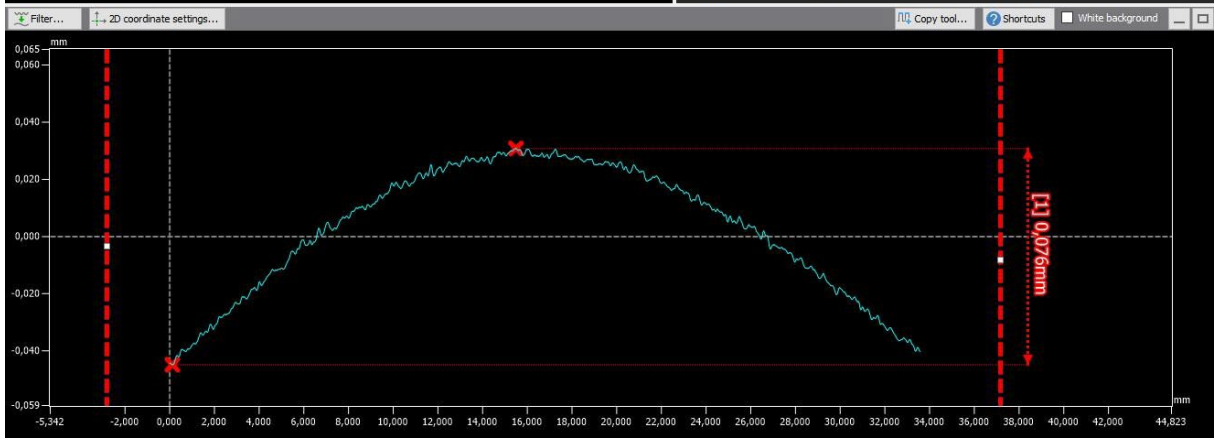
Chip warpage at different chip temperature (active heated)

chip temp.	chip warpage
30°C	153 µm
68°C	121 µm
93°C	99 µm
124°C	79 µm





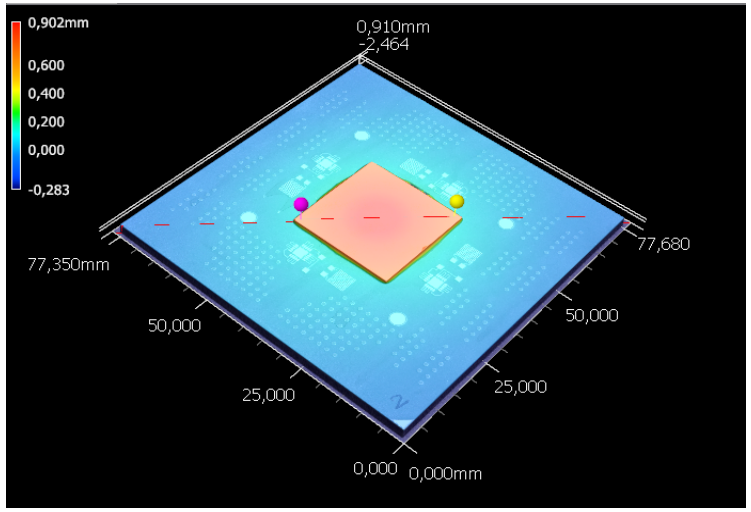


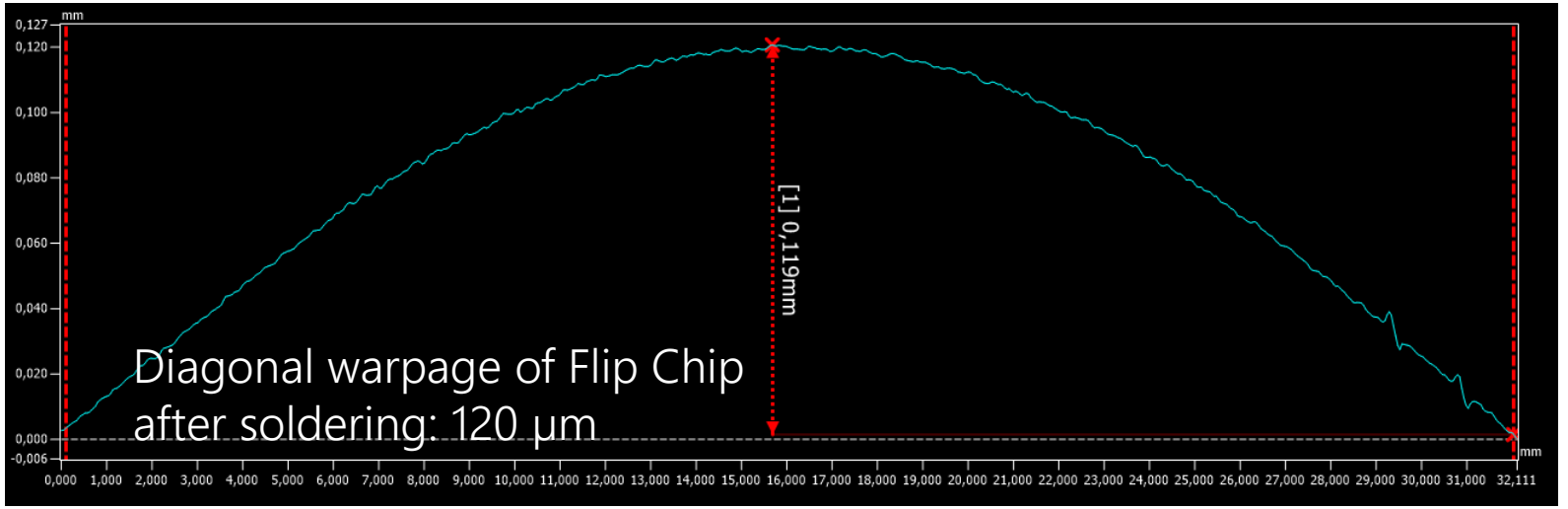


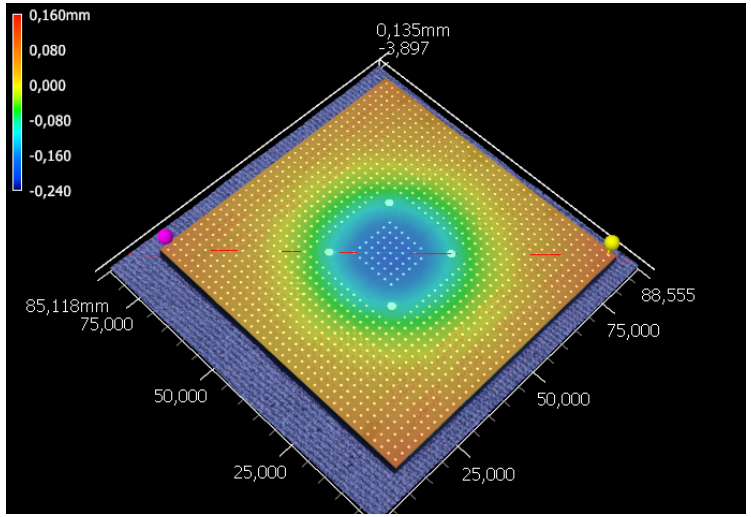
How to reduce chip warpage?

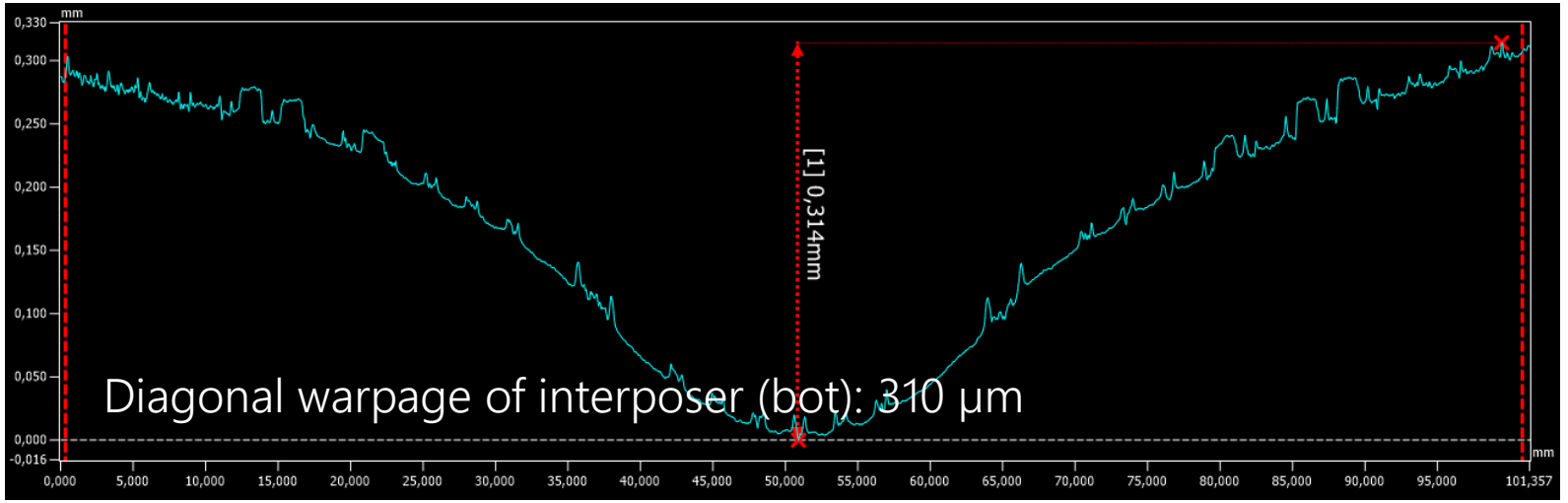
Warpage (after Flip Chip soldering and underfill)

Die size: 25mm x 25mm, package size: 75mm 75mm. Without stiffener ring



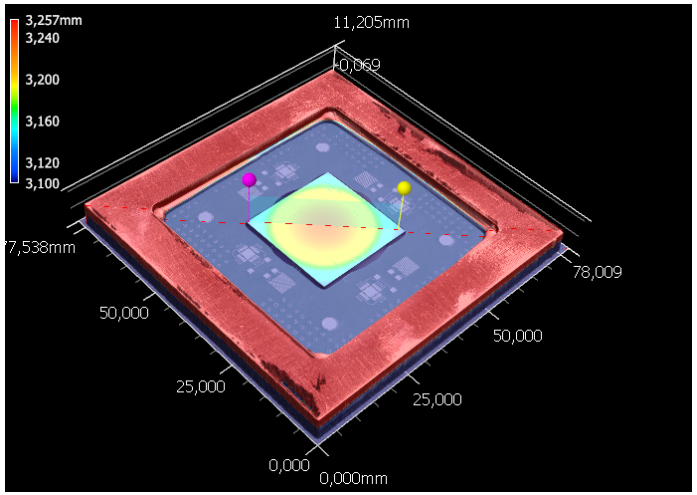


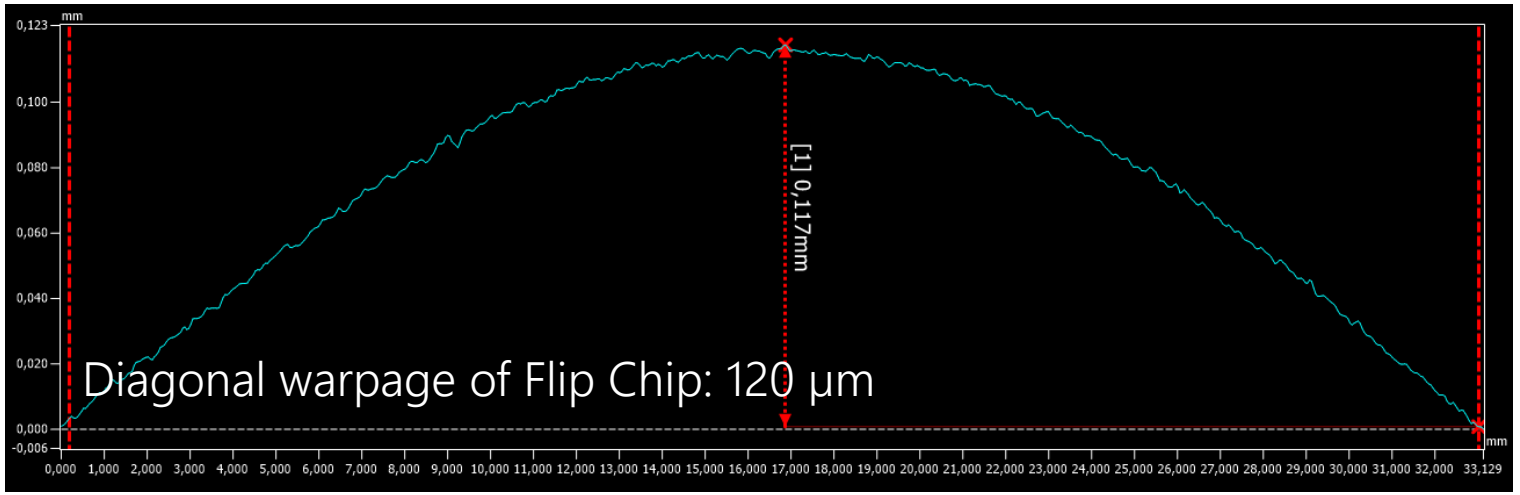


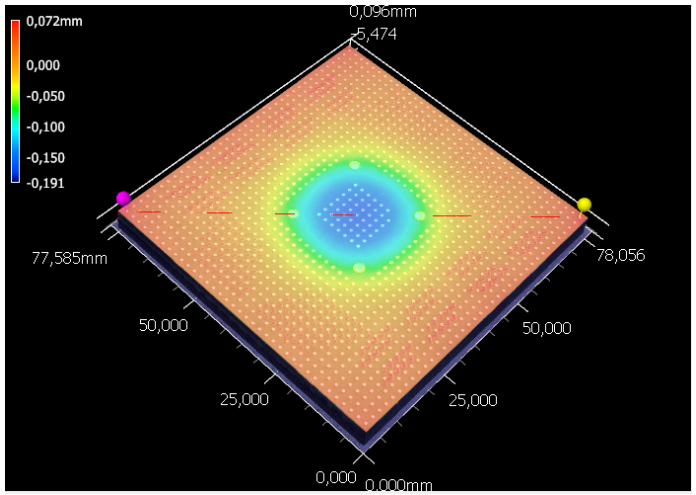


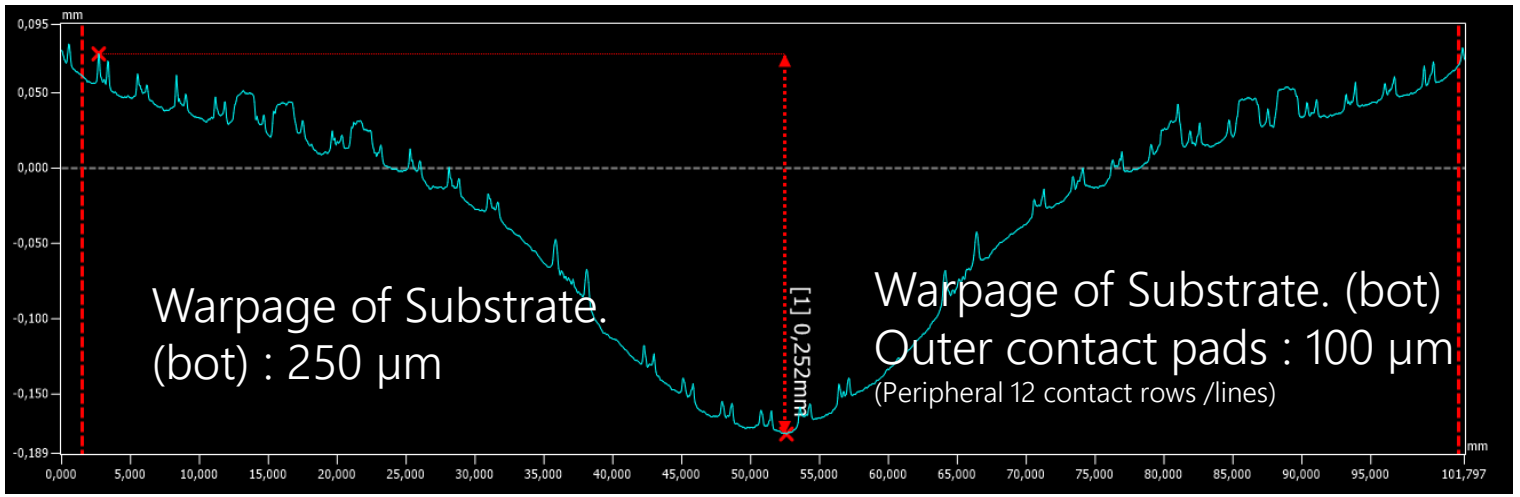
Warpage (with mounted stiffener ring)

Die size: 25mm x 25mm, package size: 75mm 75mm. With stiffener ring





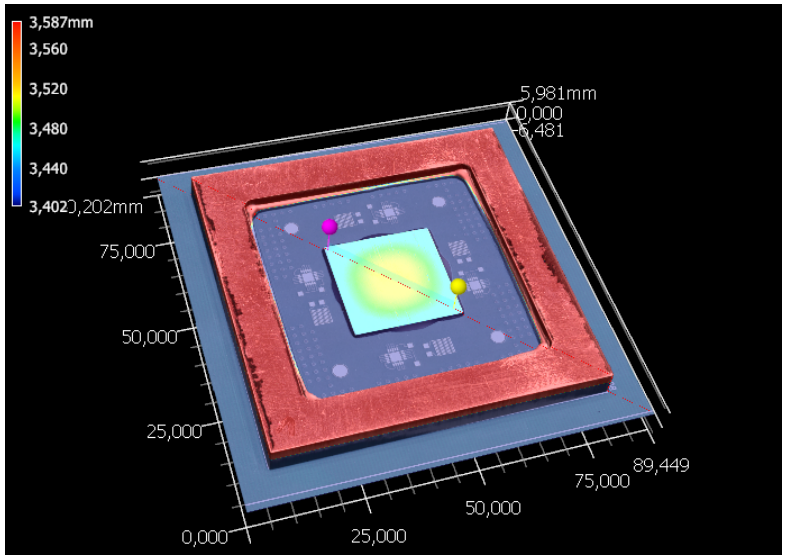


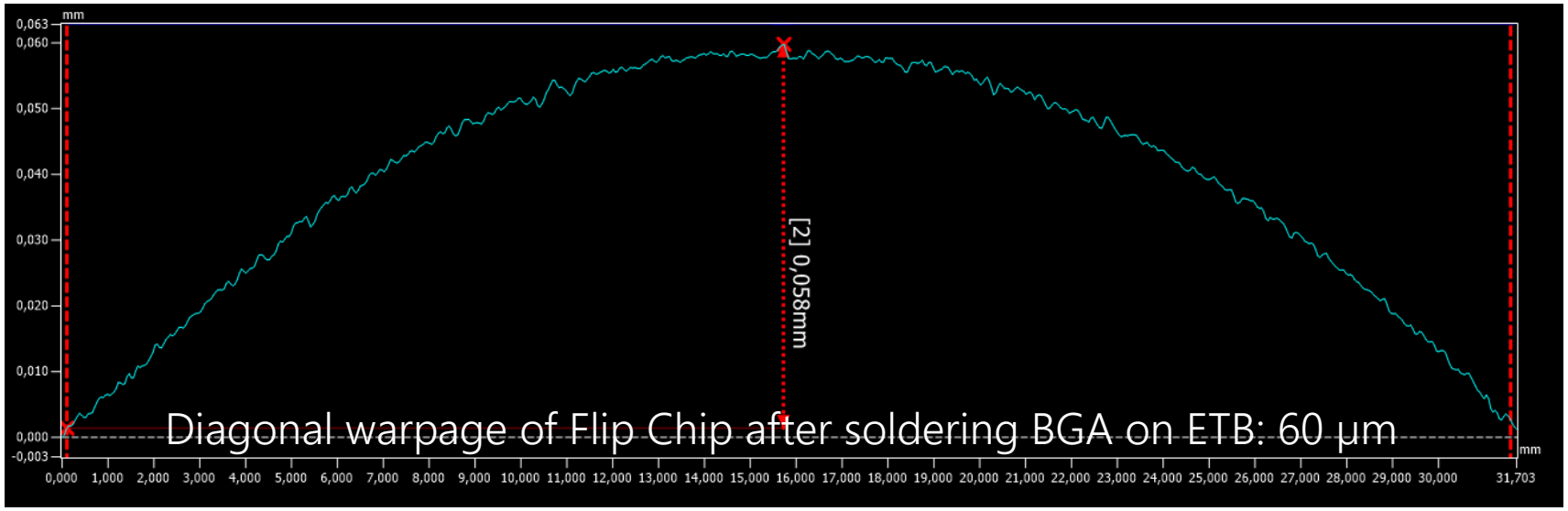


Stiffener ring does not influence a lot the chip warpage but it reduce the substrate warpage

Warpage after BGA assembly on ETB (with stiffener ring)

Die size: 25mm x 25mm, package size: 75mm 75mm. With stiffener ring and after ETB assembly



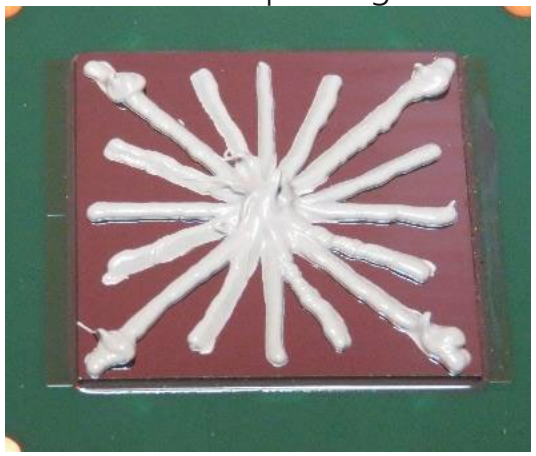


Chip warpage has been reduced from 120 µm to 60 µm after TTV assembly on ETB (BGA w/o underfill)

TIM Characterization & Aging investigation

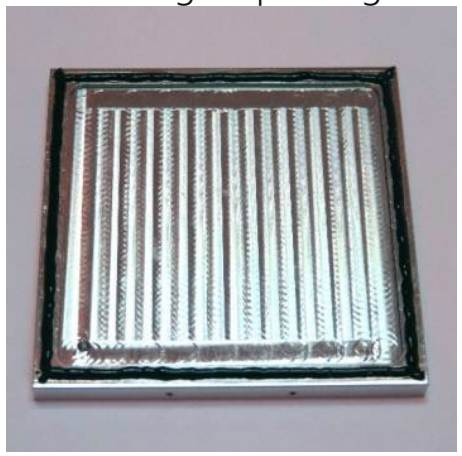
LID Assembly

TIM Dispensing

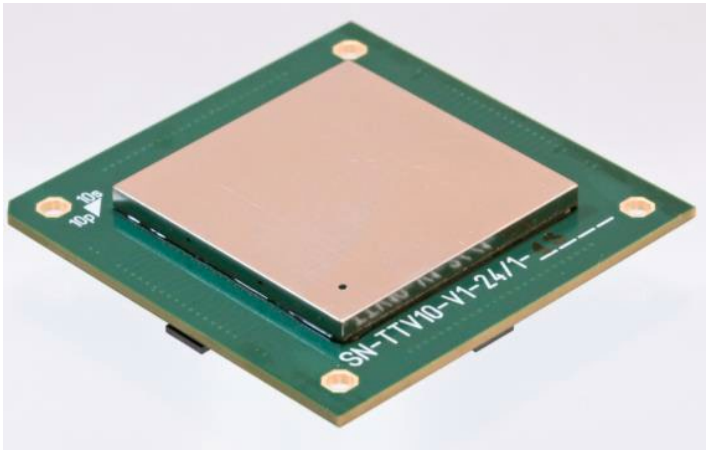


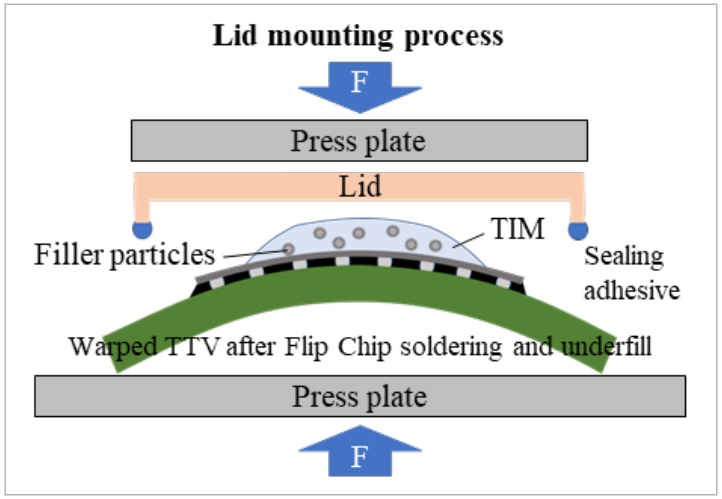
TIM pressed onto die with glass plate (quick volume check)

Sealing Dispensing

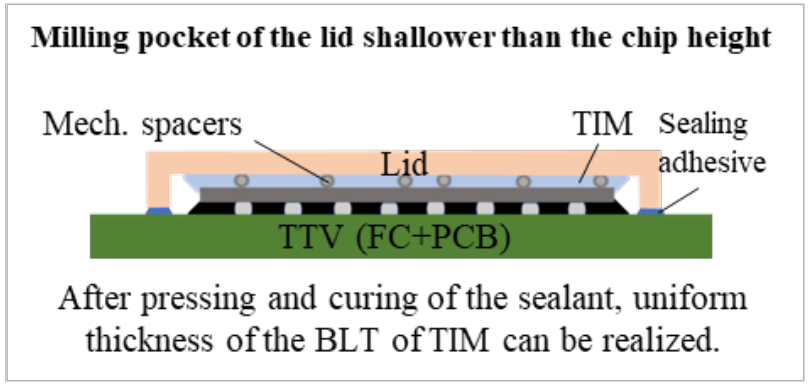


Lidded TTV

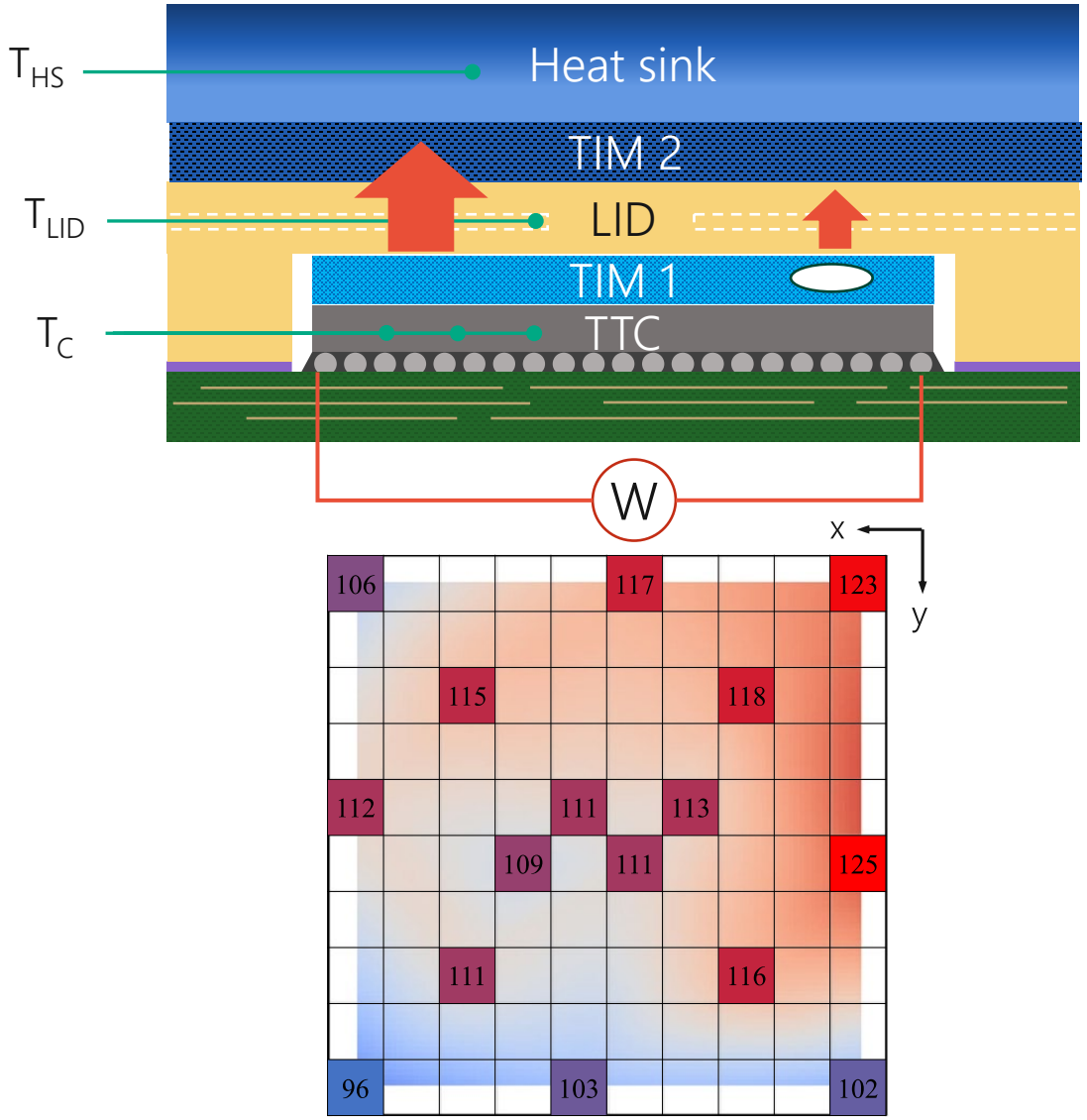




high quality and uniformity of a thin layer of TIM can be achieved if the LID pocket fits to the chip height



Thermal Steady State Testing



$$R_{th,total} = \frac{T_C - THS}{P}$$

$$R_{th,TIM1} = \frac{T_C - TLID}{P}$$

$$R_{th,TIM2} = \frac{T_{LID} - THS}{P}$$

$$R_{th,die} = \frac{\Delta\bar{T}}{P} = 0.144\ \frac{K}{W}$$

$$R_{th}(x,y) = \frac{\Delta T}{P_{cell}}$$

$$R_{th,min} = 12\,\frac{K}{W}$$

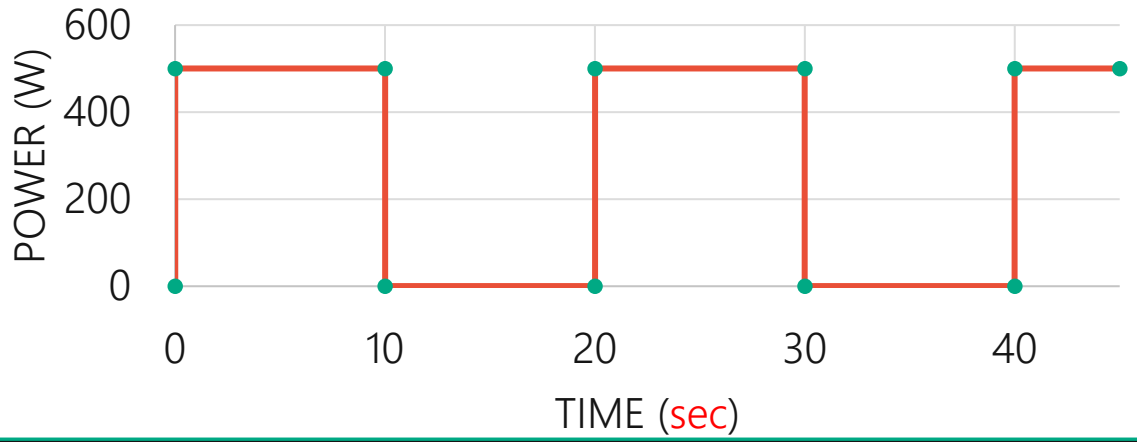
$$R_{th,max} = 16.5\,\frac{K}{W}$$

- Steady State Testing is **simple way** for:
  - Determination of maximal power P=f(T)
  - Investigation of cooling performance
  - Investigation of TIM performance
  - Determination of thermal resistance

Active cycle test vs. passive cycle test

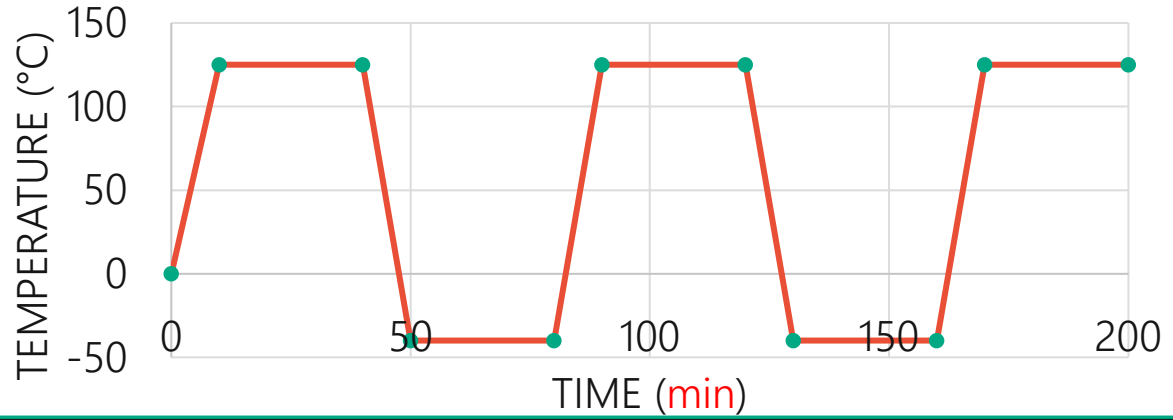
Active cycle test

- Package is powered and operational. Power cycling (turning the system on/off)
- Testing electrical, thermal and thermomechanical performance under real operating conditions
- In-situ (real time) degradation monitoring
  - Validate functionality and performance
  - Test reliability under dynamic loads
  - Identify hotspots or weak points

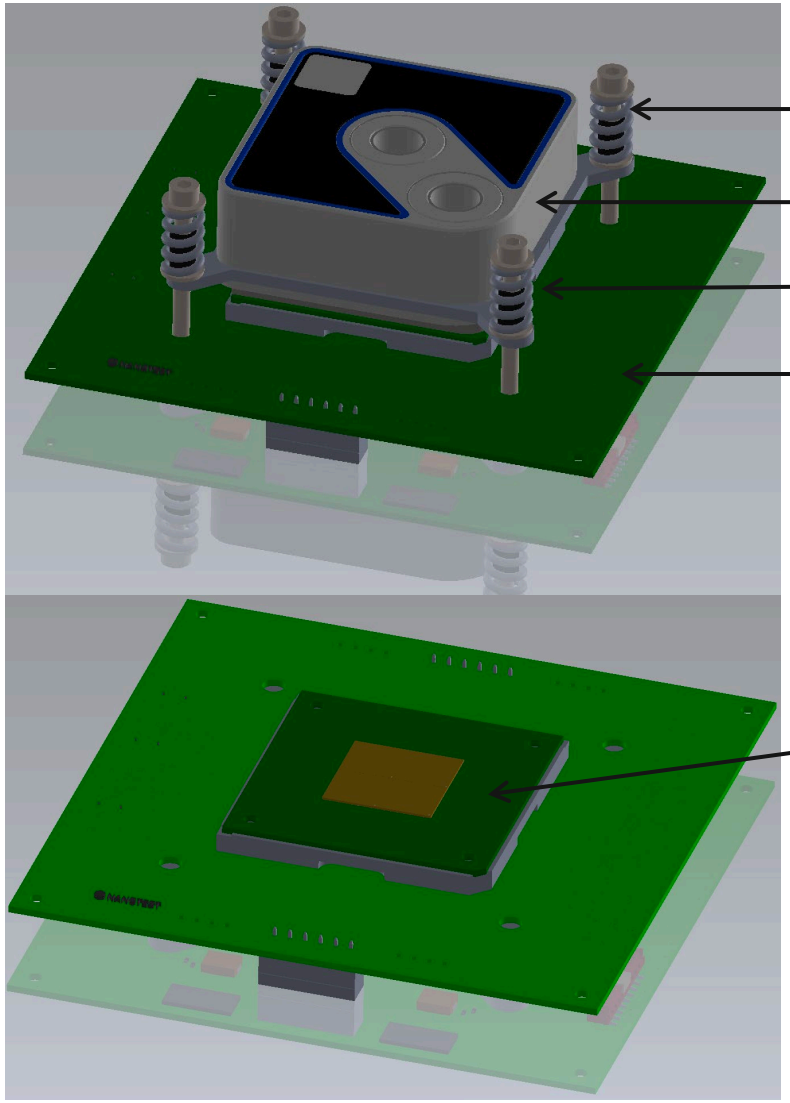


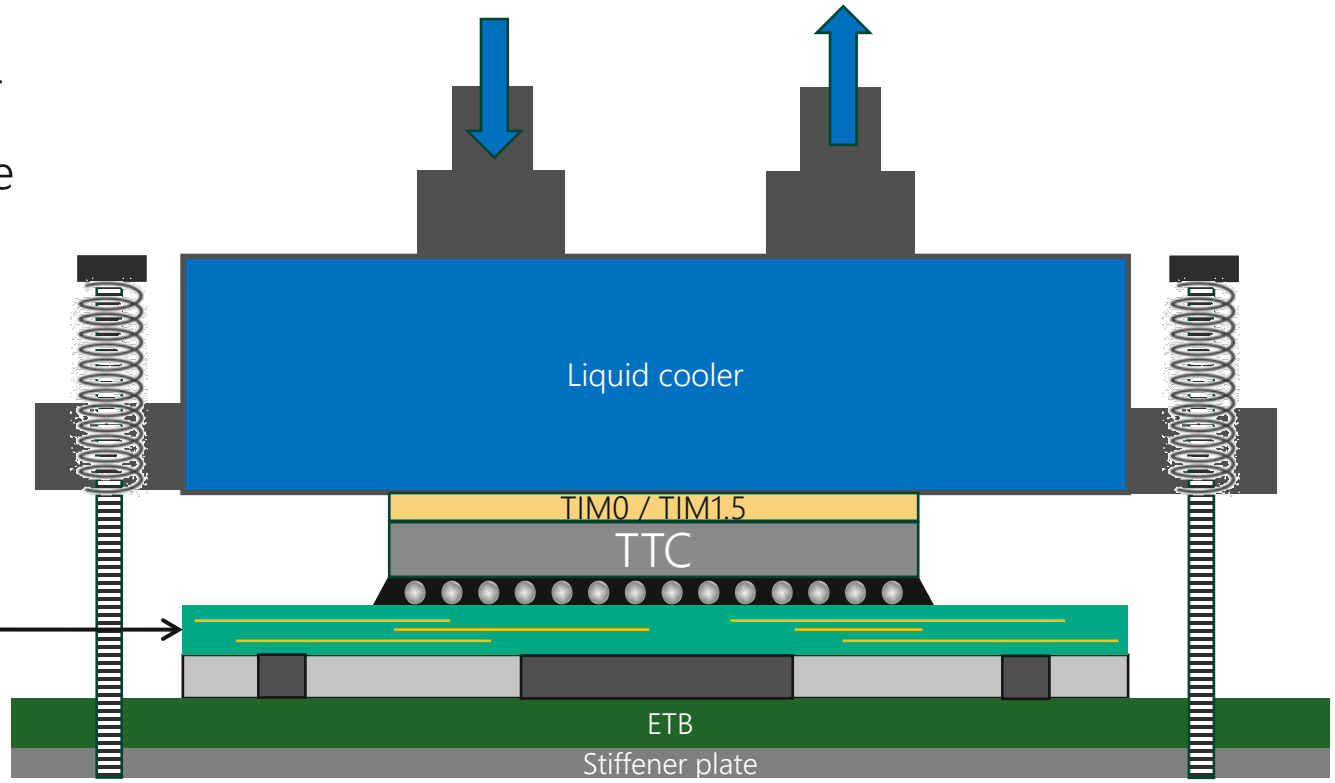
Passive cycle test

- No active power supply involved Temperature cycling tests (-55°C - +150°C) or (-40°C - +125°C)
- Testing of mechanical and thermal stability of the package
- Ex-situ degradation test (often destructive)
  - Evaluate structural integrity
  - Analyse solder joints, substrates, and package housing
  - Long-term reliability under extreme conditions

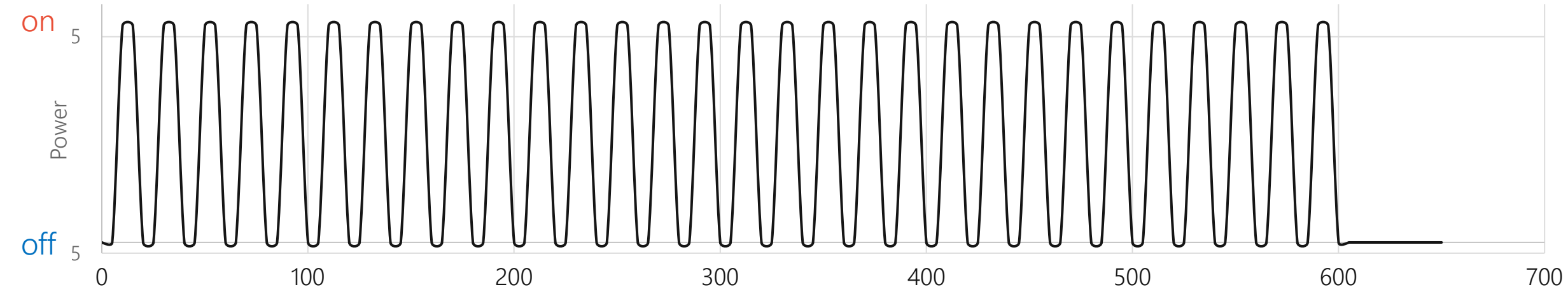


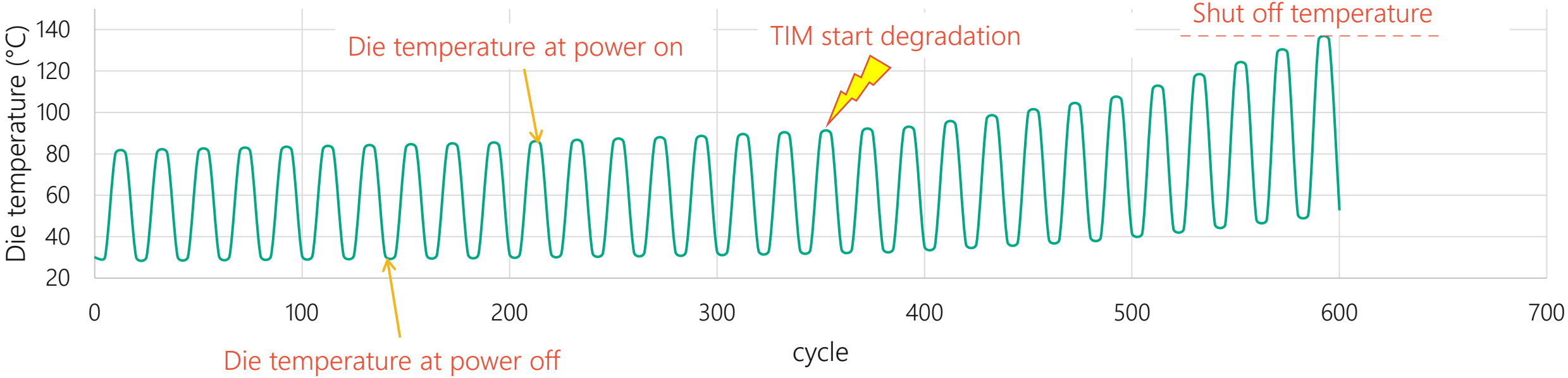
Test setup for active cycle test of TIM using TTV



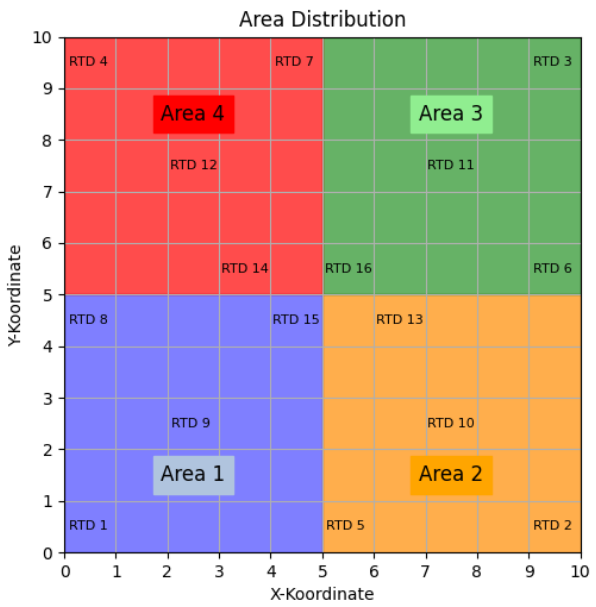


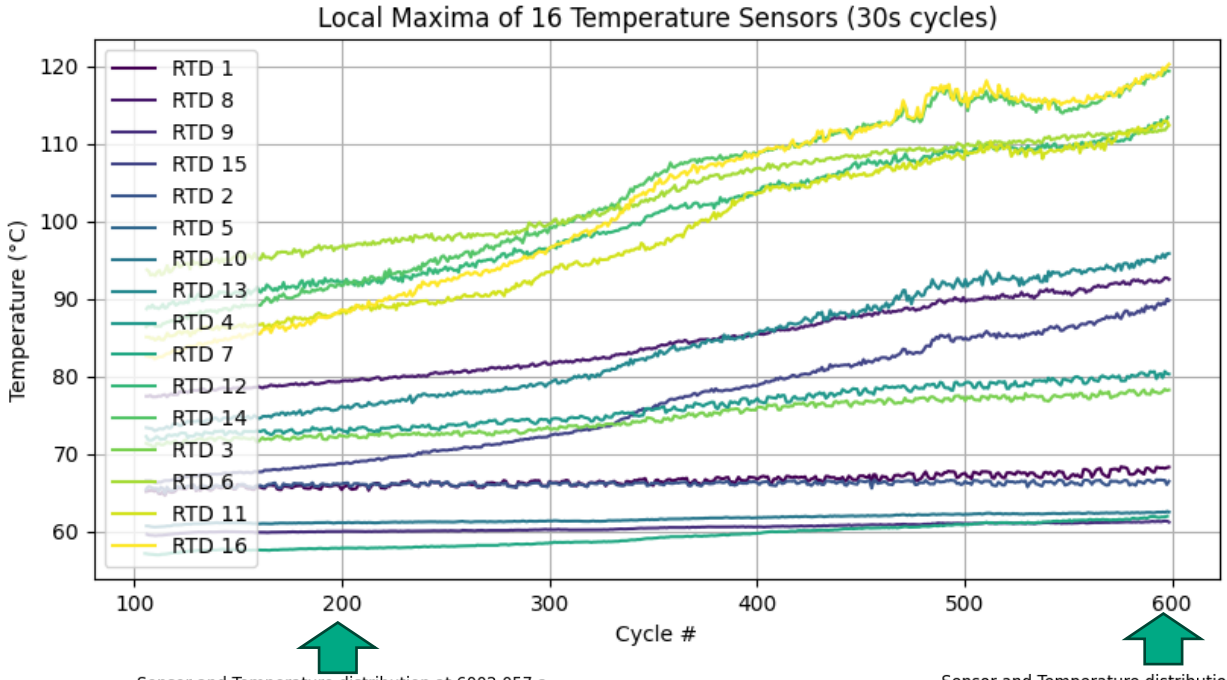
Active thermal cycle (schematics results)

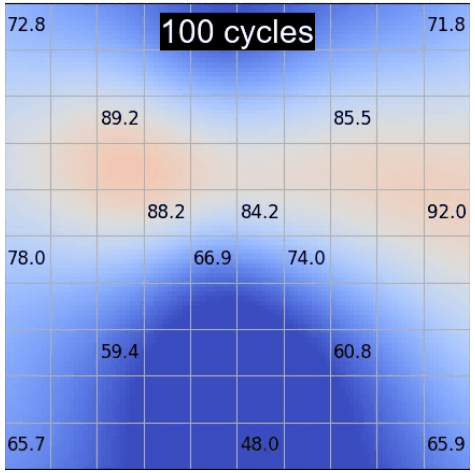


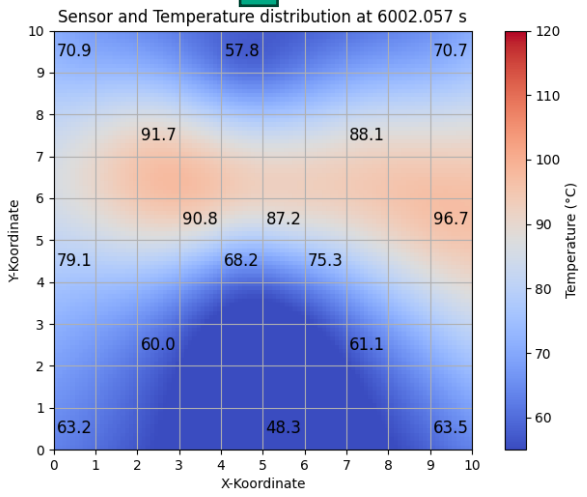


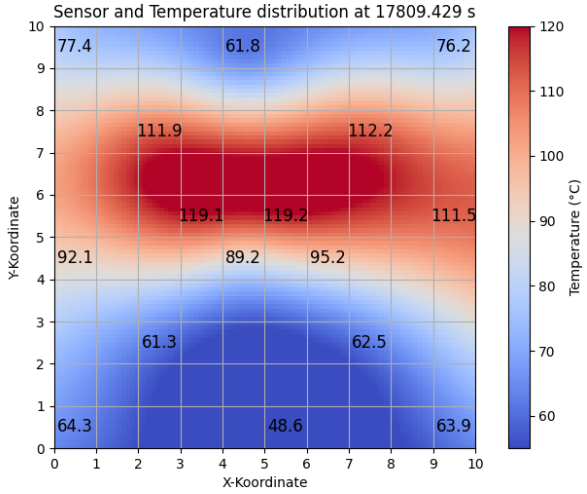
Active thermal cycle (results)



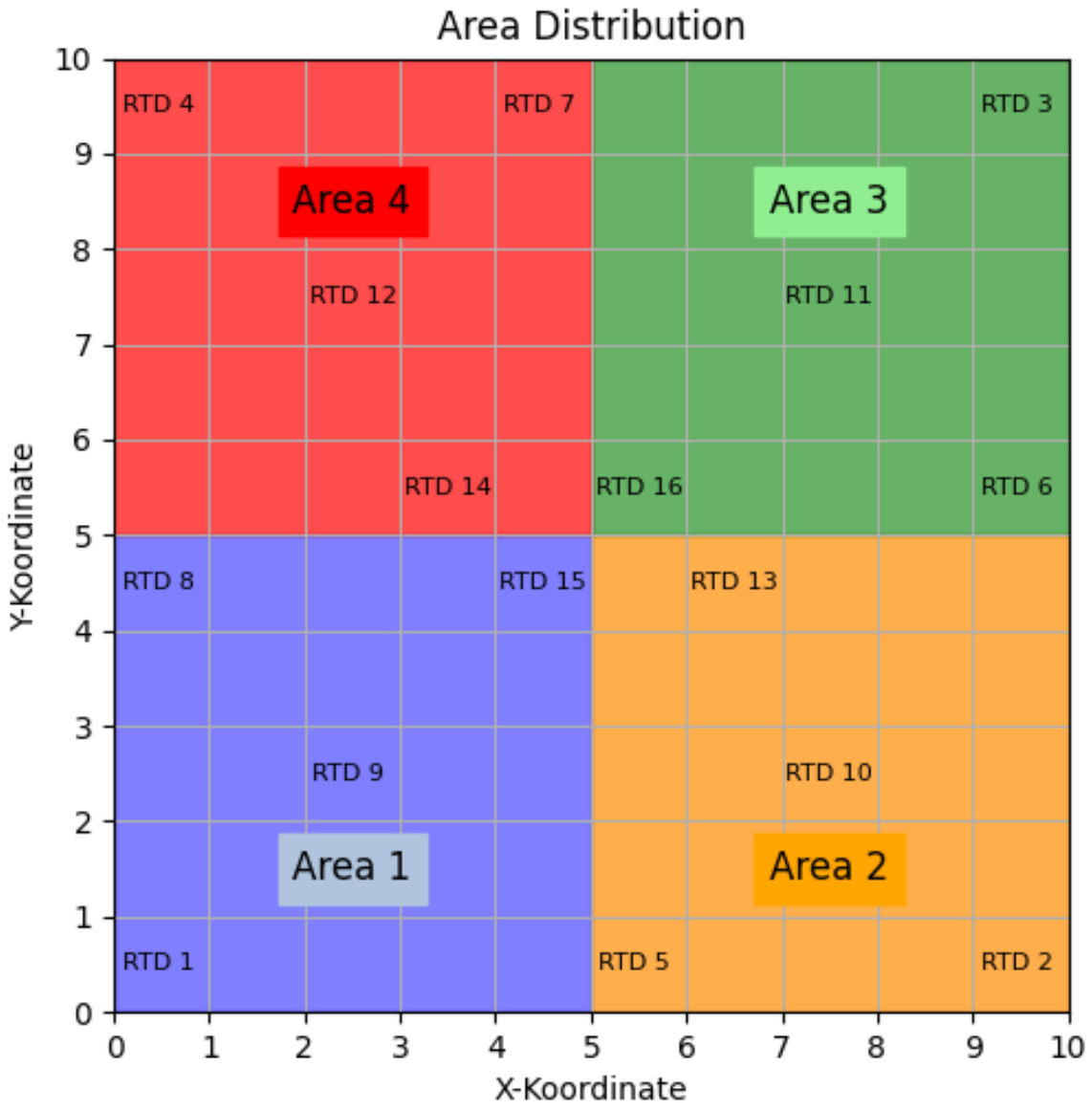


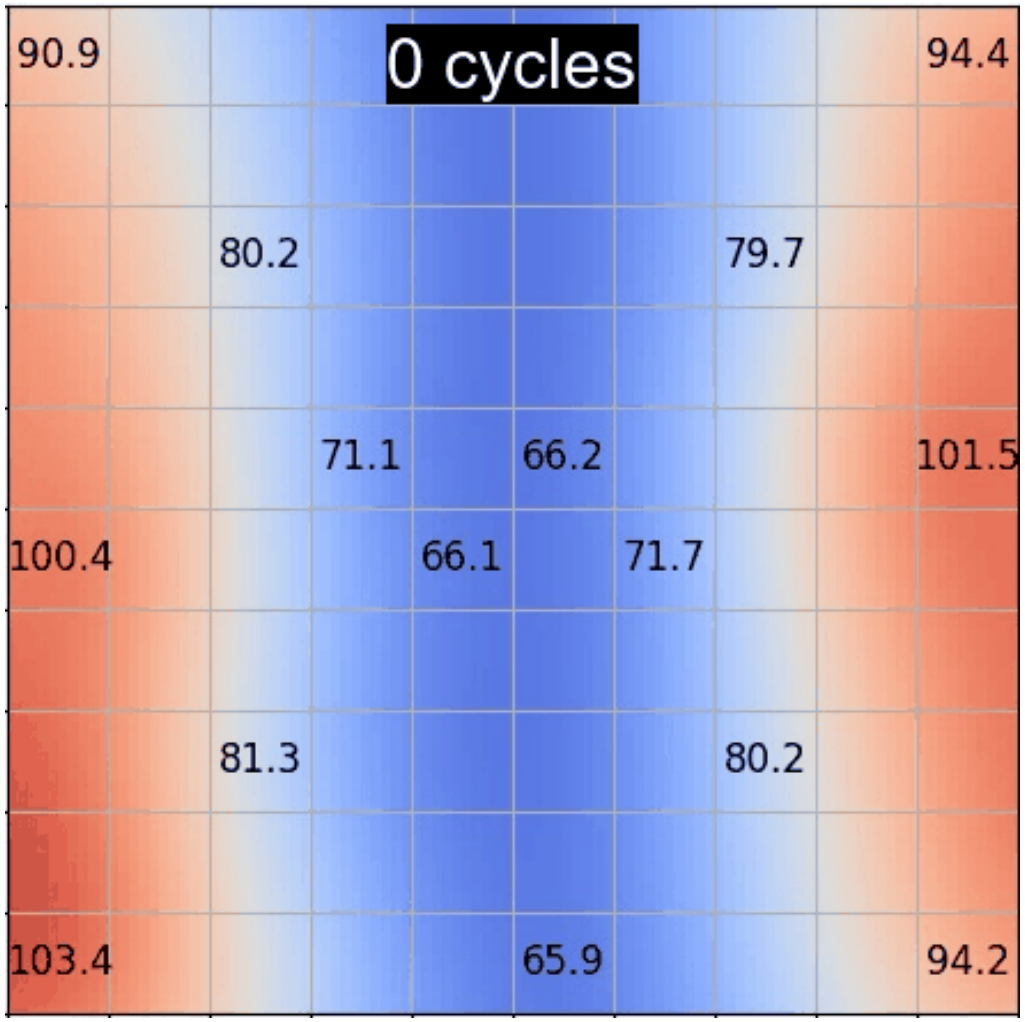






GIF 1000 cycles (40 s cycles 30-100 °C) – Worsening and Self Curing





Conclusion

- Thermal Test Vehicle serves as a valuable tool for investigation of advanced packages (e.g. HPC applications), their TIMs, cooling solution or reliability.
- The interposer of the future is an organic interposer
  - → Chip warpage is an issue → low CET substrate materials are required
  - → High stress on bumps → chiplet
  - → Chip cooling is a big challenge due to warpage → new cooling innovations are needed (e.g. LID-less or flexible LID)
- TIM is the bottleneck of thermal path.
- Initial thermal performance of the TIM is only half of the story
- Long-term stability of the TIM is much more important, as the TIM is exposed to enormous loads.
- Long-term stability of TIMs can be tested by active or passive cycle test.
- Active cycle test using TTV is the method of choice for “real world” TIM investigation

Thank you for you attention!

Any Questions?

NANOTEST
simply measured

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