Design for Reliability from Foundry perspective

February, 14th 2025

Design for Reliability from Foundry perspective

- Brief introduction of GLOBALFOUNDRIES
- Overview to support areas for Design by Foundry
- Examples of Design for Reliability support and health monitor

GF's ecosystem: more than a decade in the making

Design enablement network

IP	FDX™	RF	EDA	Design services	OSAT

Our partner community

100+
Ecosystem partners spanning IP, EDA, OSAT and design services

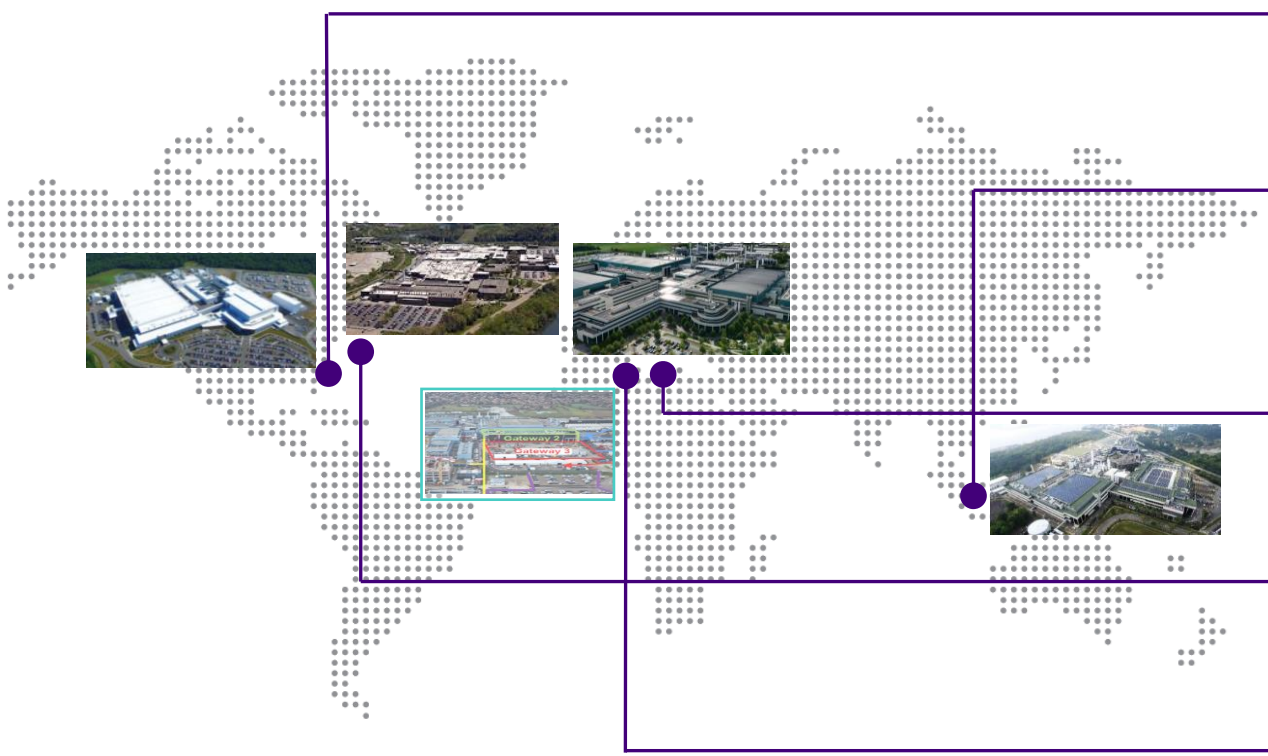
4500+
Total IP titles across all nodes from >50 IP partners

950+
IP titles currently in active development across 26 process nodes and 34 IP partners

300+
Clients enabled by ecosystem partner IPs in the last 5 years

1700+
Client designs enabled by ecosystem partners in the last 5 years

Resilient global manufacturing footprint

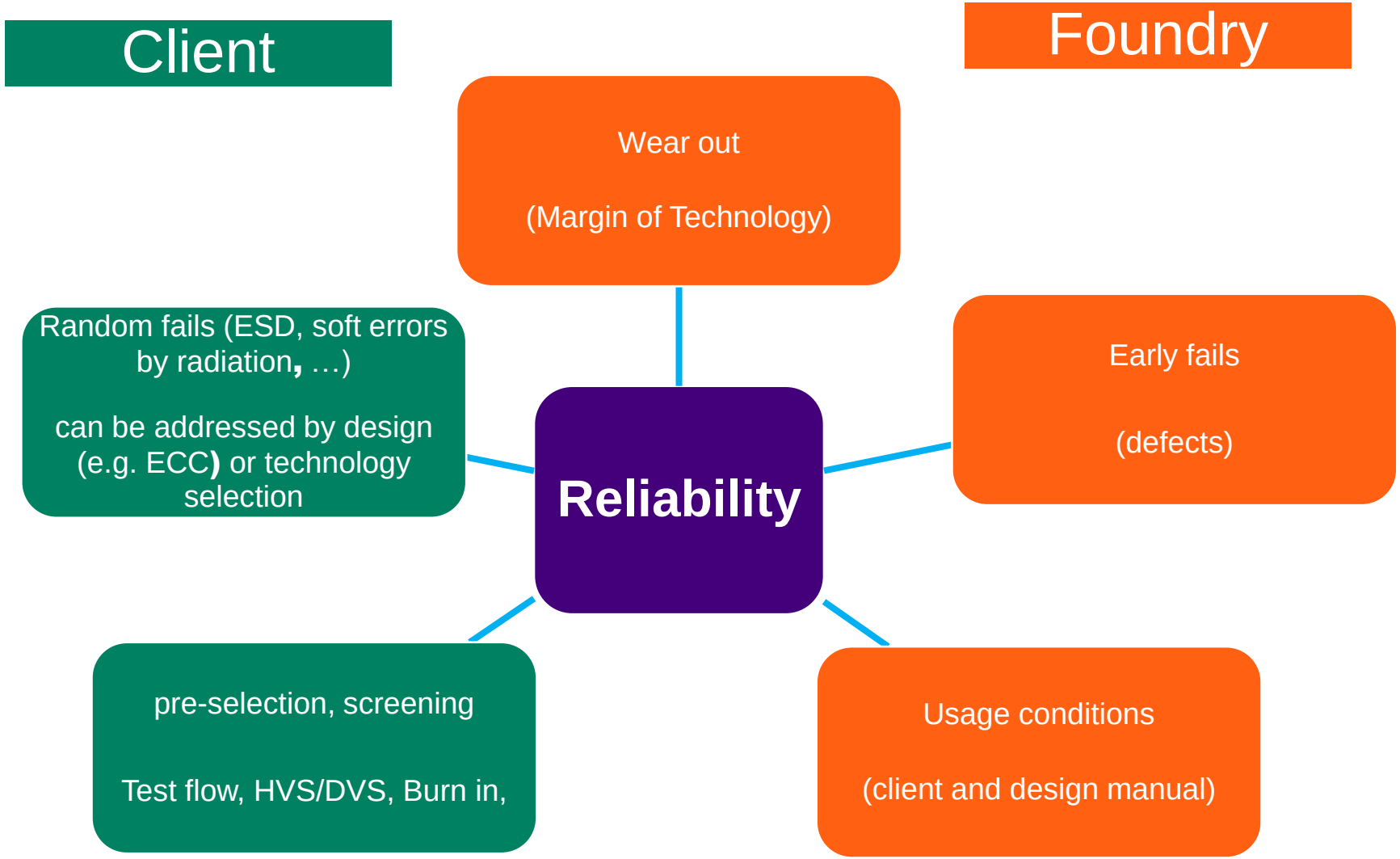


Malta, NY, USA *300mm*	**Capacity:** 404 kwpa **Technology:** FinFET, NVM, RFSOI, SiPh
Singapore *300mm & 200mm*	**Capacity:** 790 (300mm) & 361 (200mm) kwpa **Technology:** BCD/BCDLite, HV, NVM, DDI, RFSOI, LP SiGe
Dresden, Germany *300mm*	**Capacity:** 800 kwpa **Technology:** FDX™, NVM, HV, BCDLite
Burlington, VT, USA *200mm*	**Capacity:** 263 kwpa **Technology:** RFSOI, SiGe, GaN
Crolles, France	Under Construction

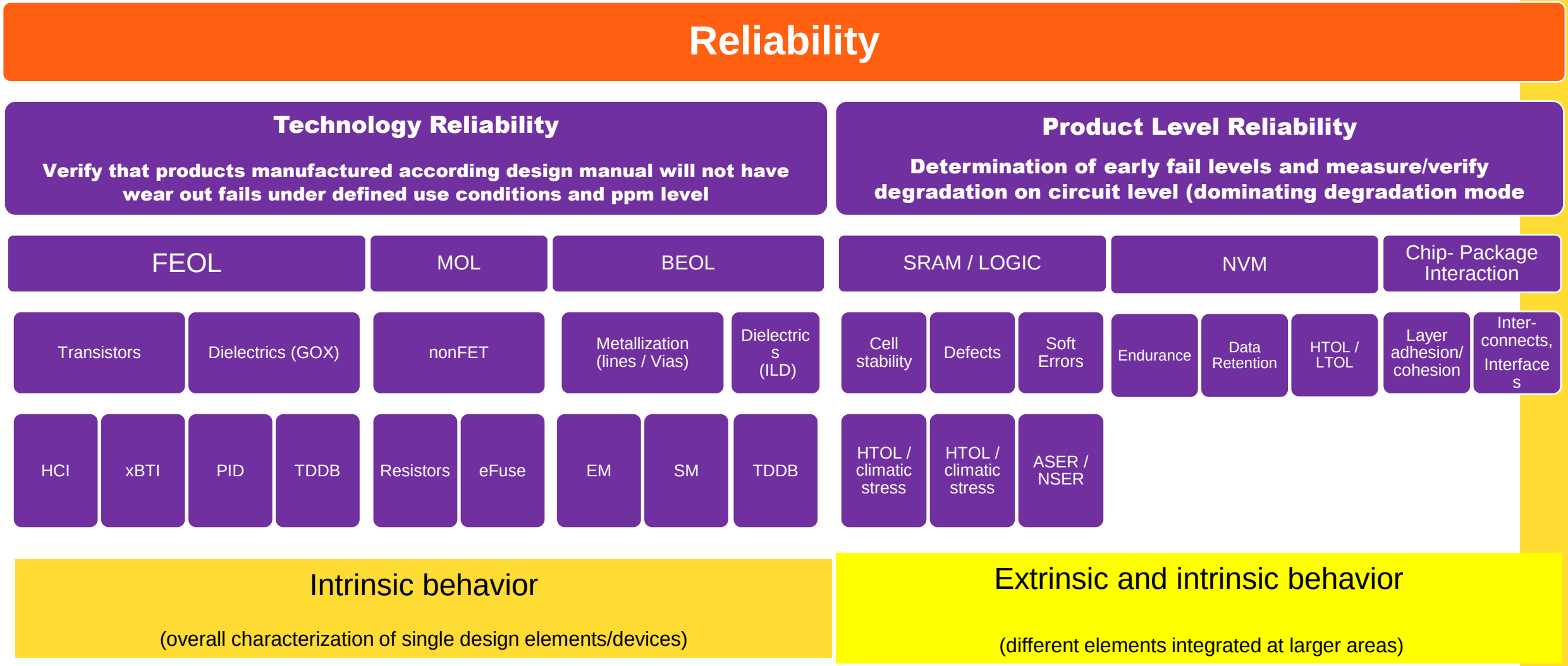
Products on the differentiated technology platforms our customers need where they want them produced

Note:
1. Kwpa is defined as installed capacity in thousand wafers per annum as of 12/31/23
2. 200mm capacity translated to 300mm equivalent

What defines Reliability?



Landscape of GF Reliability Assessments



Products and support from Reliability

- **GLOBALFOUNDRIES products are technology offerings and turnkey services**
- GLOBALFOUNDRIES does not own dedicated products, but has experts in all areas to support client product designs
- Reliability team supports clients in achieving good reliability

Design for Reliability from Foundry perspective

Design support	Screening options	IP's
• P-CELLs (e.g. Crack stop) ★ • Reliability calculators ★ • Safe Operating Area assessments (SOA) • Reviews and recommendations for specific items (e.g. short length effect in EM, Waveform analysis)	• Recommendations for design corners to enable screening e.g. • white paper for test coverage and screening • Recommendation for max. DVS Voltage ★	• Delivery of own verified IP's • Work together with 3rd party IP suppliers

★ Examples in the next slides

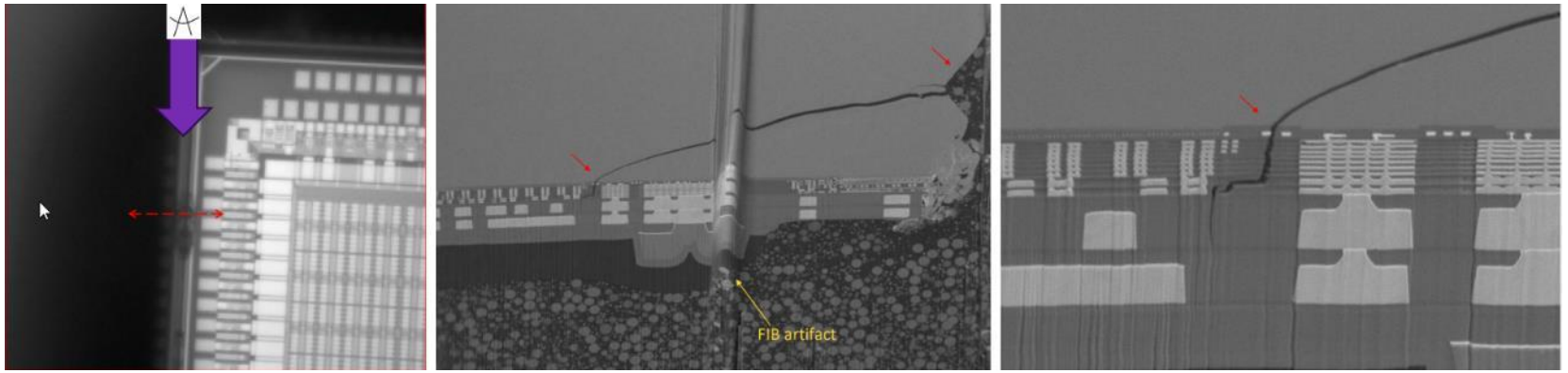
Examples for "Design for Reliability" design support

1. Pcell for crack stop with Perimeter Line
2. Reliability calculators
3. Max. Voltage definition for High Voltage Screening (HVS)

PCELL with Perimeter Line

- Assembly fails are one of the main detractors in customer fail pareto
  - Such fails can be caused by mechanical pre-damage at die edge
  - In case no electrical traces are damaged the test coverage is for those defects is poor
    - ➔ The crack can continue to grow by mechanical stress
    - ➔ Humidity can penetrate and cause opens/leakages (for porous ILD materials also TDDB performance will significantly drop)

Mechanical damage in GF test chip found in Humidity Stress (uHAST)



Infrared microscope image

Cross section by FIB cut

Assembly damage + Test coverage escape

Humidity stress test (uHAST 96hrs)
Caused single via resistance increase

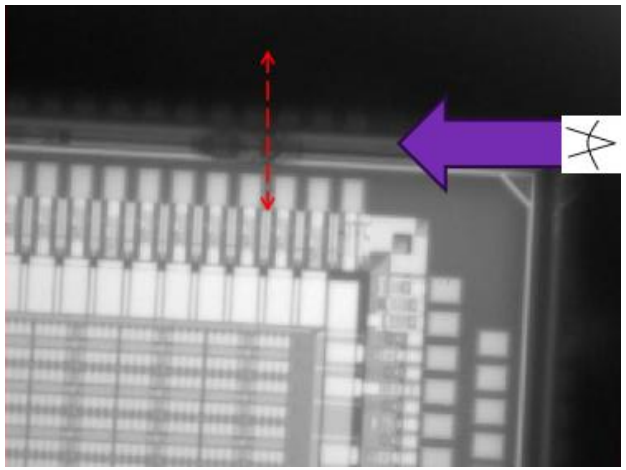
Improved test coverage + health monitor could reduce fail probability

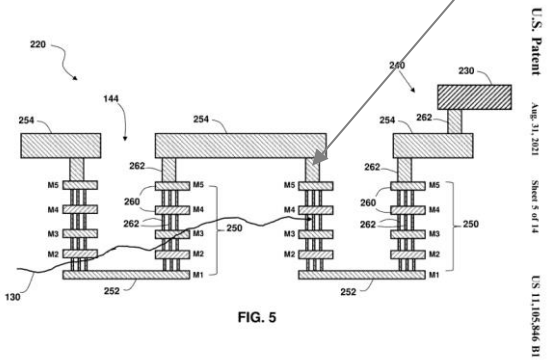
Example for simple health monitor + better test coverage

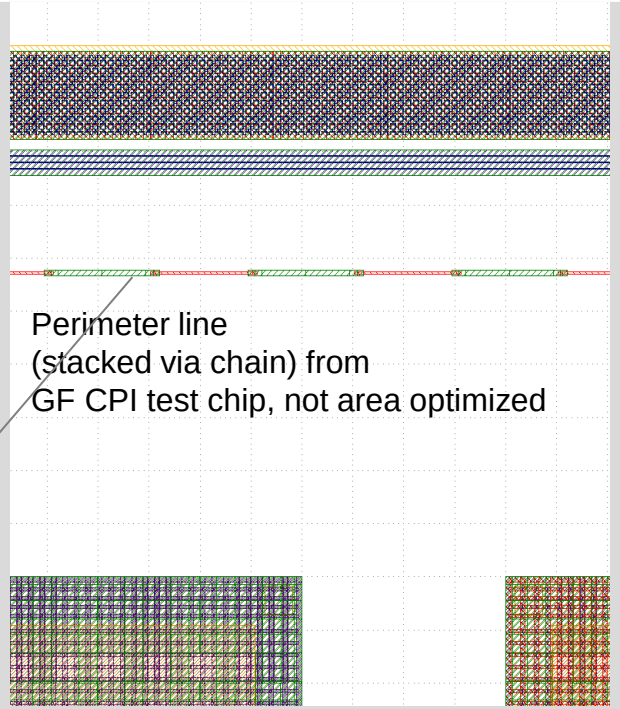
- Die perimeter has mechanical and humidity protection
- Typical this element is only passive
- In test chips for Chip Package Interaction (CPI) a structure is used to indicate cracks at die perimeter during stress (perimeter line) see also JEP156
- An integration of such feature into Crack stop can improve test coverage and used as health monitor for die integrity

Crack stop

Guard ring





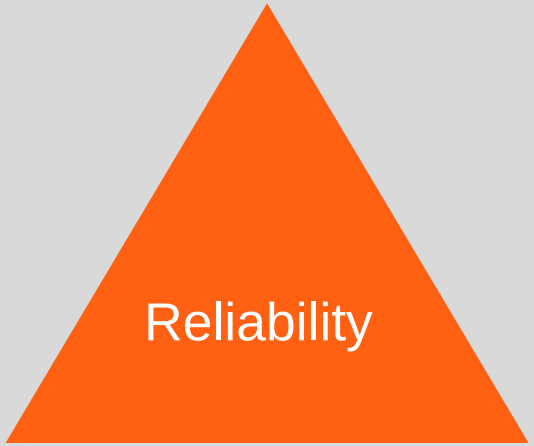


For 22FDX Products GLOBALFOUNDRIES offer an area optimized PC cell option of perimeter line integrated into crack stop/die seal

US11105846B1
“Crack detecting and monitoring system for an integrated circuit”

Fine tuning of Designs for cost, performance reliability

- Design manual / PDK contains a framework for design



But what happens if client needs more voltage / higher temperatures for short period of time ?

What's the impact to gate oxides, xBTI degradation, ILD degradation ?

Examples for "Design for Reliability" design support

1. Pcell for crack stop with Perimeter Line
2. **Reliability calculators**
3. Max. Voltage definition for High Voltage Screening (HVS)

Reliability Calculators

- Reliability calculators are part of PDK (Product Design Kit) and offers for a specific design situation the calculation between Design, CDF (ppm) and use conditions.
- They are available for different failure modes (xBTI, HCI, BTS, EM*)

GlobalFoundries 22FDX BEOL BTS Calculator

Instructions

Fill in all tabs except one from 1-6 below.

Please click the Calculate buttton to update results

Input Parameters		Results of BTS calculation	
Product Group Target	Consumer Grade		
Metal/Via Level	M1	Metal/Via Level	M1
1. Spacing (microns)	0.040	Metal/Via Spacing (microns)	0.040
2. Runlength (microns) /# Vias	1.0E+08	Runlength at min spacing (microns)	1.00E+08
3. Maximum Operating Voltage (V)	1.320	Maximum Operating Voltage (V)	1.320
4. Junction Temperature (°C)	125	Tjunction (°C)	125
5. CDF (ppm)	1000	CDF (ppm)	1.0E+03
6. Circuit lifetime (years)		Lifetime (years)	Output (e.g. 2000 years)

Calculate | Set to defaults

* Values in red exceed technology specifications or violate design rules.

*EM adjustments are part of design manual and also supported in design release flow

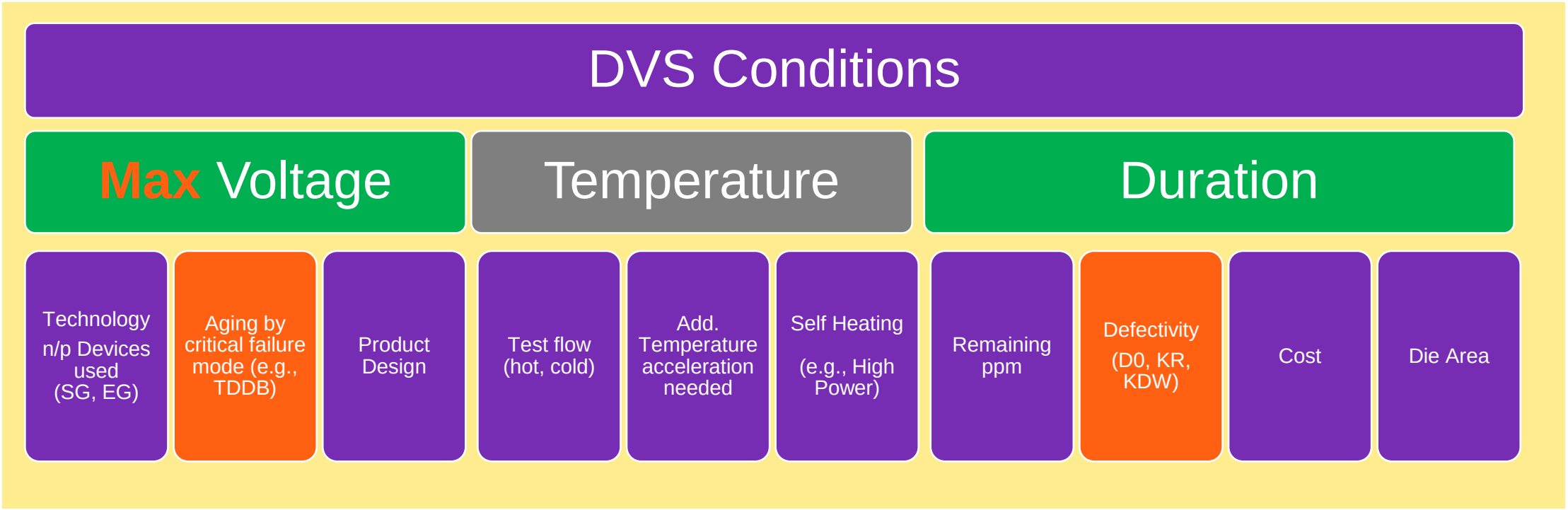
Examples for "Design for Reliability" design support

1. Pcell for crack stop with Perimeter Line
2. Reliability calculators
3. **Max. Voltage definition for High Voltage Screening (HVS)**

HVS Conditions influencing factors

Client definition

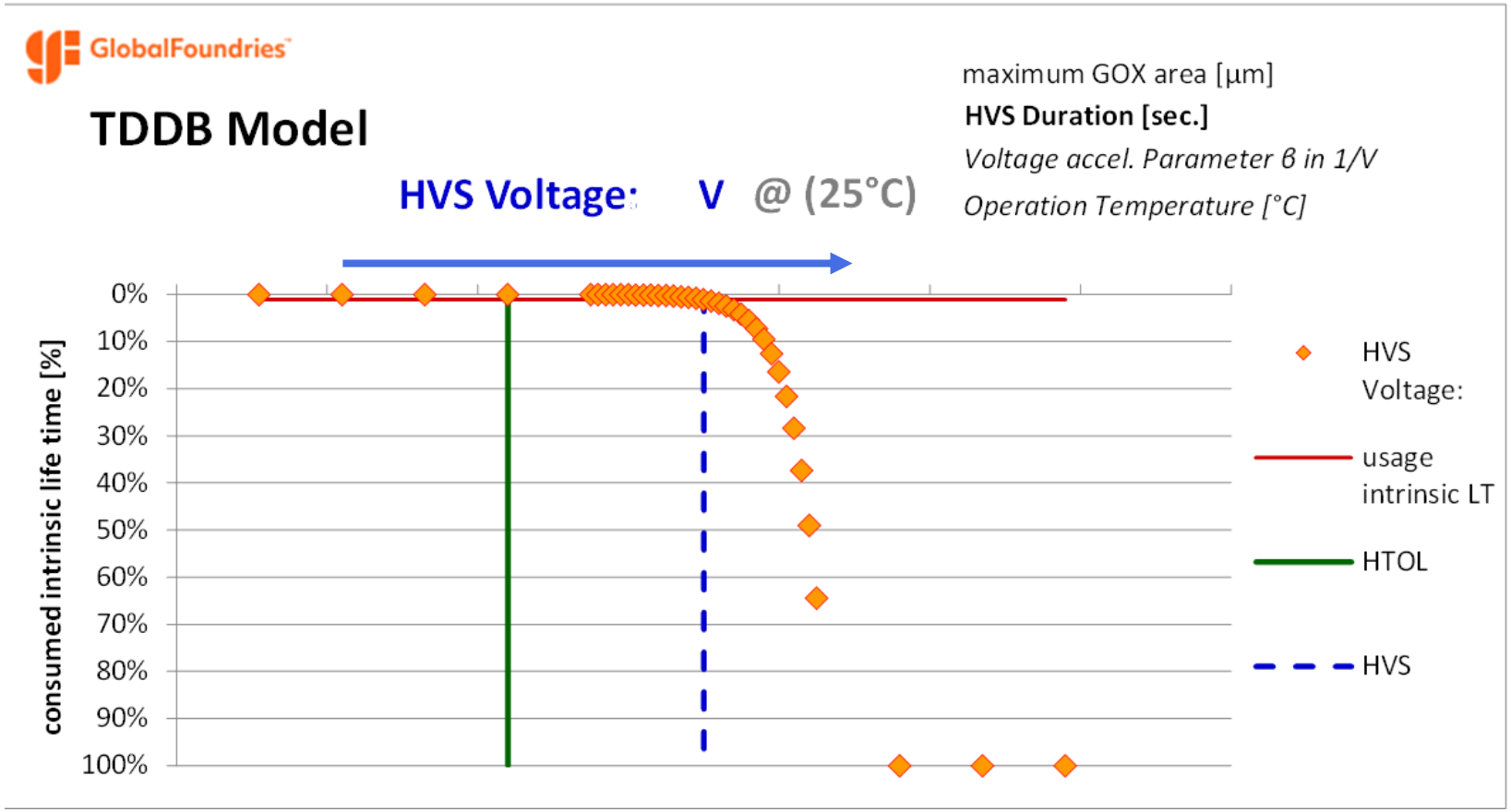
Foundry input



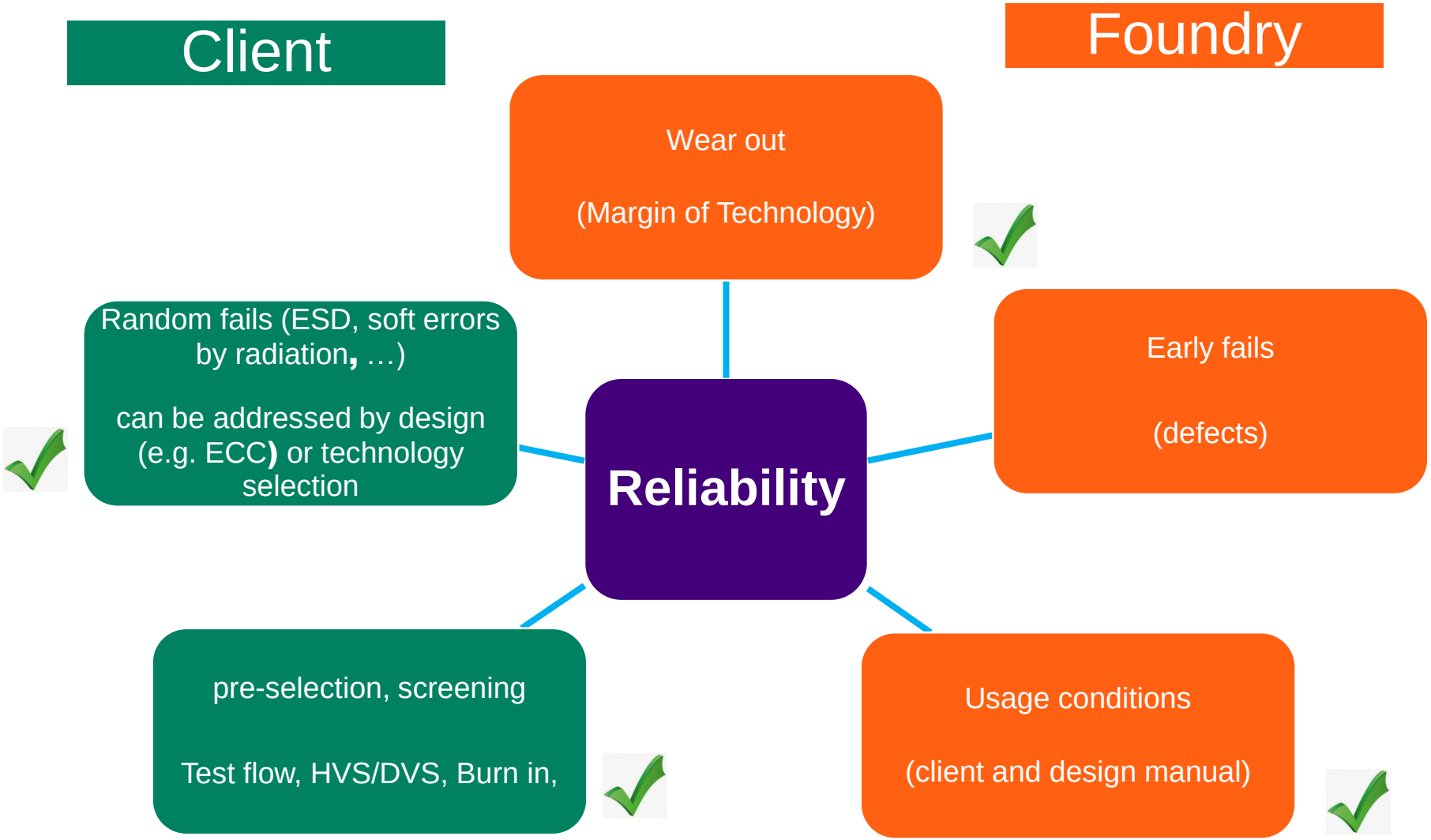
- Before design client need to have a screening strategy.
- Design should be reviewed if needed voltages for HTOL / HVS can be applied (no need to fulfill complete datasheet under those conditions, but nodes should toggle)
- Verification of HVS conditions by HTOL strongly recommended

Boundary of HVS

- **HVS Calculator**
  - GF uses as reference consumption of max. 1% of intrinsic lifetime for the most sensitive failure mode (e.g. nLV TDDB).
  - The determined voltage is the absolute maximum voltage recommended for screening (Digital).
  - If client can apply such a voltage depends on design (e.g. voltage regulators)



Summary


Client
Foundry
Wear out
(Margin of Technology)
Random fails (ESD, soft errors by radiation, …)
can be addressed by design (e.g. ECC) or technology selection
Reliability
Early fails
(defects)
pre-selection, screening
Test flow, HVS/DVS, Burn in,
Usage conditions
(client and design manual)

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Thank You