# Electrodeposition of Aluminum towards wafer level thermo compression bonding

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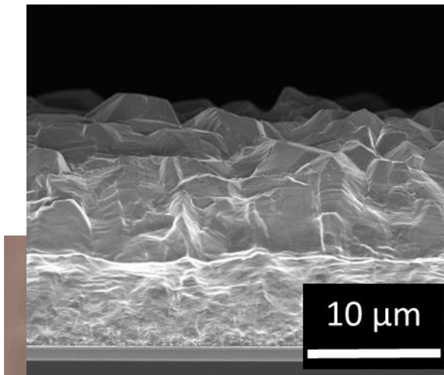
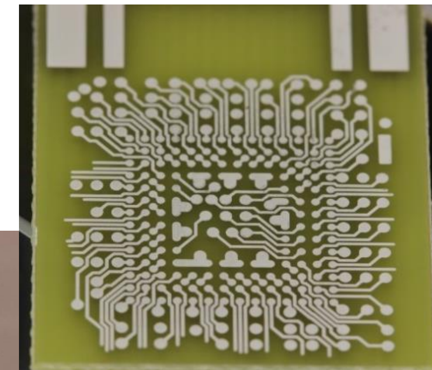
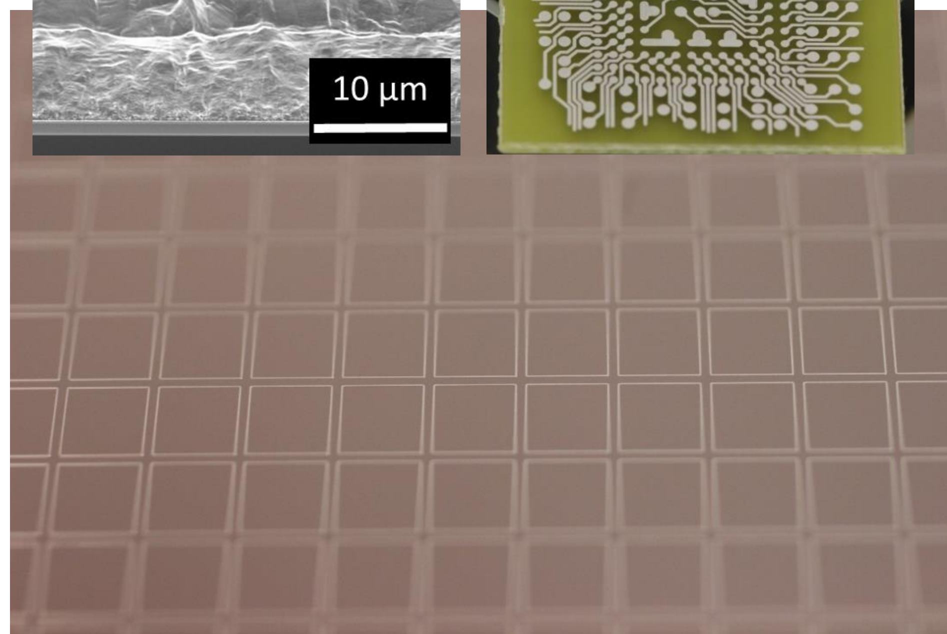
Chemnitzer Seminar 2019







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# Electrodeposition of Al: Why?

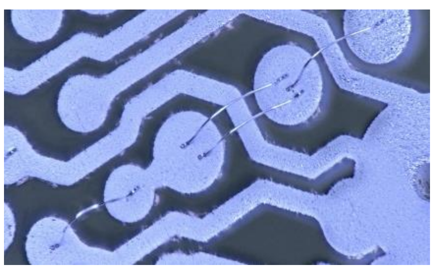
## Microsystem technology

- Al as conducting and connection material
- Al as bonding material → assembly and packaging
- Al and its anodized layer → medical applications, micro fluidics, micro reactors, insulated micro coils
- Al as optical material due to highly reflective character → micro optics

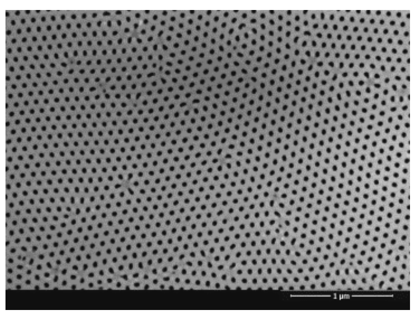
## Printed circuit board

- Cu as metal for numerous of applications
  - Electricity net (buried cables)
  - Electrode material in Li-Ion batteries
  - PCBs
  - ⇒ Supply bottlenecks for PCB industry

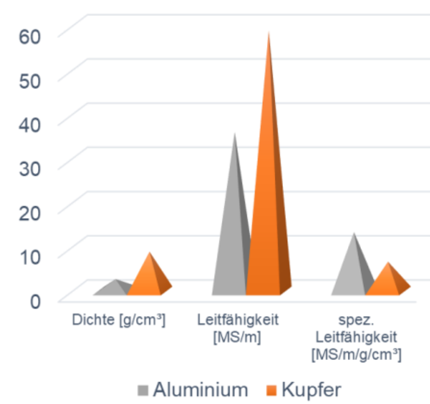
⇒ Al as alternative material due to higher specific conductivity and availability



Al wire bonds on ECD-Al




anodized ECD-Al (ECD @ENAS, Oxidation @ Smart Membranes


source: www.ariva.de

# Electrodeposition of Al: Why?

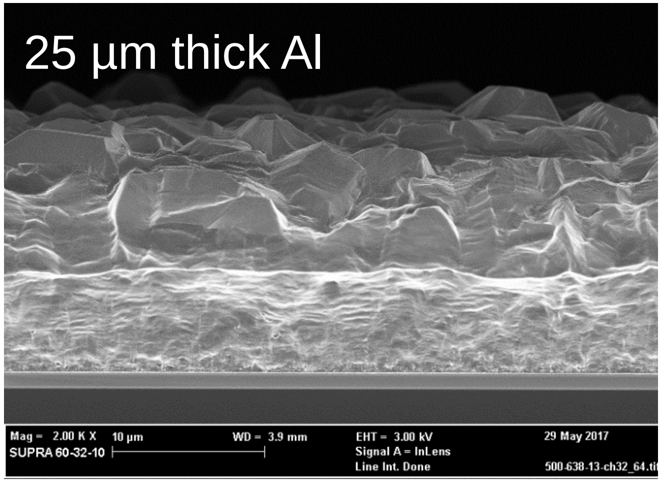
## Al-Al Thermo compression bonding

**State of the Art**

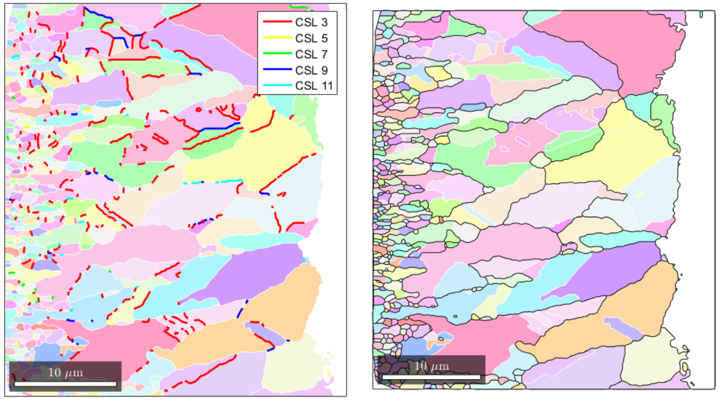
- High temperatures and bond pressures needed
- Diffusion is inhibited because of native oxide layer
- Removal of Al oxide prior to bonding not possible (except of in situ plasma treatment)
- Use of thin PVD layers → compression is limited

**Why could electroplated Al overcome some current challenges?**

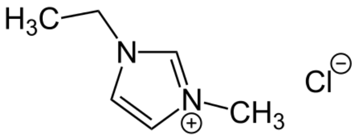
- Grains in as-deposited Al layers are thermally active
- ECD-Al shows higher roughness than PVD-Al → cracking of Al oxide layer
- Al as well-malleable material → thicker Al layer as intermediate bonding material can improve the thermo-compression bonding process
- No specific grain orientation




Grains merged, if sharing at least two Σ3 boundaries



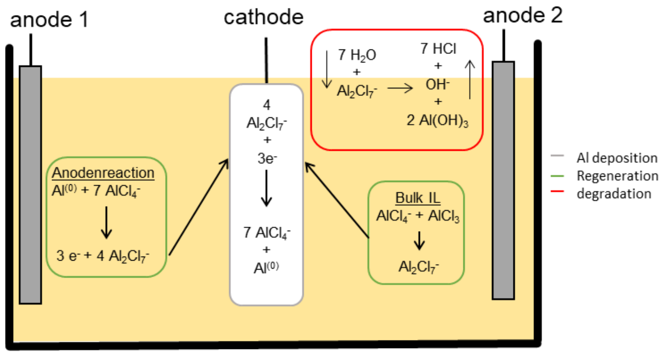
# Electrodeposition of Al: How to?



Chemical structure

- $E^0_{Al}$= -1,67 V vs. NHE → deposition from aqueous solutions is not possible

  → ionic liquids (Ils) are used
- ILs= organic salts with a melting temperature < 100 °C
  - Properties are tunable by varying the composition
  - Wide electrochemical window
- Use of EMImCl/$AlCl_3$ 1:1,5 (~150 g/l Al)
- Moisture sensitivity of IL requires inert gas atmosphere




ECD process for double-side deposition and reaction equations

Glovebox with $N_2$ atmosphere

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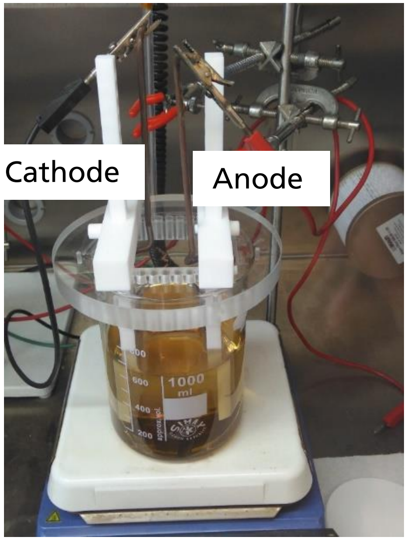
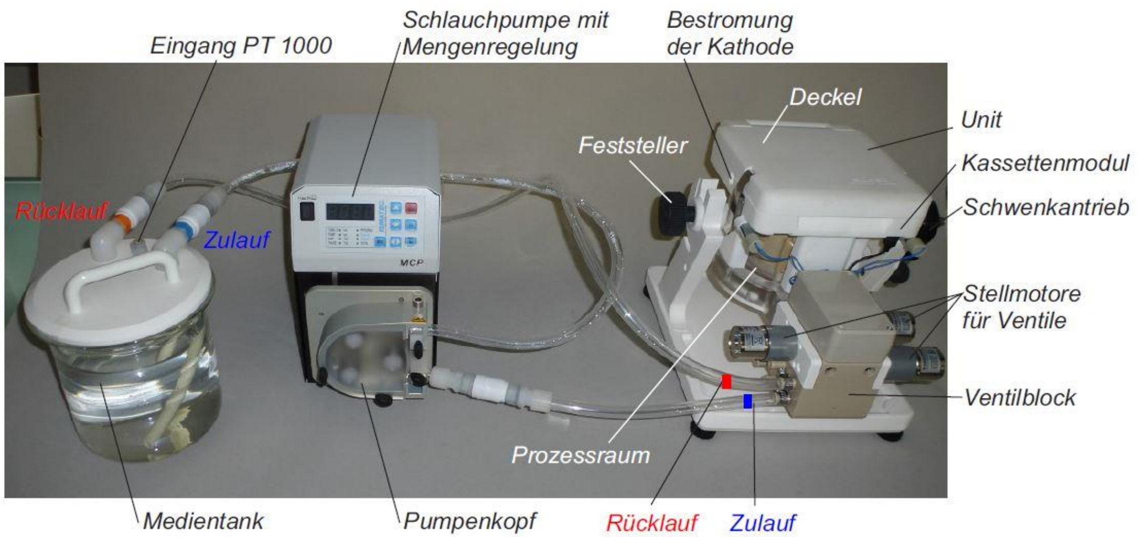
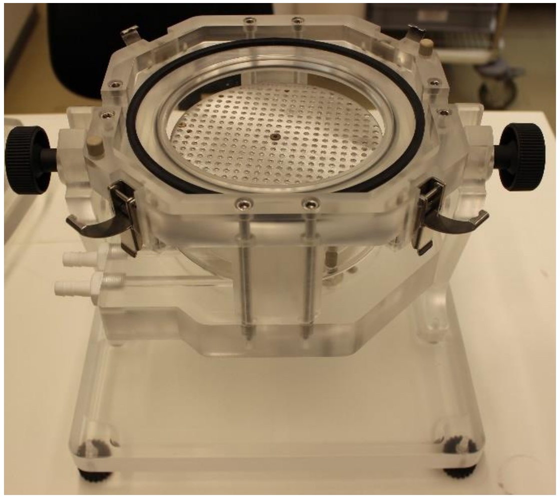
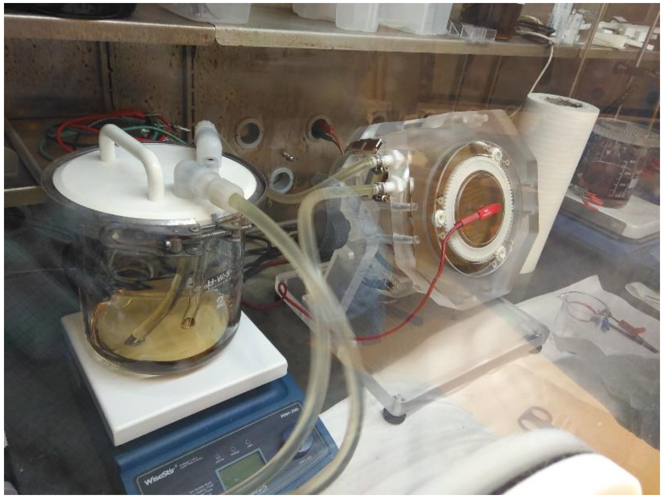
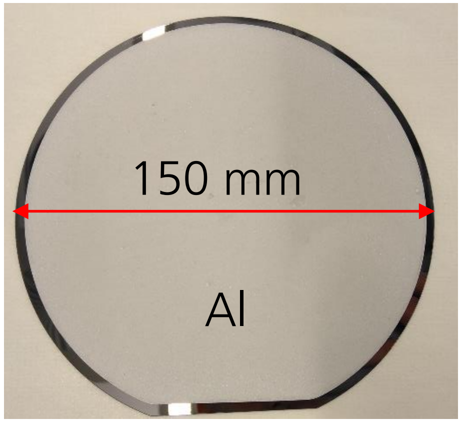
# Electrodeposition of Al: Process equipment











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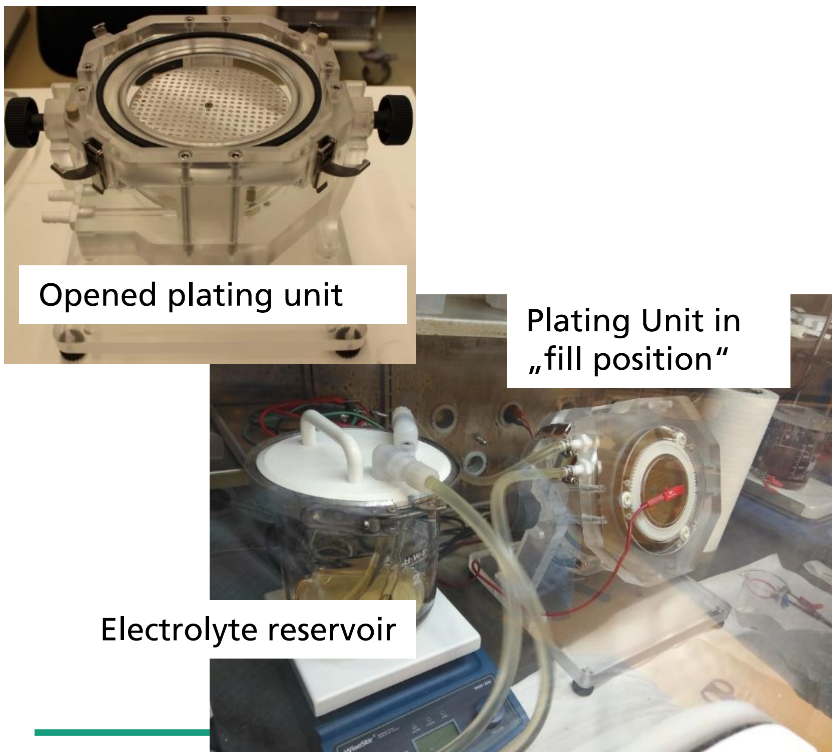
# Electrodeposition of Al: Process equipment

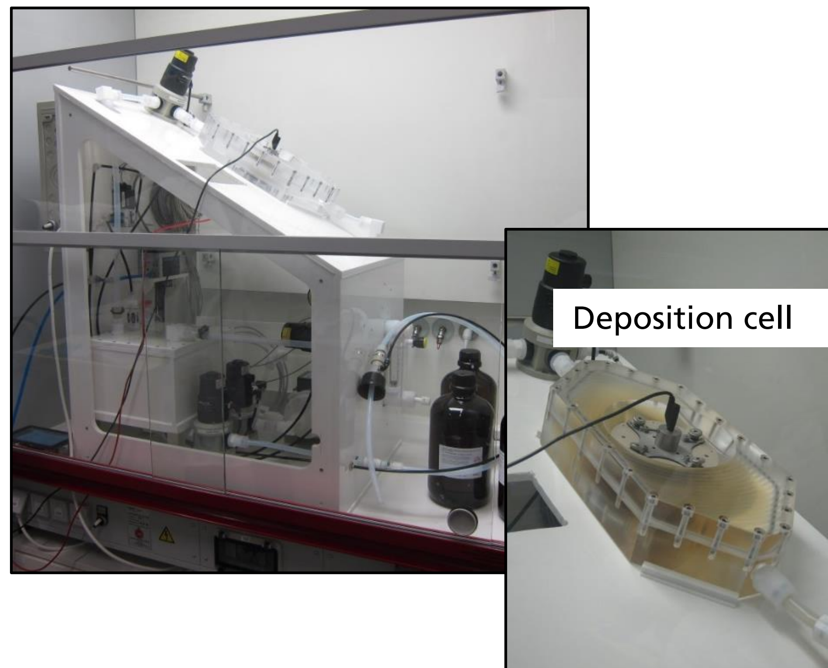
## @ Fraunhofer ENAS:

- Plating setup for 6 inch waferlevel inside a glovebox
- 180 ° tiltable cathode face up, Anode face down




## @ NB Technologies:

- Plating in standard fume hood
- deposition cell is rinsed with $N_2$ during sample exchange
- Cathode face down, anode face up







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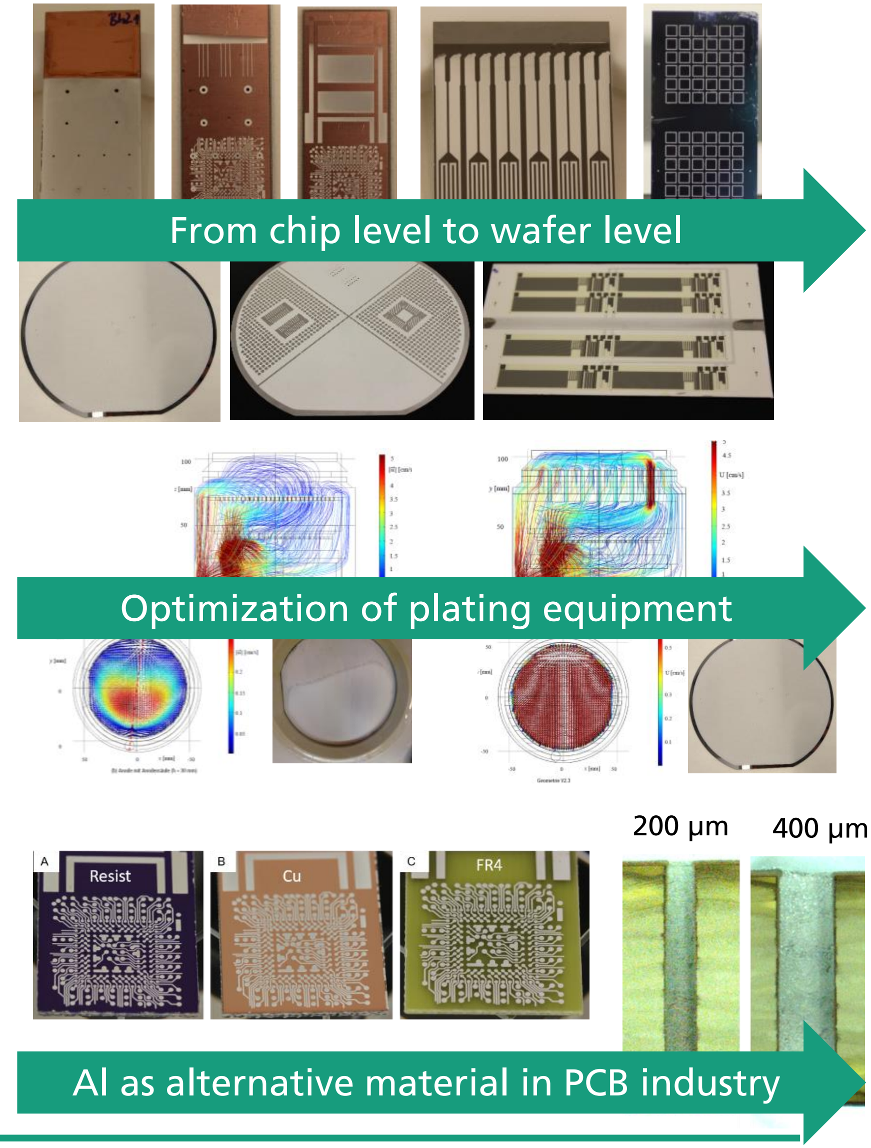
# Electrodeposition of Al: Process development steps

- Electrodeposition process of Al on various substrates developed incl. pretreatment of seed layer
  - Si wafer
  - Glass and ceramics
  - PCBs
- Up scaling from chip to 4 inch to 6 inch wafer level coating
- Optimization of the plating set up using fluid dynamic simulation
- Pattern Plating with photoresists and selective etching of Cu seed layer
- Showing the feasibility of Al deposition in vertical interconnects down to 200 µm in PCBs (AR: 1:5)



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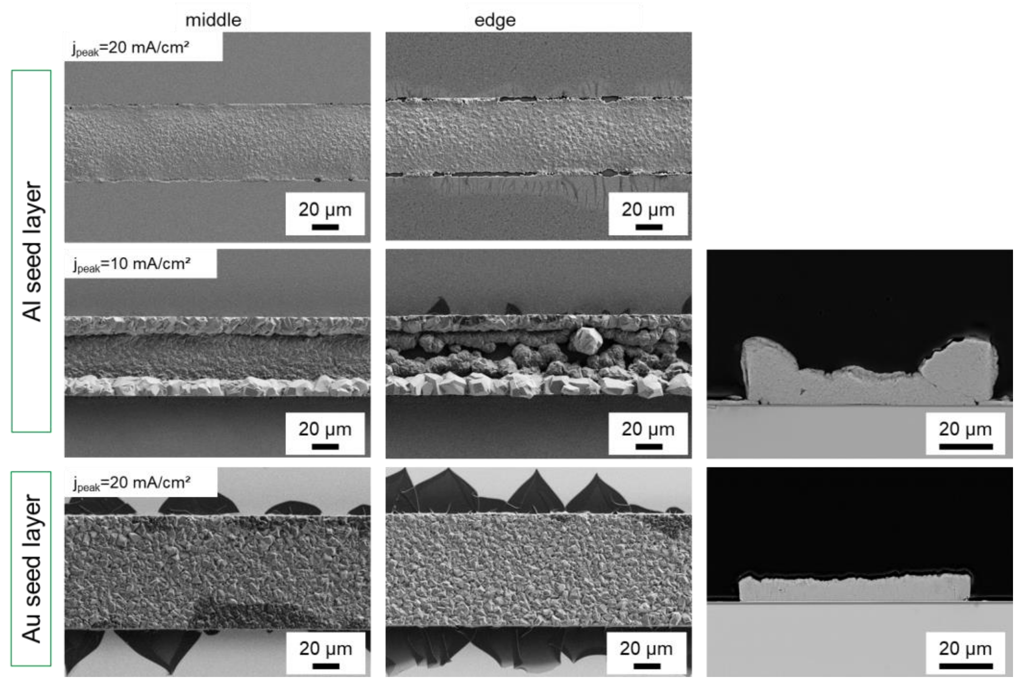
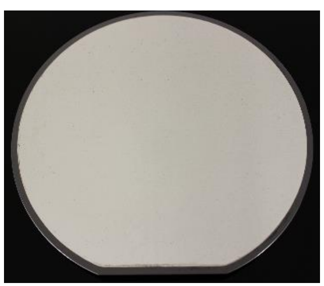
# Electrodeposition of Al: wafer level plating

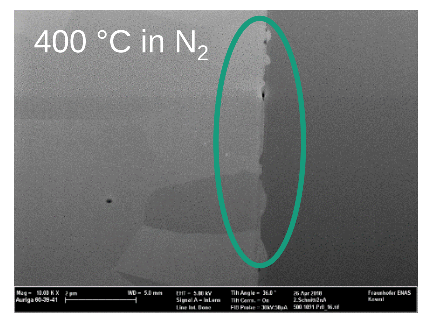
- Deposition parameters have to be adjusted for different seed layer
- Al ECD on Al seed layer needs further process development

⇒ First bonding trials with Al on Au seed layer

- Deposition on highly doped Si without seed layer possible
  - thermal post treatment necessary for sufficient adhesion



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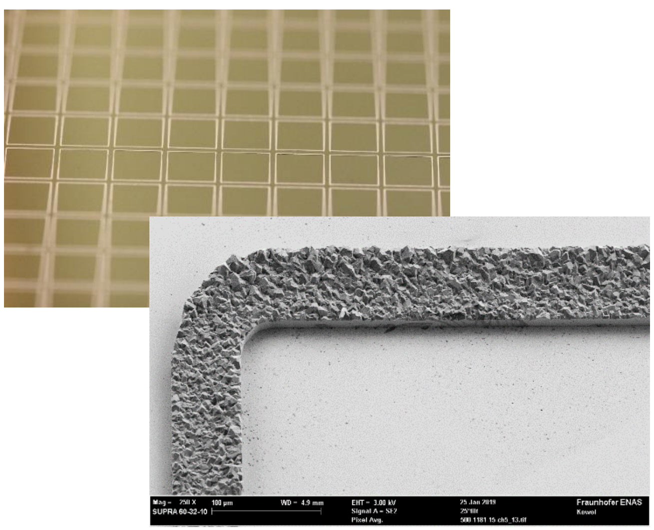
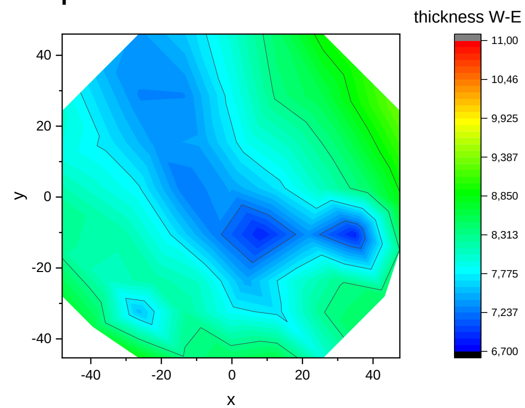
# Electrodeposition of Al: wafer level plating

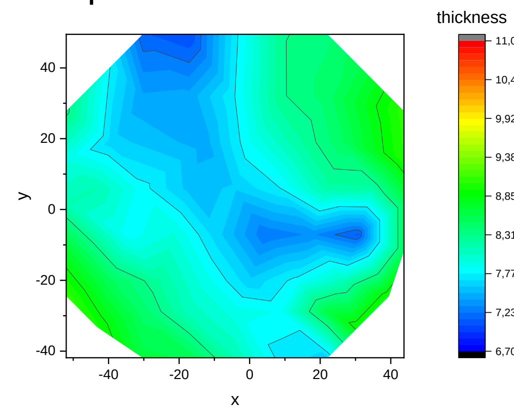
- Preparation of wafers with Au seed layer for bonding trials
- Deposition with same parameters shows reproducible layer thickness
  - Overall average thickness: **8,17 ± 0,30 µm (12 wafer)**
  - Some wafers are post treatet with CMP



80 µm frame width




60 µm frame width



# Bonding with electrodeposited Al: overview

| Wafer ID | Materials | F(MPa) | Temp |
|---|---|---|---|
| 1+1 (program error) | ECD+PVD | 47 | 500° |
| 2+2 | ECD+PVD | 47 | 500° |
| 11+3 | ECD+PVD | 35 | 400° |
| 12+4 | ECD+PVD | 52 | 400° |
| 3+13 | ECD+ECD | 52 | 400° |
| 4+14 | ECD+ECD | 35 | 450° |
| 16+5 | ECD+PVD | 35 | 450° |
| 17+6 | ECD+PVD | 35 | 450° |
| 7+7 | ECD+PVD | 35 | 450 |
| 6+8 | ECD+PVD | 21 | 450 |
| 5+9 | ECD+PVD | 35 | 400° |

Limit of bonder (EVG540) → are the asperities to high? Substrate cracking?

Temperature reduction

ECD vs ECD Al, What are challenges here?

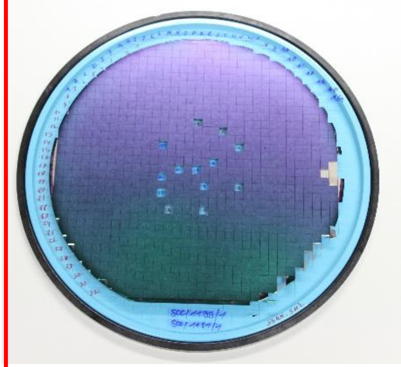
Same parameters with same behavior?

CMP pretreatment: How is the bonding working without the high roughness

# Bonding with electrodeposited Al: dicing yield

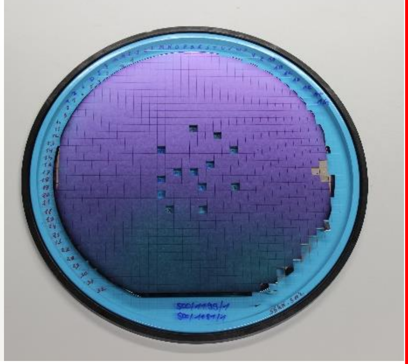
Further characterization

1+1



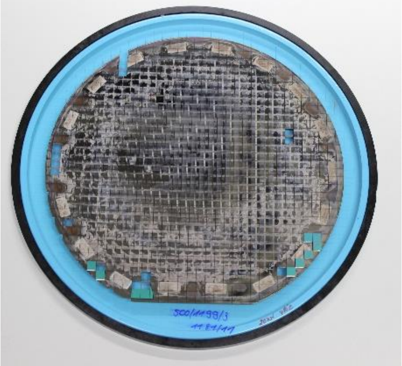
500 °C, 47 MPa, bond program failure

2+2



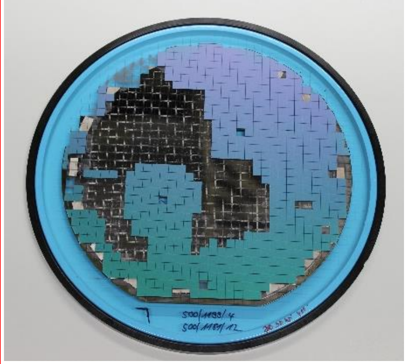
500 °C, 47 MPa

11+3



400 °C, 35 MPa

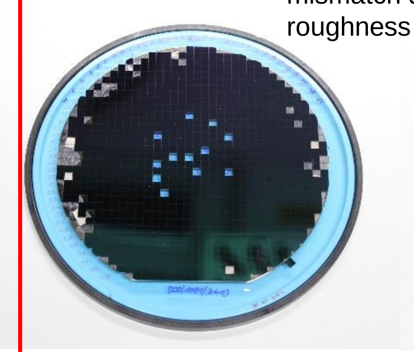
12+4



400 °C, 52 MPa

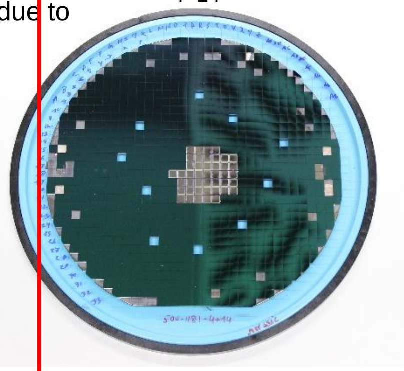
3+13

80 to 60 µm with bond mismatch due to roughness



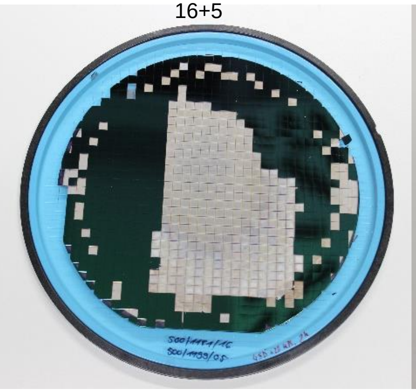
400 °C, 52 MPa

4+14



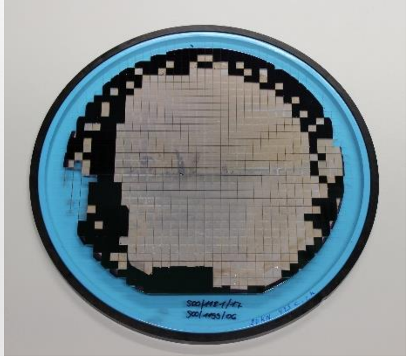
450 °C, 35 MPa

16+5



450 °C, 35 MPa

17+7



450 °C, 35 MPa



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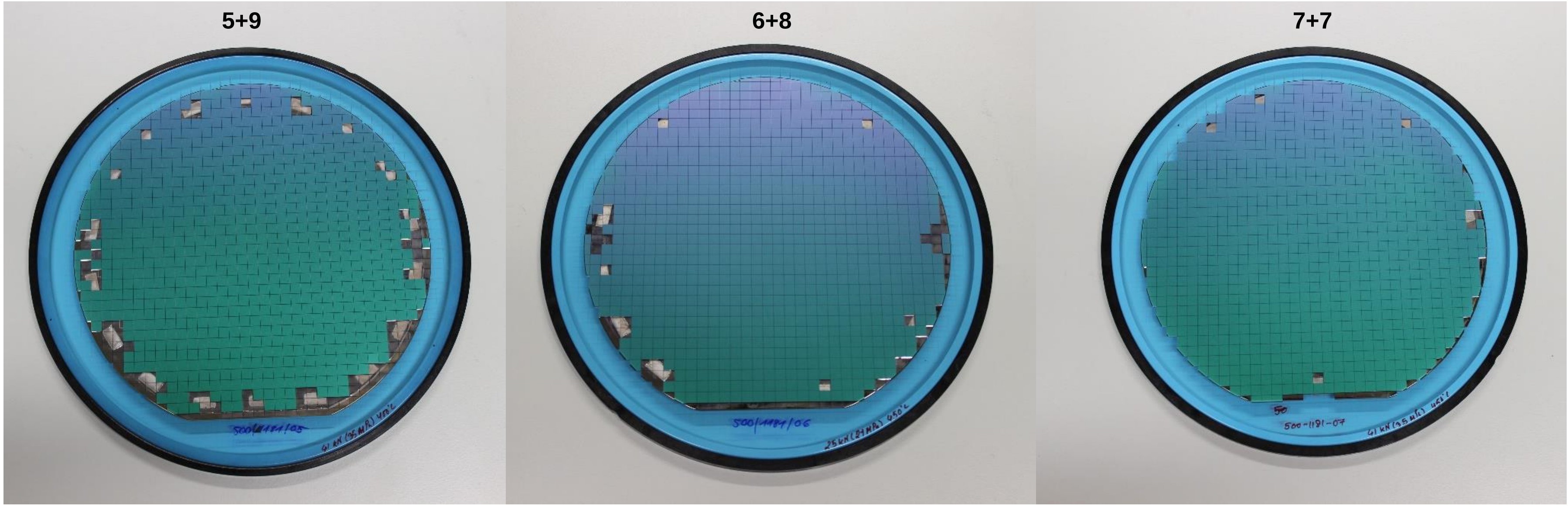
# Bonding with electrodeposited Al: dicing yield

- CMP pretreatment to remove asperities from ECD layer




400 °C, 35 MPa | 450 °C, 21 MPa | 450 °C, 35 MPa

Nearly 100% dicing yield → missing chips on the edges should not have been bonded due to current collectors

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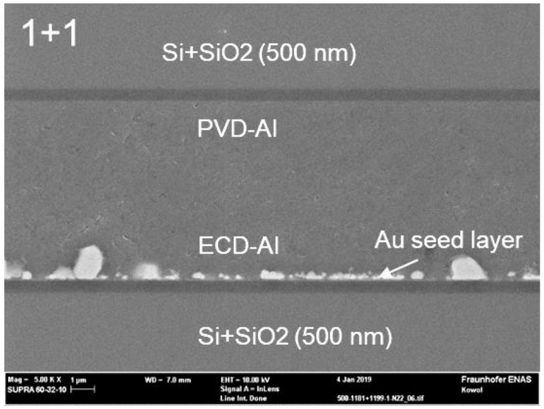
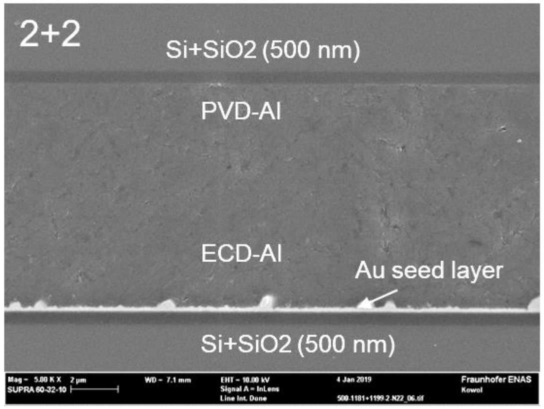
# Bonding with electrodeposited Al: cross sections

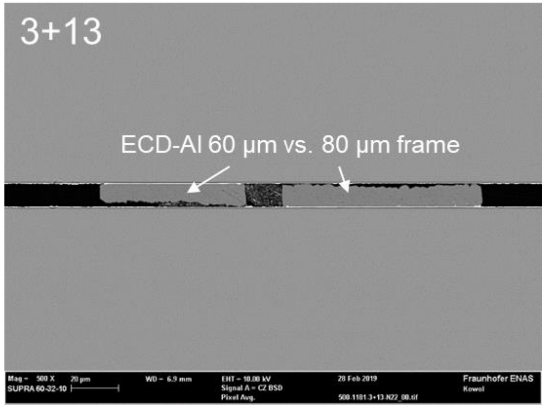
- High pressure + high temperature result in good bonding without visible interface (1+1, 2+2)
- Bonding of ECD vs. ECD need CMP at least on one side to reduce misalignment

Al compression ~2 µm



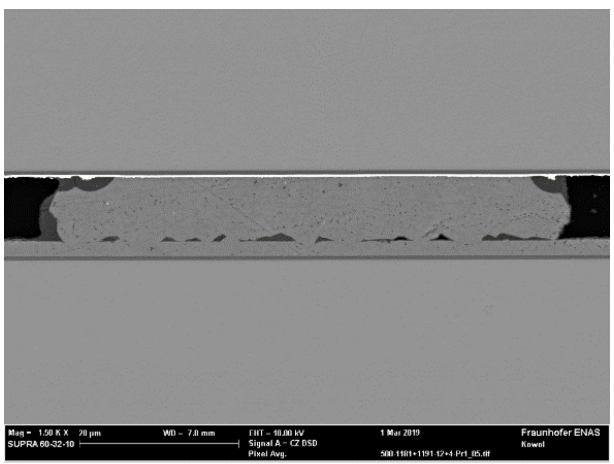

Al compression ~0,5 µm

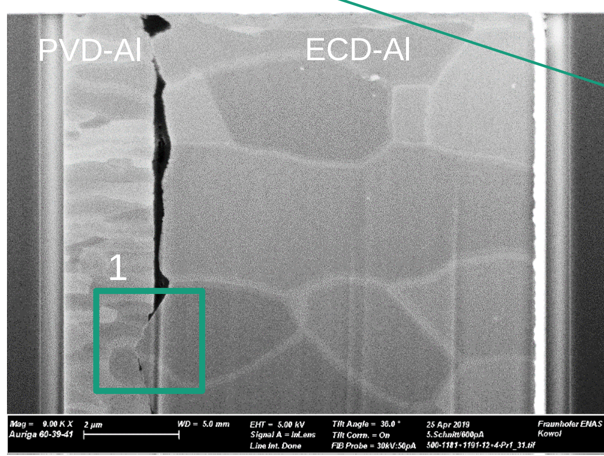


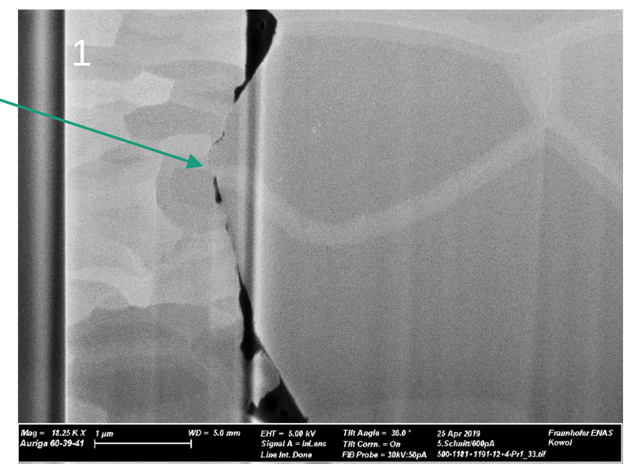



# Bonding with electrodeposited Al: cross sections

- Asperities can be pressed into PVD-Al layer
- Roughness is to high to achieve a void free interface
- FIB preparation shows grain structure
  - Large grains for ECD-Al
  - Grain interdiffusion started on asperities at 400 °C

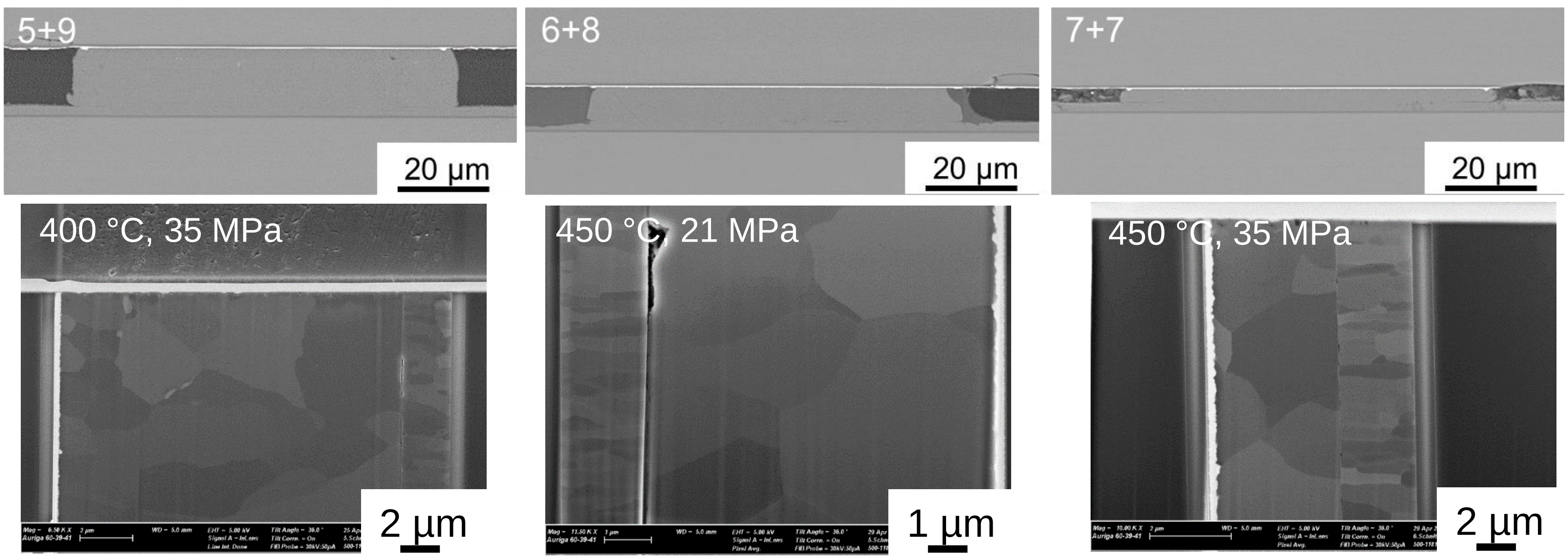




# Bonding with electrodeposited Al: cross sections

- Cross sections look well bonded
- Interface is visible in higher magnifications
- FIB preparation shows large Al grains on ECD side, but small grains on PVD side with no tendency to grow
  - → no interaction at the inferace due to Al oxide







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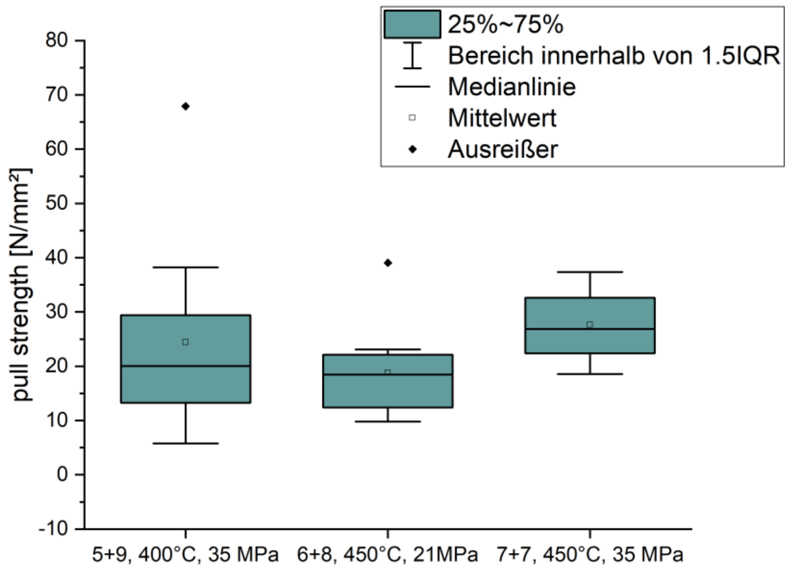
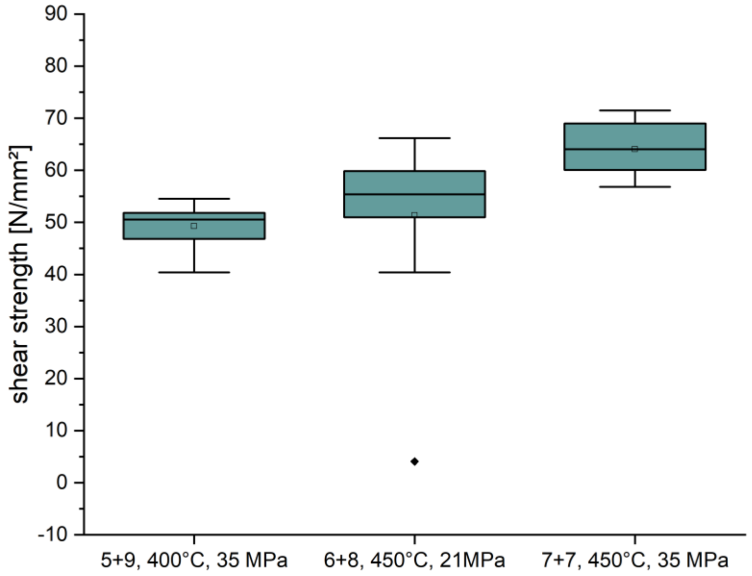
# Bonding with electrodeposited Al: bond strength

- 10 samples per method characterized
- Pull test dependents on glue interface to stud
- Without optimized parameters the strength can be compared to other TCB combinations







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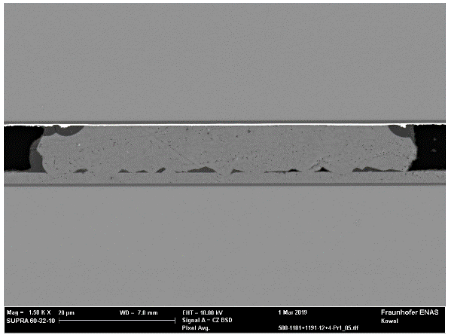
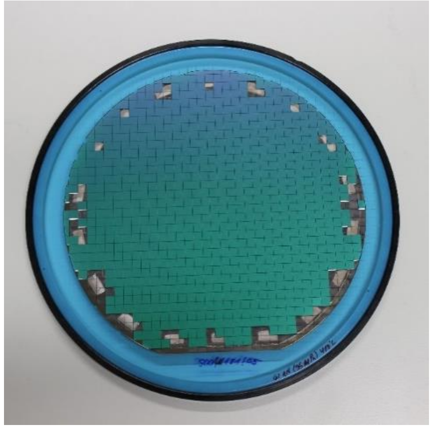
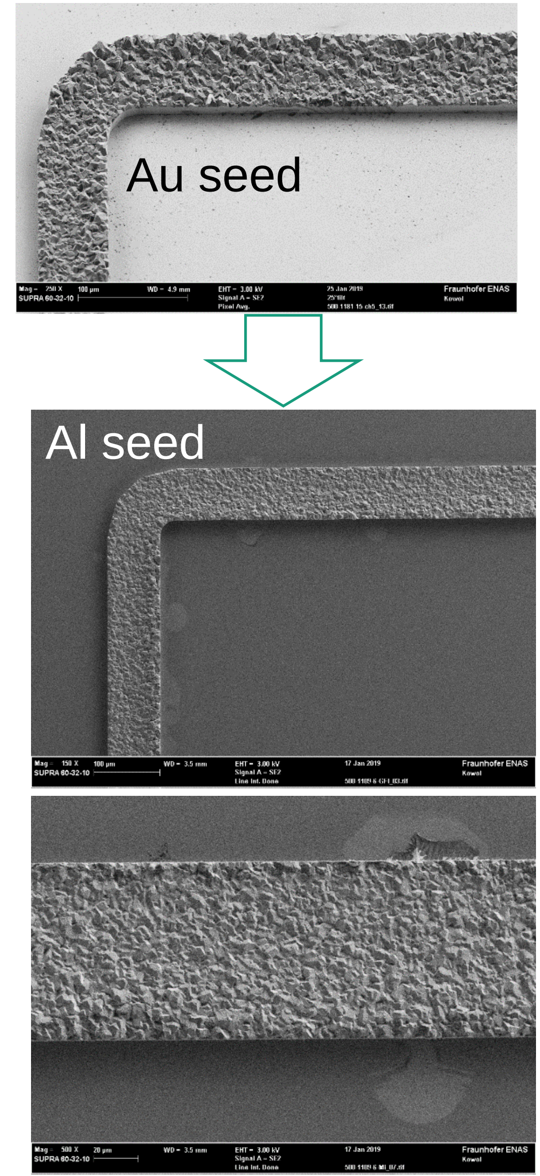
# Conclusion

- ECD of Al on wafer level is a reproducible process @ ENAS
- ECD-Al peaks can crack the Al oxide layer
  - Roughness to high to compress it
- Parameter scan for Al-Al-TCB
- Bonding with ECD-Al is possible: 400 °C, 35 MPa as lowest parameter set
- CMP can be applied to remove asperities of ECD-Al
- Hermeticity not clear yet
- ECD-Al is thermally active: grains can diffuse together
- PVD-Al is sputtered with highest power → grains are thermally inactive and show no diffusion any more



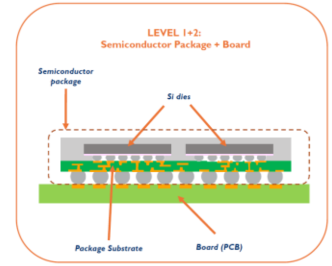


# Outlook



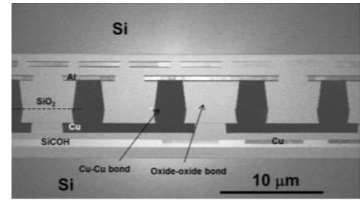

- Deposition process development of Al on Al seed layer ongoing
- Using low power sputtered Al for bonding to achieve better grain diffusion
- Bonding of ECD vs ECD Al with at least one CMP treated side
- Further reduction of bond temperature and pressure
- Detailed pull strength analyzation
- Hermeticity tests

# Outlook and Roadmap for ECD-Al



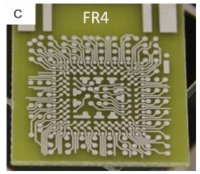

Quelle: Yole Report 2017: Status of Advanced Packaging

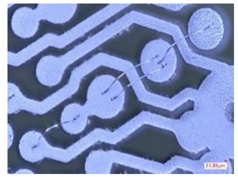
Advanced Packaging of all components

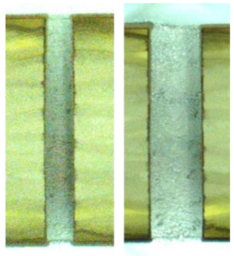



Quelle: Reliability of hybrid bond interconnects

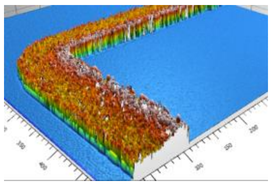
Flip Chip assembly using Al Pillars in future

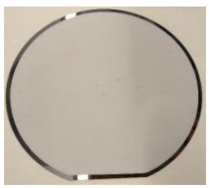


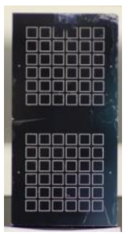






Al in PCBs







Basics of Al-ECD on various substrate evaluated within AioLi-project

Investigation of the bonding behavior of ECD-Al in Al-Al-Thermo-compression bonding

First results presented

Al coated mulilayer PCBs incl. via technology and soldering on Al surfaces

Al-Pillars for Flip Chip assembly resulting in an homogeneous package between MEMS, ASIC and PCB

Al-TSVs for MEMS applications and hybride wafer bonding with Al

Development duration is an estimation: acceleration is possible if industry push it in application cases

2017 2019 2023 2027

# Thank you for your attention

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