JUNE 13 AND 14, 2017 | FRAUNHOFER ENAS
TECHNOLOGIE-CAMPUS 3 | 09126 CHEMNITZ

CHEMNITZER SEMINAR
SYSTEM INTEGRATION TECHNOLOGIES

Advanced Packaging Technologies at Peking University

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14/06/2017
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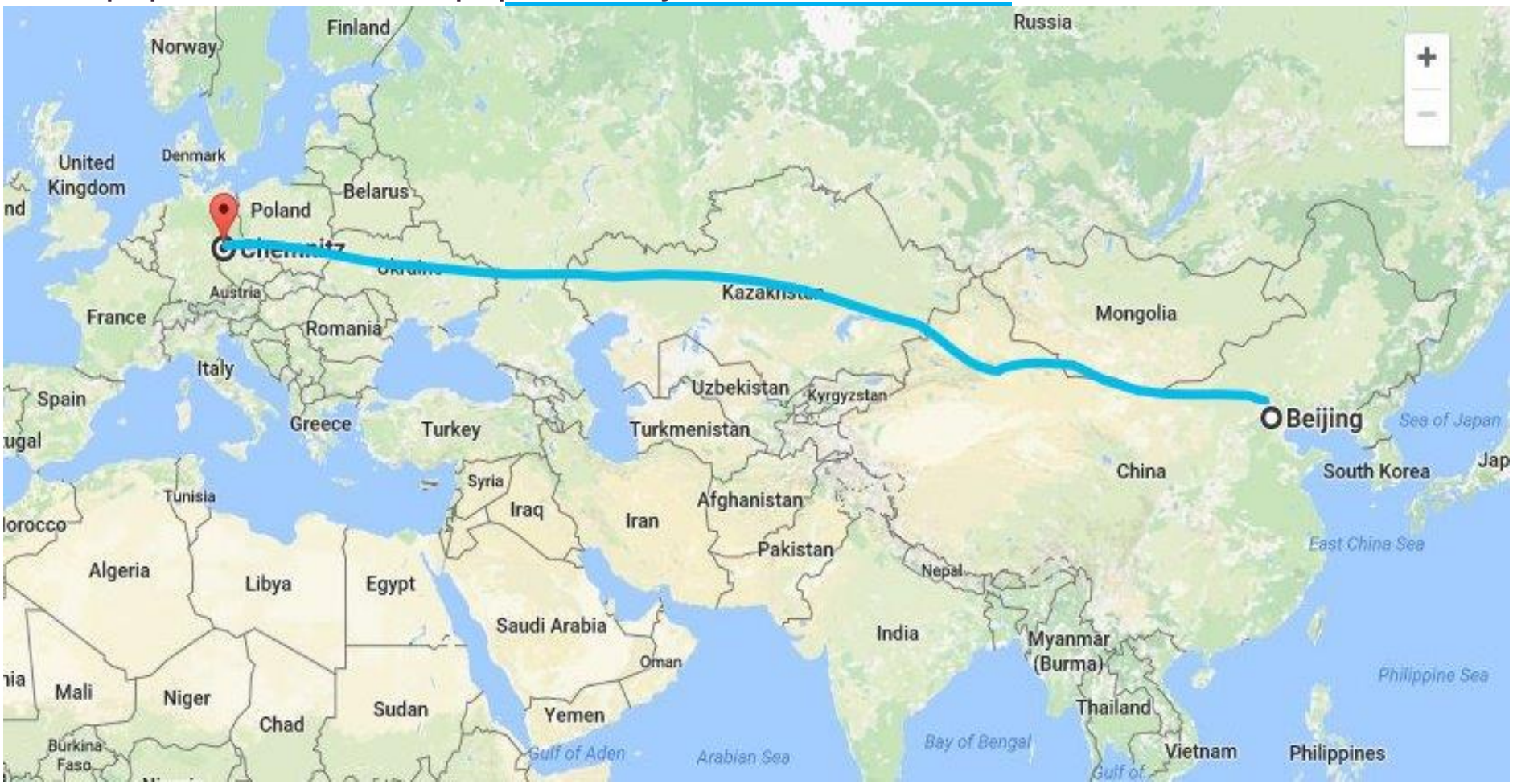
Peking University @ Beijing
Beijing or Peking ?
21M population, 3rd most populous city in the world

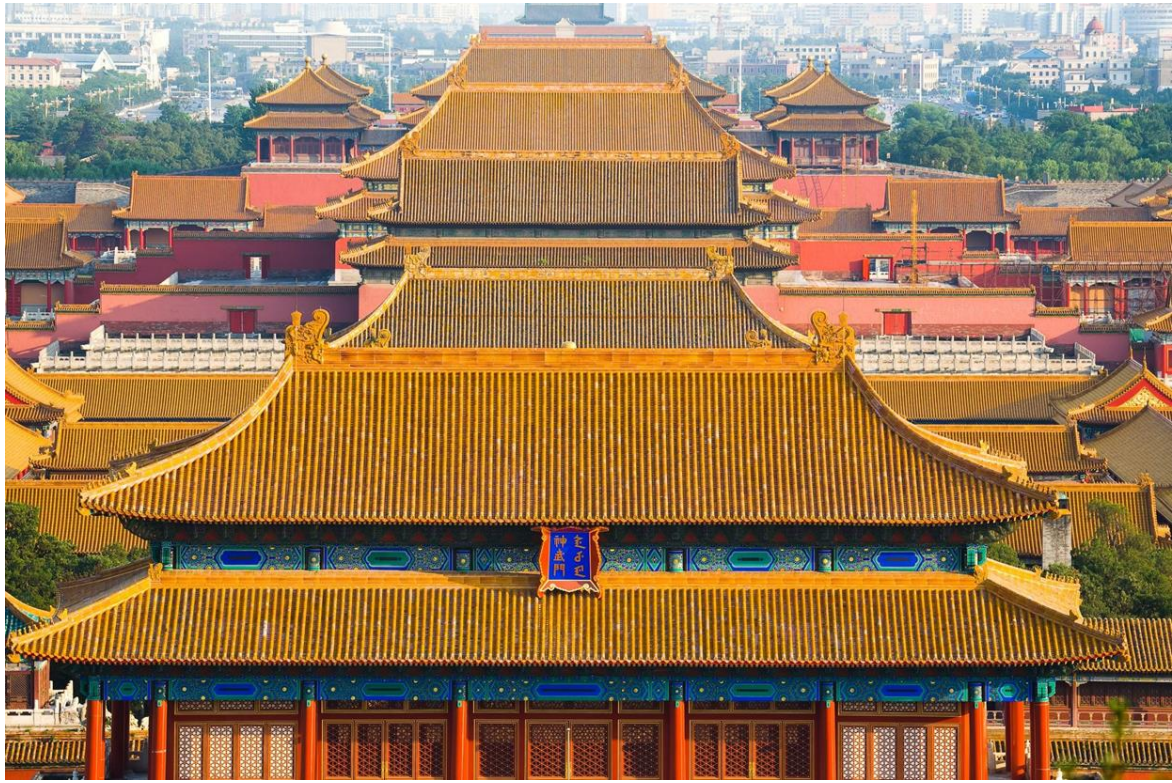


7395KM

Berlin — **Beijing**

The Great Wall is an ancient Chinese military defense project, for more than 2000 years. Great Wall was over 10,000 km

The Forbidden City is the royal palace of China, **built from 700 years ago.**
It is the largest and most complete ancient building complex existing wooden structure in the world. The Forbidden City known as the world's top five palace



Tian'anmen Square is the main entrance of The Forbidden City in Ming and Qing Dynasties .Only the ancient emperor can go through. Tian'anmen covers 4800 square meters, is the world's largest city center square.

The Summer Palace

The Summer Palace was built in 1750.It's is the royal garden of the Qing Dynasty, whereTte royal family met with foreign guests and lived..

One of 91 universities in Beijing, Peking University founded in 1898, is the first national comprehensive university in China, with 15,000+ staffs and 36,000+students. Many students come from different countries

National key lab of Science and Technology on Micro/Nano Fabrication

- **Established in 1996. cleanroom 1000m^2**
- **Full professor: 10; Associate professor: 3**

  engineers: 10+
- **PhD: 50 +, M.S. : 40 + students**
- **Three key fields:**

  - Micro/nano fabrications

  - Micro/nano sensor/actuators

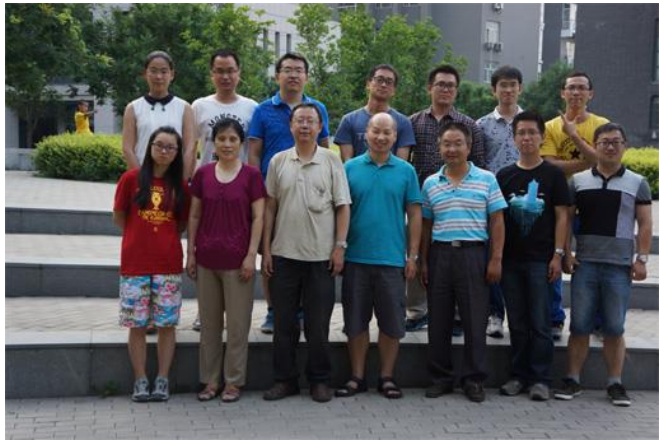
  - Integrated micro/nanosystems

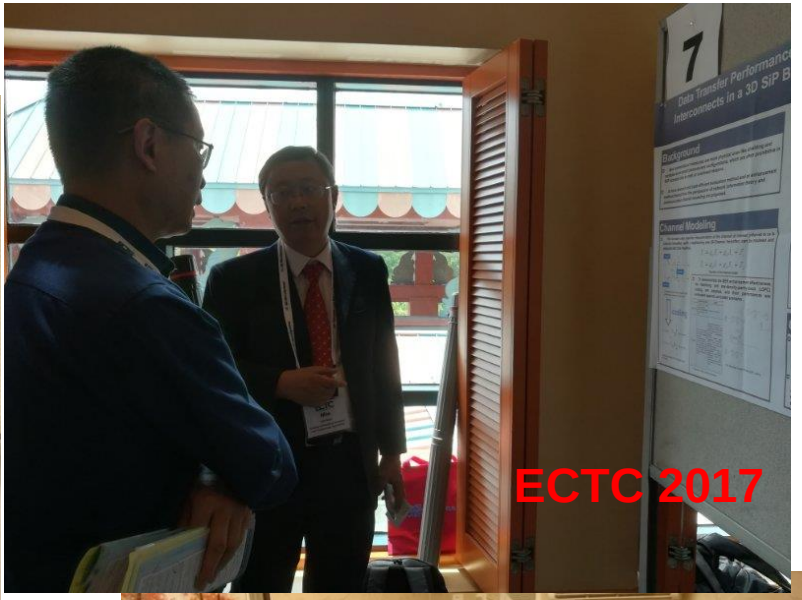
Future Research

- **Two key techniques for established MEMS products**
  - **TSV-based 3D integration**
  - ***in-situ* process-quality monitoring**
- **One key MEMS application**
  - **Human-machine interface: e-brain (collaborate with Profs. in SOC/ULSI)**
- **Future plan**
  - **MEMS application for health care and biology**

3D SiP group @ Peking University

professors: Yufeng Jin, Wei Wang,Jing Chen, Min Miao, AP Shenglin Ma,
7 PhD students: Yong Guan, Yudan Pi, Qinghua Zeng...
18 M.S. students Ningyu Wang, Li Ma, Jingnan Gao…





ECTC Jun. 2, 2017,
Orlando, FL, USA

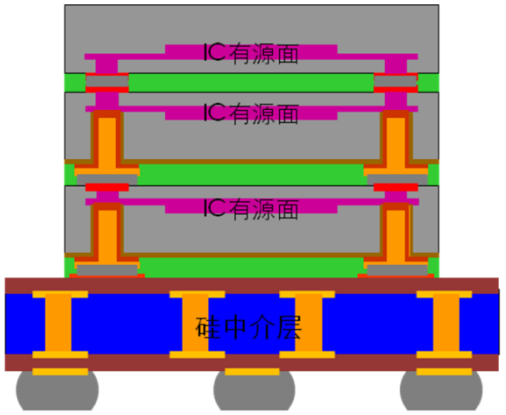
R&D Experiences(1/4)

- Dec. 2008 –Jun. 2011, to **develop the TSV fabrication process** recipes for different electronics product, e.g., NAND flash memory, application , funded by : ASTRI, Hong Kong & Intel

Tin plating with mask to form microbump on Pads of NAND chip

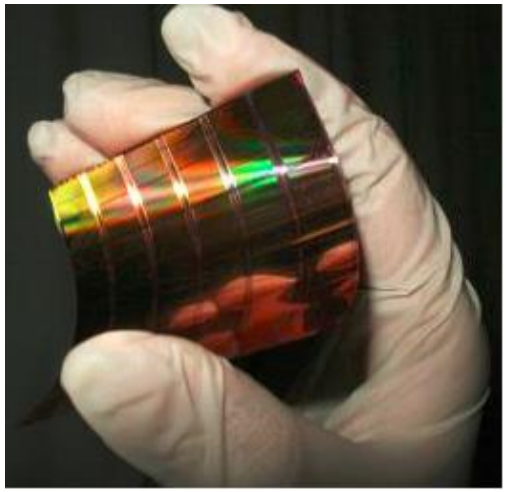
Copper plating with mask to fill TSVs and form micro-bump with tin plating, singulation

Transfer of thinned NAND chip pannel on carrier wafer to form TSV under Pads



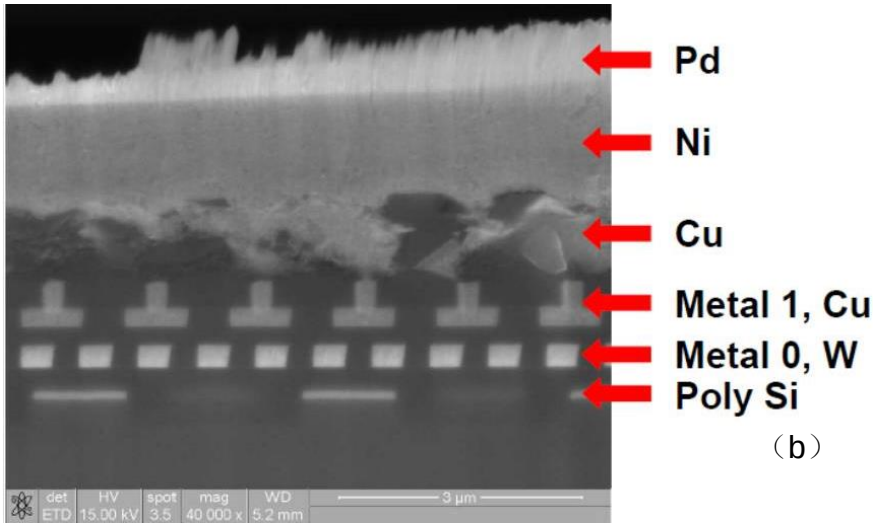
stacking of thin layer of NAND chips

R&D Experiences(2/4)

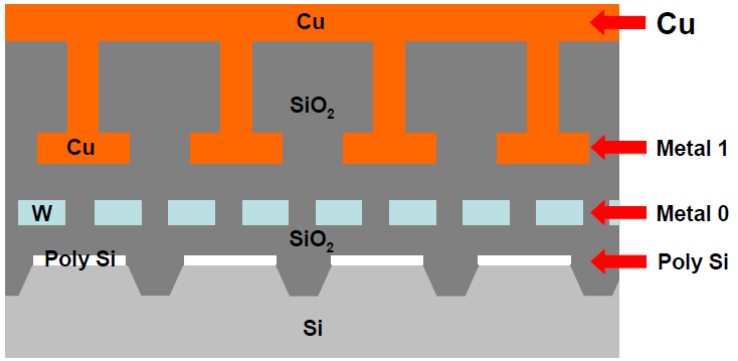


diced NAND(40nm) chip panel,
thickness:70μm size :62mm×62mm

I/O layout of NAND chip
（ size:1.05mm×16mm）

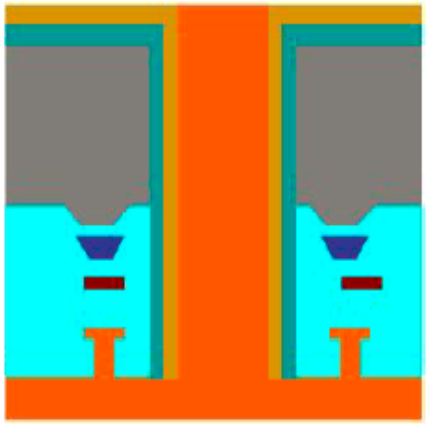


（b）

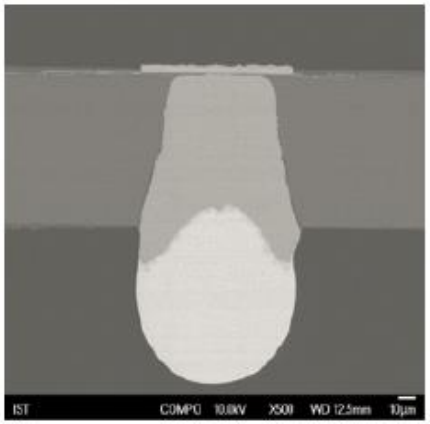


Crossection view of I/O pad of NAND chip

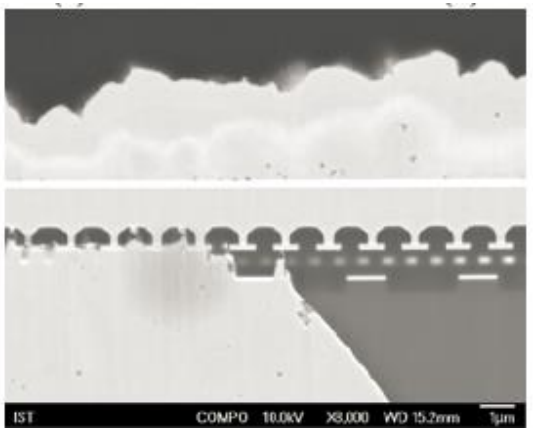
R&D Experiences(3/4)



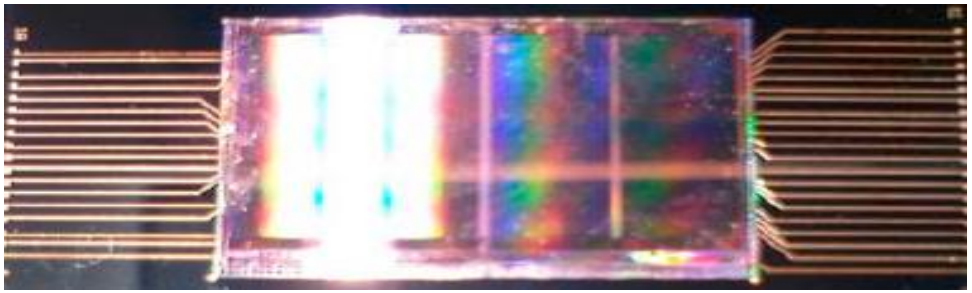
Crossectional view of Under Pad TSV interconnection



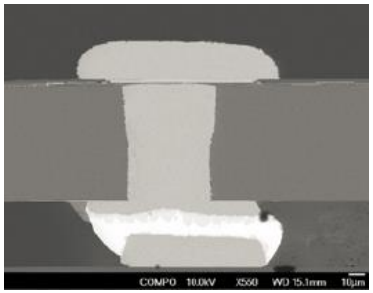
SEM photo of Under Pad TSV Crossection sample



Close-up SEM photo of Under Pad TSV crossection sample



NAND chip assembed on Si test board with Under pads TSV interxonnections

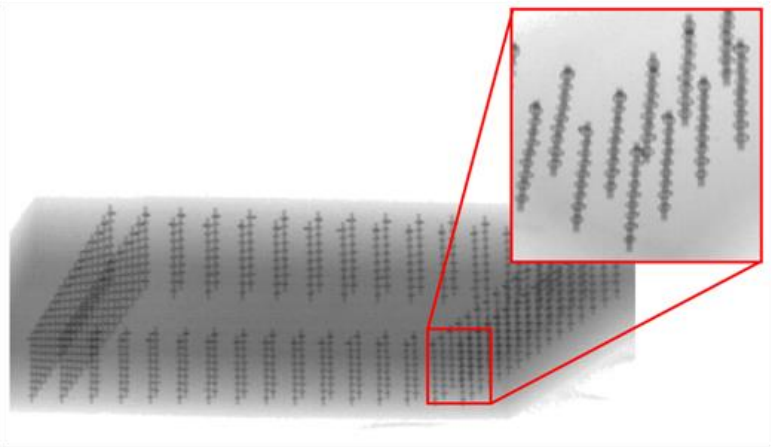


SEM photo of crossection of NAND chip assembed on Si test board

"Development of CMOS-Process-Compatible Interconnect Technology for 3D-Stacking of NAND Flash Memory Chips," 60th Electronic Component and Technology conference(**ECTC), Las Vegas, Nevada USA, Jun. 1-4,2010,pp.74-78**.

R&D Project Experiences(4/4)

- Jan. 2009 – 2012 ,to develop the key technologies for TSV-based 3D package technology ,funded by National Science & Technology Key Project
- Key technological parameters:
  - ✓ TSV size:20,AR:5
  - ✓ **No. of stacked layers:10**



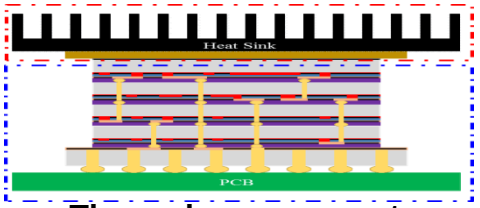
X-ray photo of 10 TSV test chip layers stack module

Crossectional SEM photos of 10 TSV test chip layer stack module

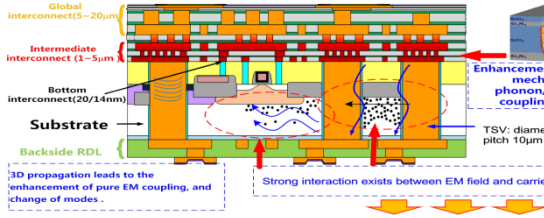
"Design and Process Development of a Stacked SRAM Memory Chips Module with TSV Interconnection"62nd Electronic Components and Technology Conference (ECTC),San Diego, California, USA, May 29 - June 1, 2012
"Development and Characterization of a Through-Multilayer TSV Integrated SRAM Module," 63rd Electronic Componentsand Technology Conference (ECTC), Las Vegas, NV, US, pp. 885-890, 28-31 May 2013.

Current research

Advanced Packaging for
- **NEMS, bio-MEMS**
- **3D RF Module**
- **20/14nm IC**
- **Multi-chip/sensor integ.**

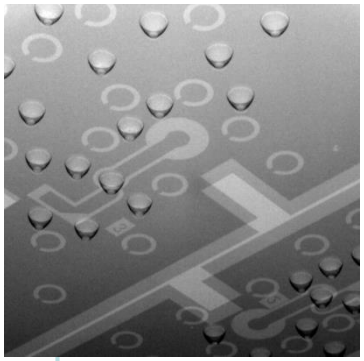


Thermal management



electromagnetic modeling and Simulation

Packaging
- **For MEMS**
  (Inertial sensor, RF)
- **For stacking chips**
- **LTCC based integ.**



Interposer for high-f intergration

Multi-sensor integration

PAST RESEARCH

CURRENT RESEARCH

Outline

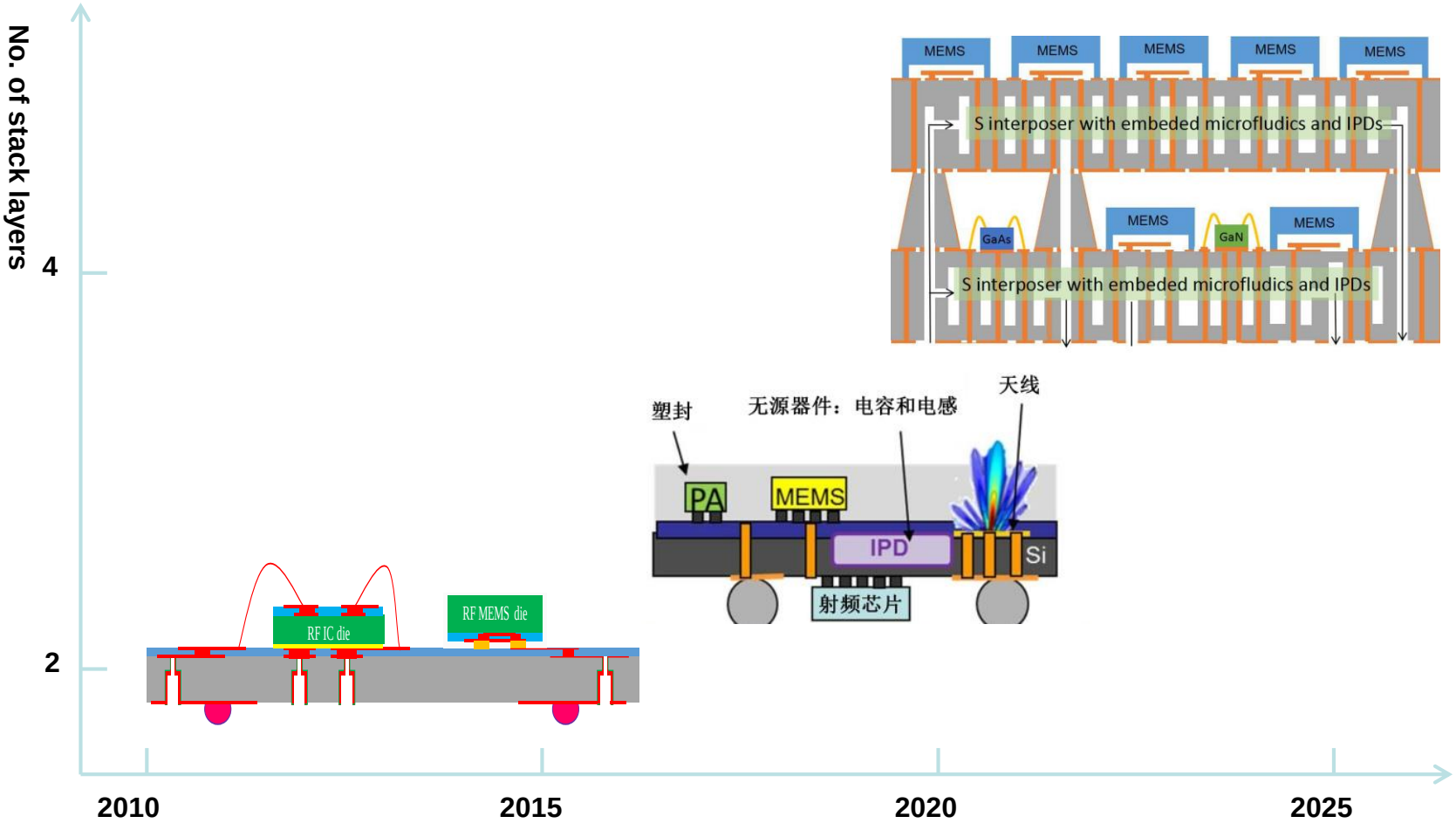
Part 1: TSV/TGV 3D Packaging For RF Module

Part 2: 3D Packaging For 20/14nm IC

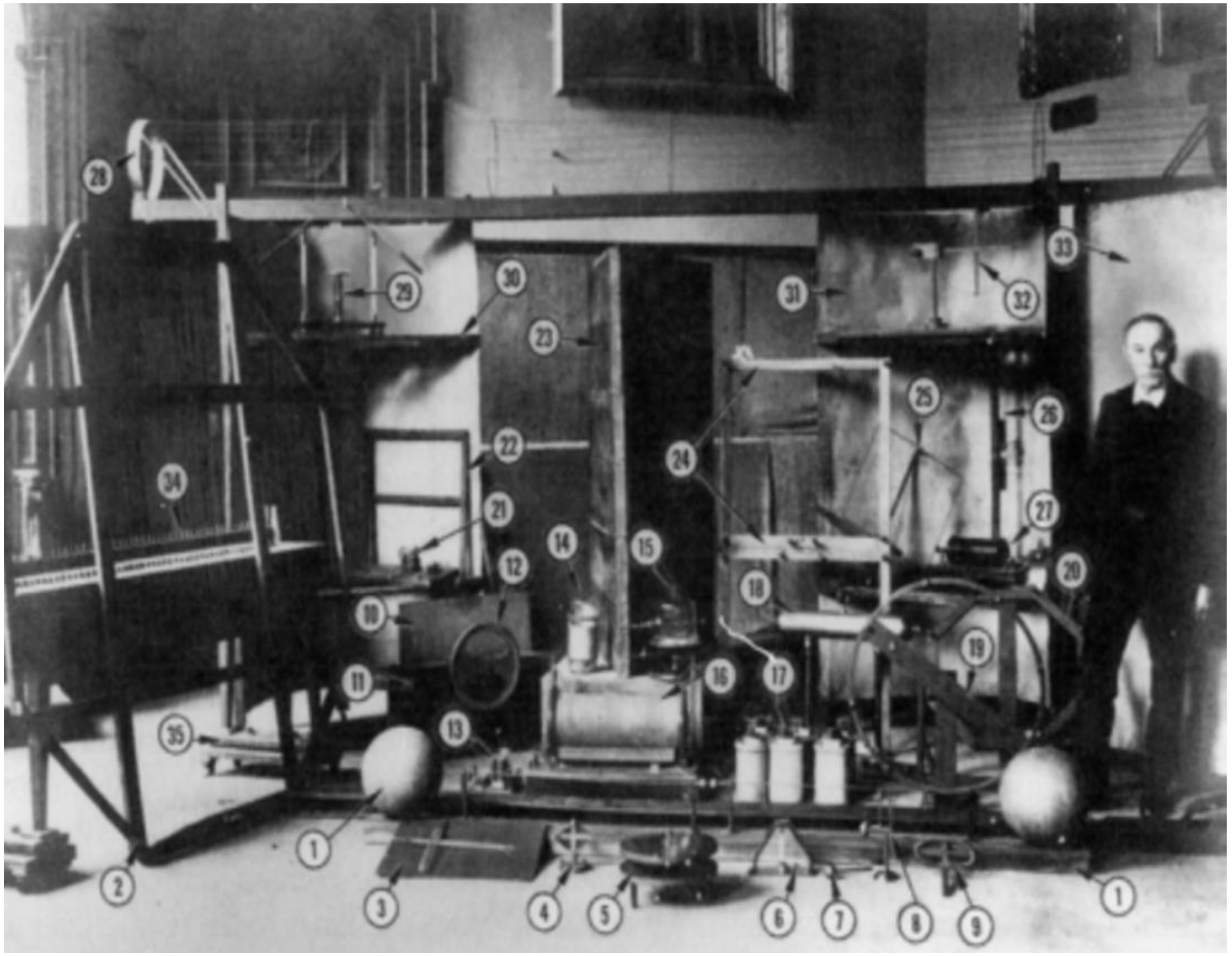
Part 3: Thermal management for 3D Stacked IC

Part 4: Packaging for multi-sensor application

Part 1: TSV/TGV 3D Packaging For RF Module



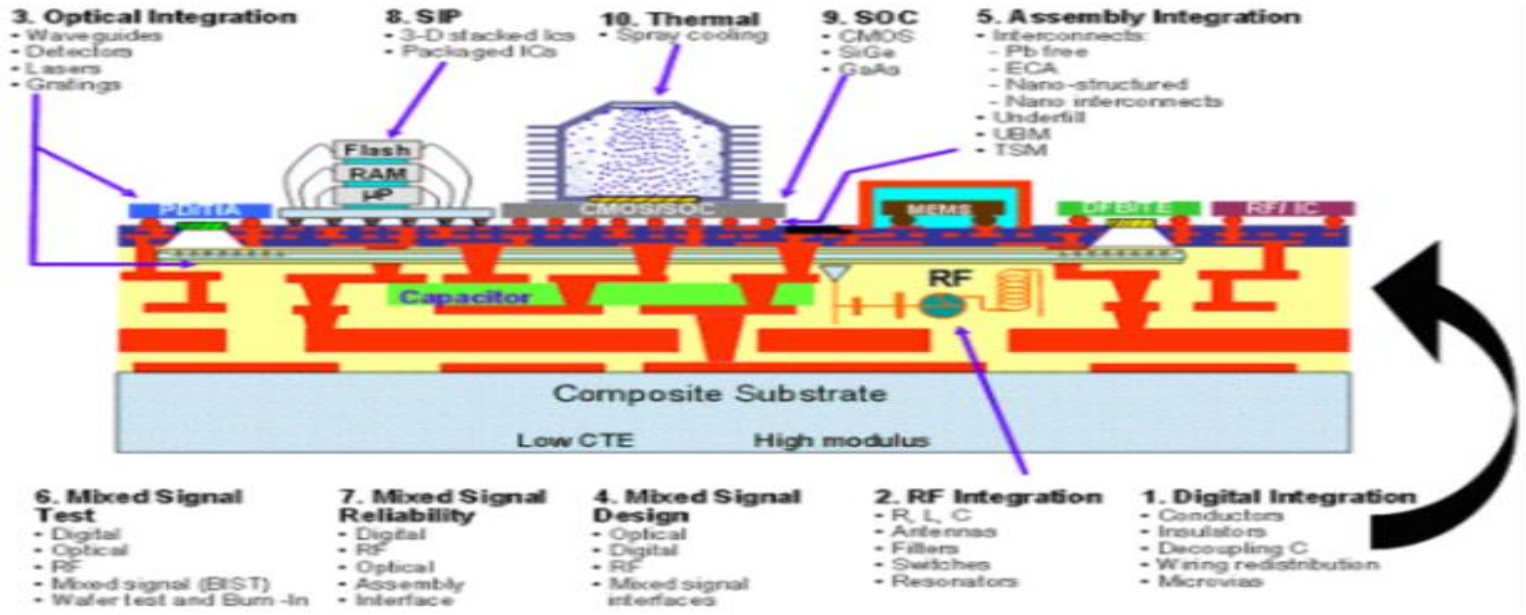
Frequency:	~2GHz	~20GHz	60GHz
Integrated passives:	planer Inductor	3D Capacitor, inductor, filter	3D Capacitor, 3D inductor, filter,microfludics...
Min. Critical dimension:	~50μm	~30μm 3D vias	~10μm



A system photographied at october1,1913,at the Bavarian Academy of Science, Munich, Germany, with Hertz's assistant, Julius Amman.

Advanced package for RF module is needed!

- ✓ Smaller size
- ✓ Better performance
- ✓ More function
- ✓ Lower cost



Potential applications

- 5G, RF frontend
- Wearable electronics
- Internet of things
- Radar
- Automotive electronics

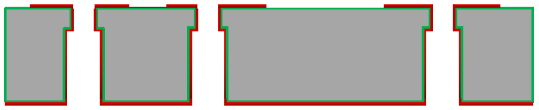
1.1 High resistivity Si interposer for 2.5/3D RF integration(1/4)

- started since 2012, cooperated with CETC, to **develop Si interposer for 2.5/3D RF integrated module** **with** RF transmission lines:CPW,Microstrip
- key technological parameters of TSV interposer：

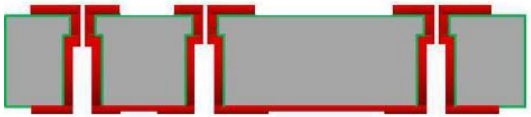
✓ TSV size:40/80μm,AR≈5,

✓ No. of RDL：≧2；

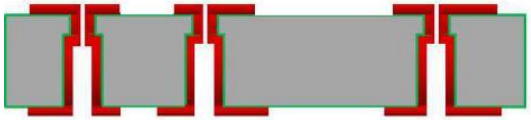
(a)TSV formation



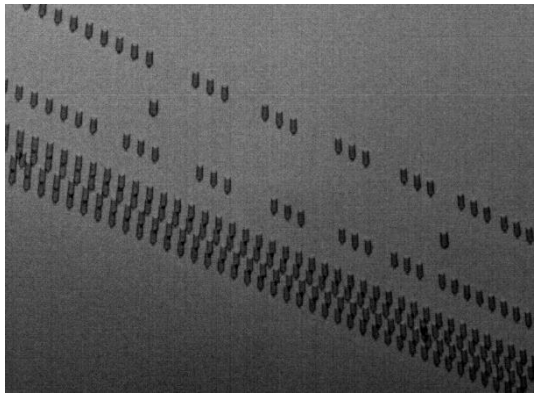
(b) barrier/seed layer deposition



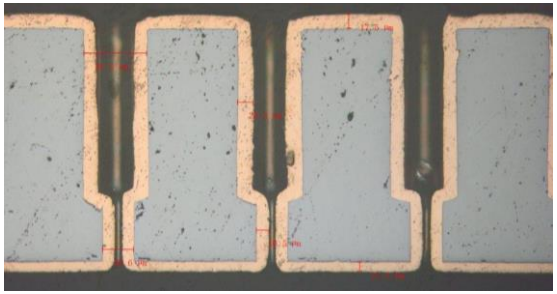
(c) Copper plating with mask



(d) removal of barrier/seed layer



X-ray image of TSV array

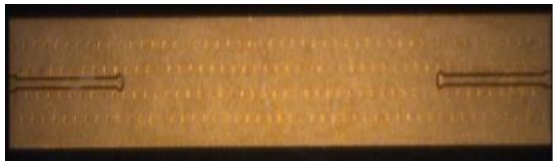


Crossectional view of TSV sample

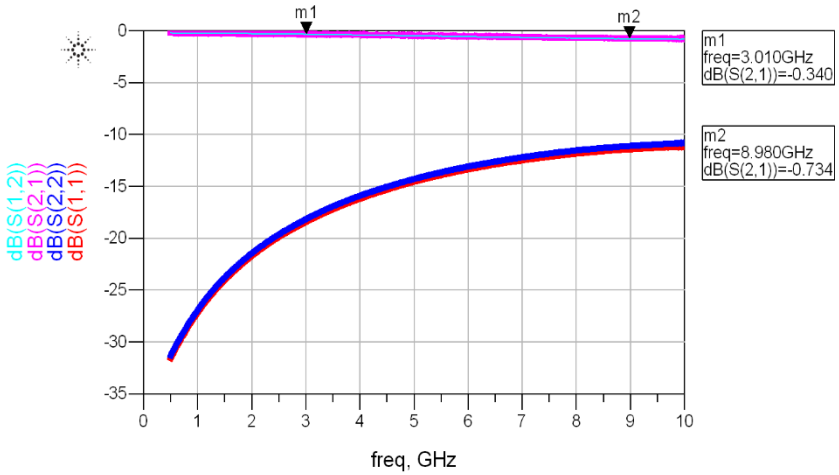
High resistivity Si interposer for 2.5/3D RF integration(2/4)

- Si interposer sample and test results

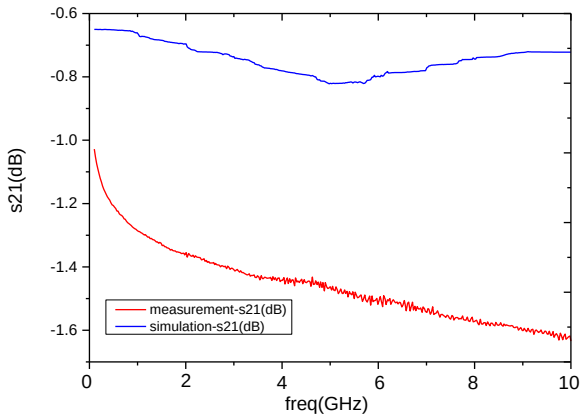
TSV array grouned CPW line



2 TSVs linked CPW line



S parameters test results for TSV array grouned CPW line

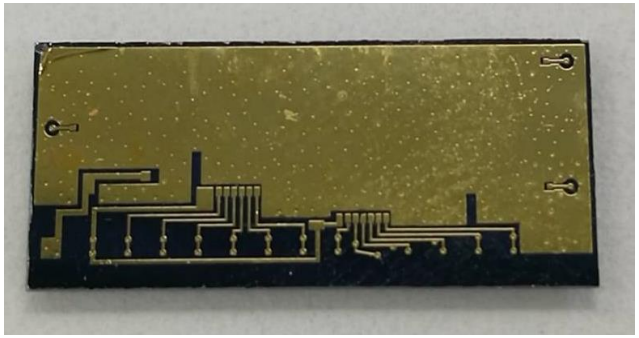


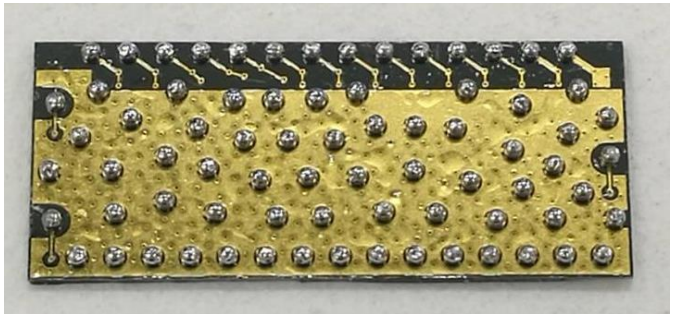
simulation and test results for 2 TSVs linked CPW line

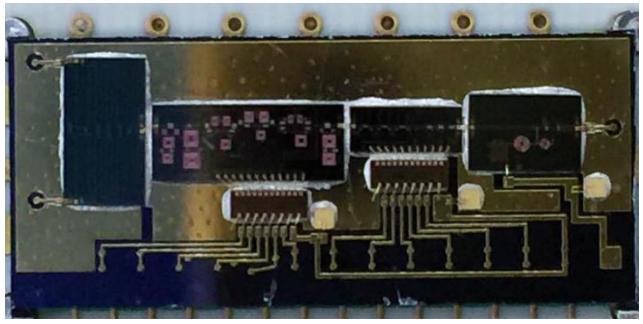
TSV/TGV/TXV based 3D integration technology and applications, **Keynote speech**, **2016 IEEE MTT-S, July 20-22, 2016**,Chengdu,china

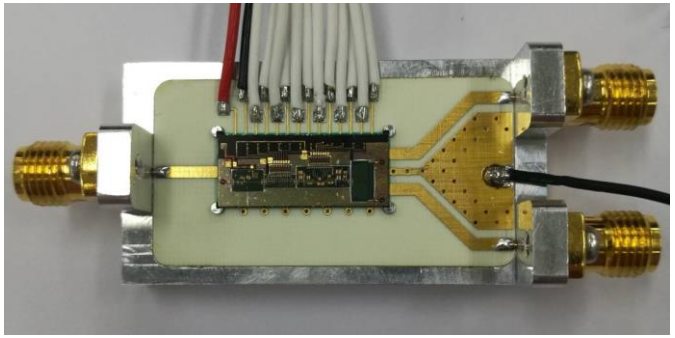
High resistivity Si interposer for 2.5/3D RF integration(3/4)

- Fabrication of Si interposer based **2.5D RF receive module**
  - ✓ Size:16mm×7mm×1.5mm;
  - ✓ No. of RF devices：6；
  - ✓ frequency：0.9-2.7GHz；



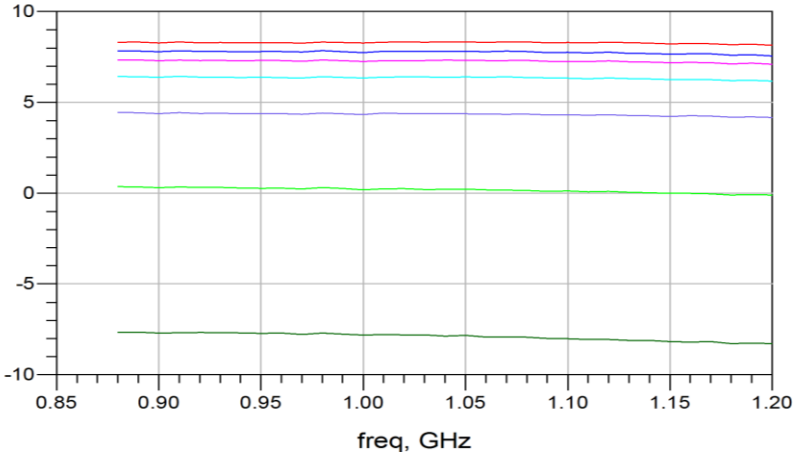


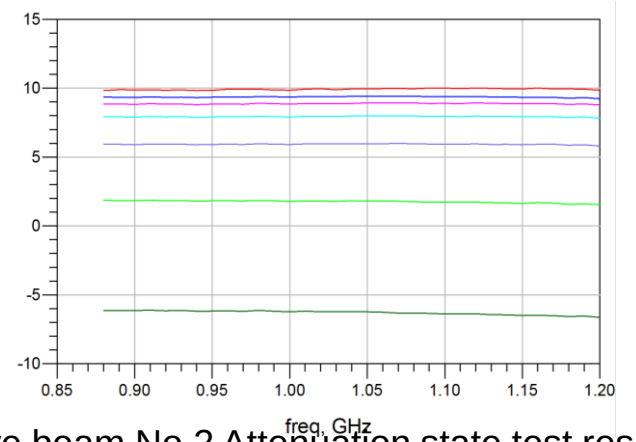




High resistivity Si interposer for 2.5/3D RF integration(4/4)

- TSV interposer based 2.5D integrated RF receive module function test results





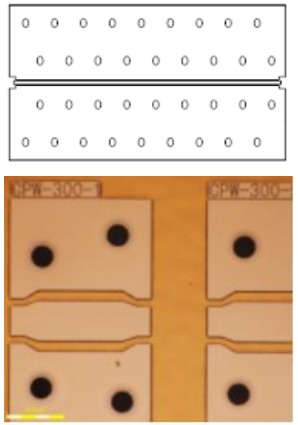
Wave beam No.2 Attenuation state test results

Test results of TGV interposer based 2.5D Receive module

test results(1GHz)	Gain（dB）	Input VSWR	Output VSWR	Phase shift	attenuation state control
Wave beam No.1	9.9	1.33	1.34	work	work
Wave beam No.2	8.24	1.33	1.85	work	work

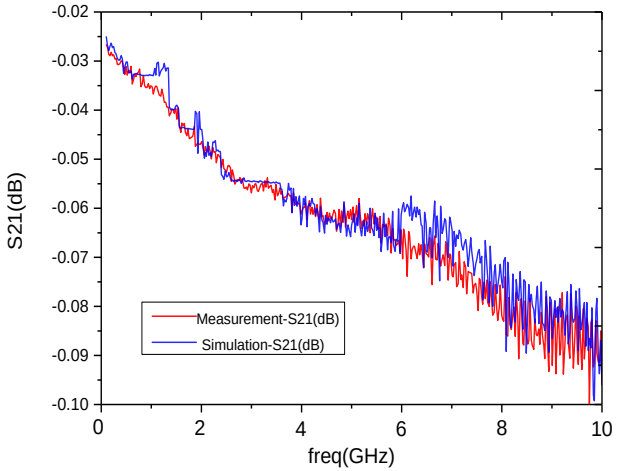
1.2 Glass interposer for 2.5D RF integration(1/3)

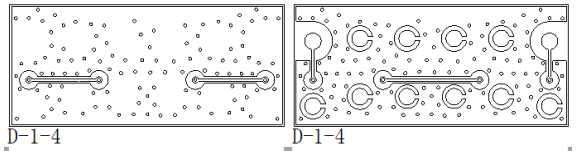
- TGV interposer for 2.5D/3D RF integrated system

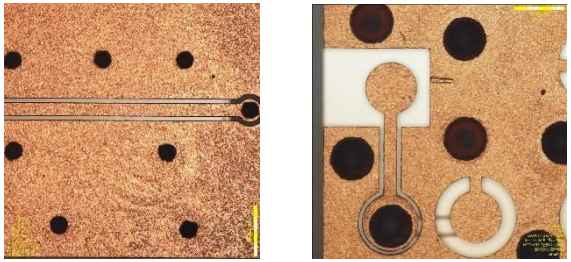


TGV grounded CPW line

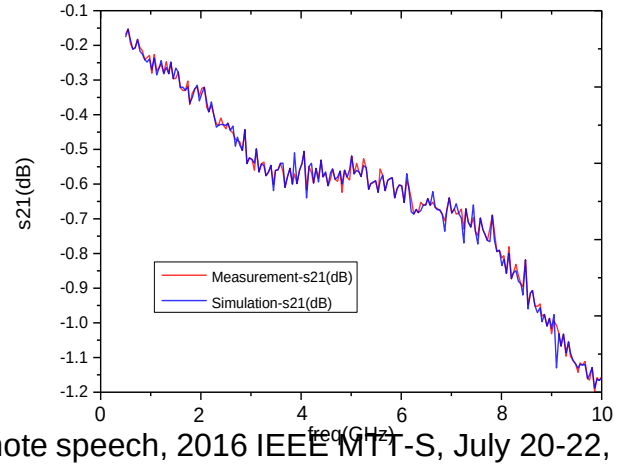
simulation and test results for TGV grounded CPW line







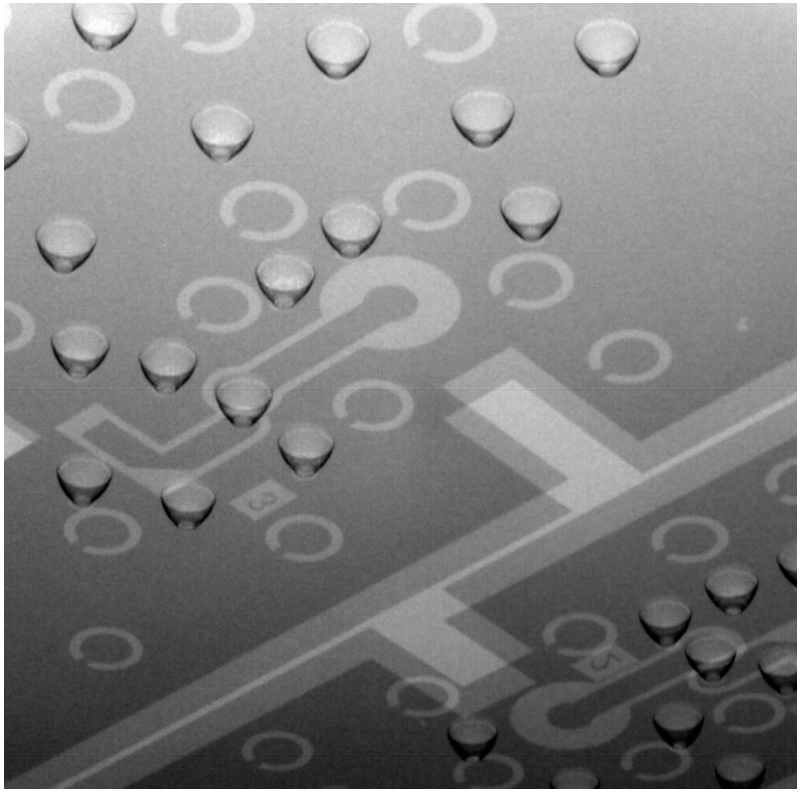
simulation and test results for four TGVs linked CPW line

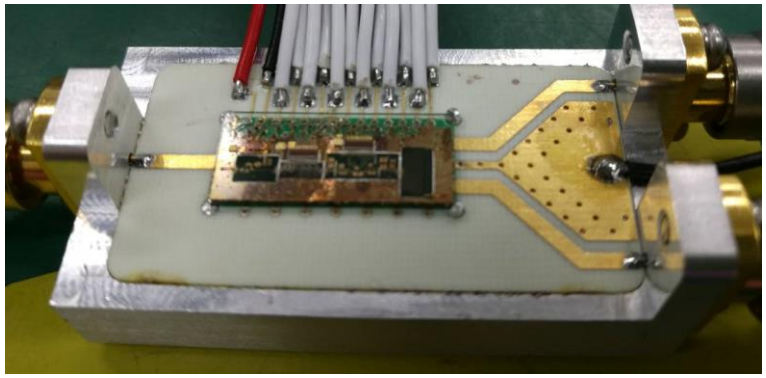


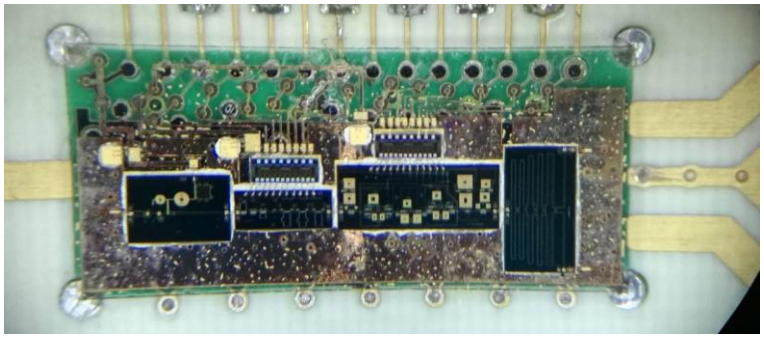
TSV/TGV/TXV based 3D integration technology and applications,Keynote speech, 2016 IEEE MTT-S, July 20-22, 2016,Chengdu,china

TGV interposer for 2.5D RF integration(2/3)

- TGV interposer based 2.5D RF receive module

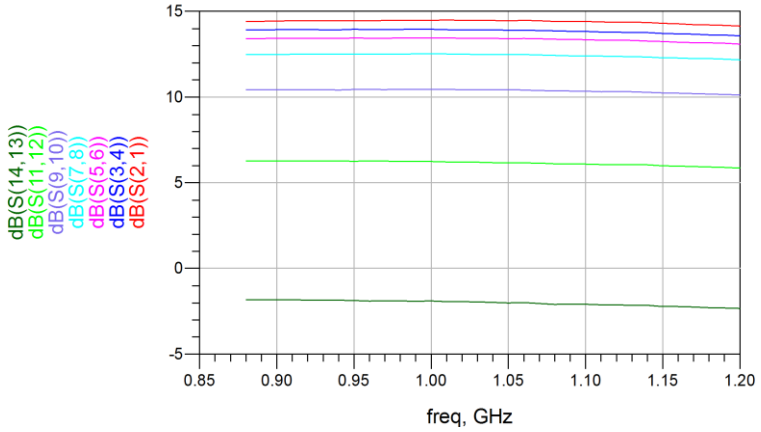




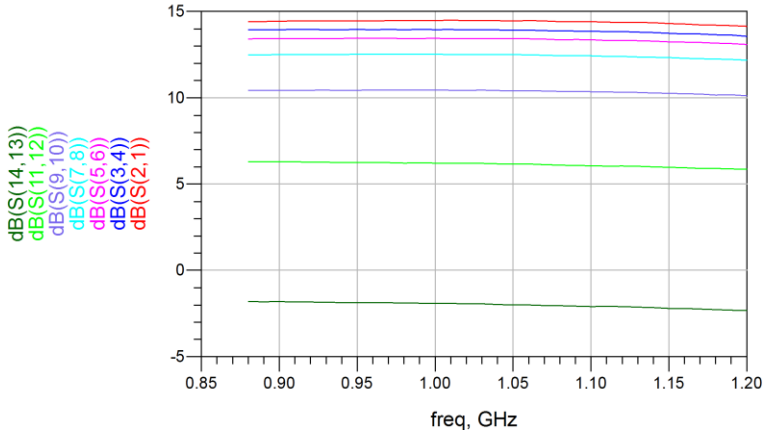


TGV interposer for 2.5D RF integration(3/3)

- TGV interposer based 2.5D integrated RF receive **module function test**



Wave beam No.1 attenuation state test results

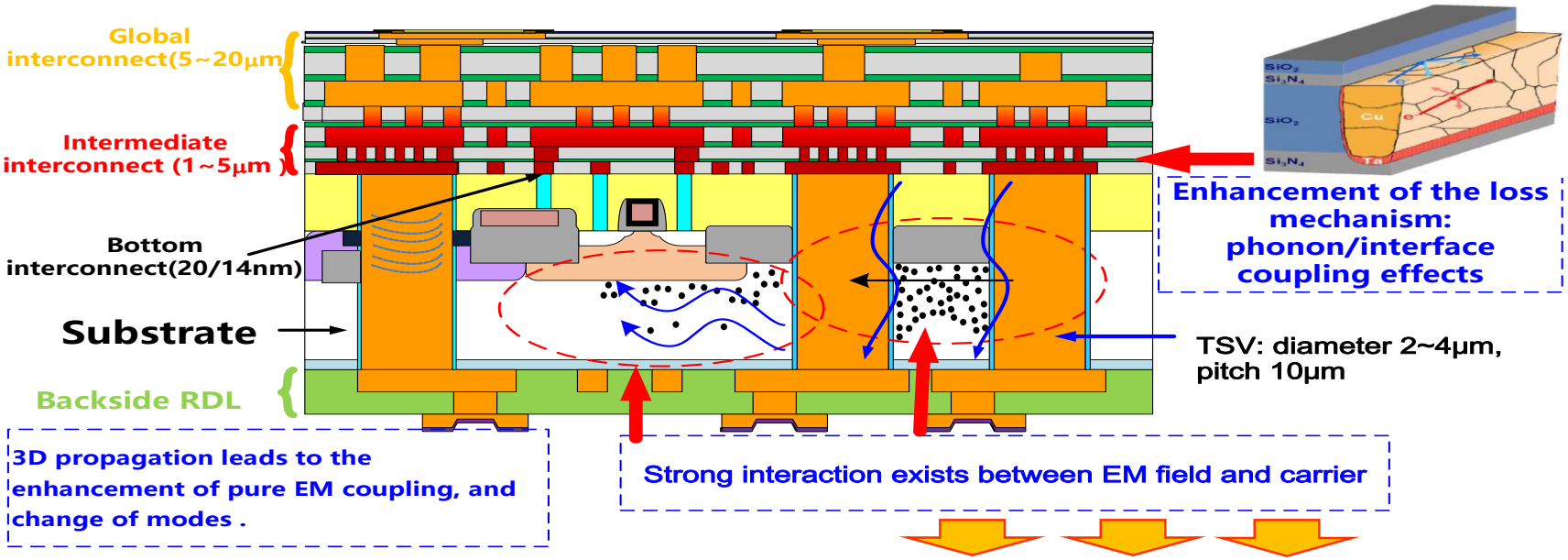


Wave beam No.2 Attenuation state test results

Test results of TGV interposer based 2.5D Receive module

test results(1GHz)	Gain（dB）	Input VSWR	Output VSWR	Phase shift	attenuation state control
Wave beam No.1	14.47	1.61	1.17	work	work
Wave beam No.2	14.46	1.6	1.17	work	work

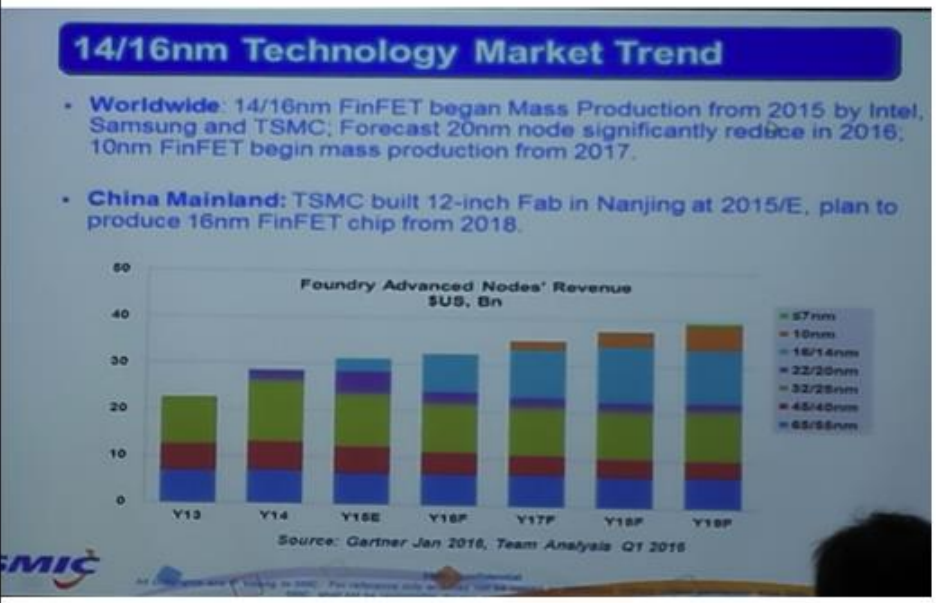
Part 2: 3D Packaging For 20/14nm IC



New problems with TSVs embedded in semiconductor!

- At 20/14nm node, the cross-scale effect of the 3D integrated system is significant, and modeling methods with both efficiency and precision need to be proposed.

Research Directions

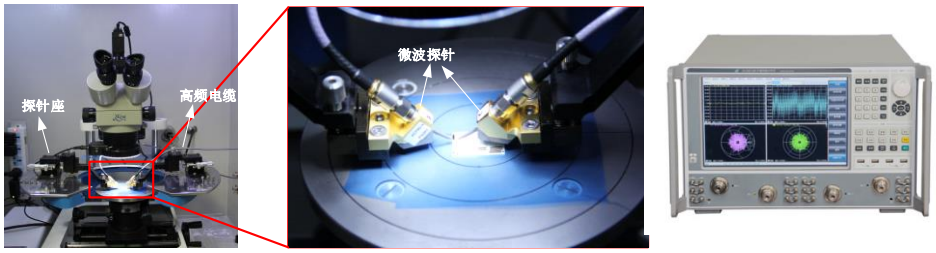


Discussion with industries,

- New phenomena of electromagnetic wave propagation in 3D cross-scale interconnects
- Cross-scale electromagnetic modeling and Simulation of 3D interconnects
- High-quality information transmission method and functional structure design

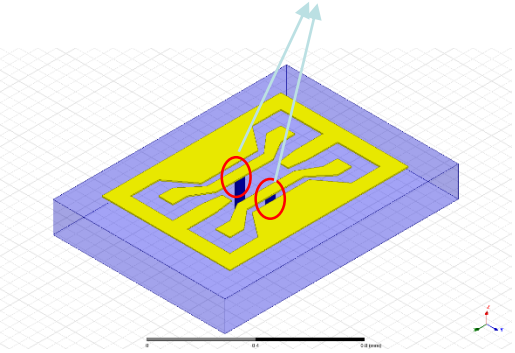
TSV characteristics test for 20/14nm IC interconnection

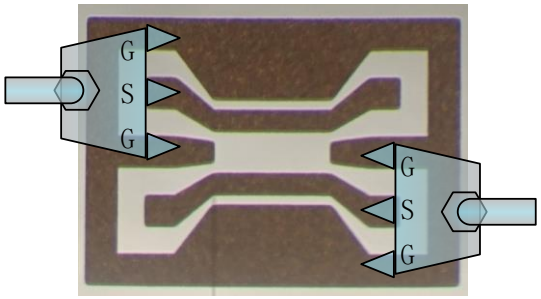
- Measurement setting
  - CETC 41 AV3629 VNA + Cascade probes
  - SOLT calibration ,
  - Frequency: 0.1GHz~67GHz
  - DUT
  - Case Study: V diameter 40μm, height 130μm
  - N-type substrate 1000Ω·cm

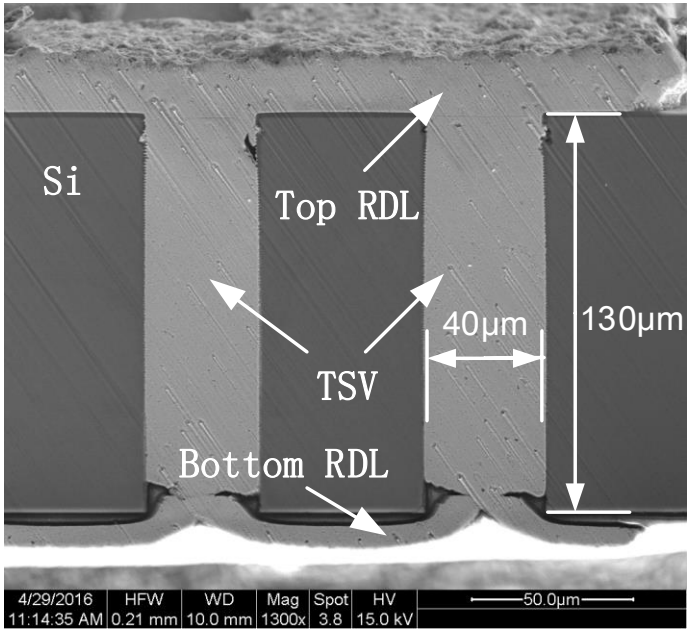


Test Set-up

TSV pair pitch 160μm







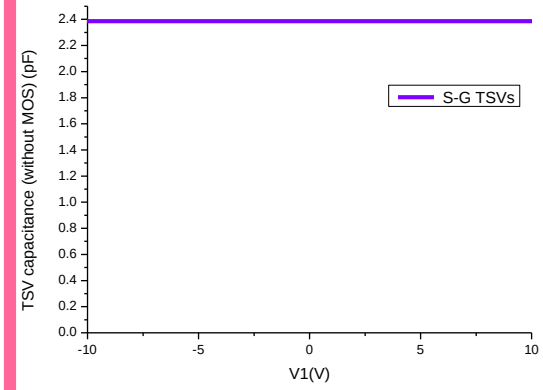
A typical test samples

2.1 An accurate analytical model of TSV coupling capacitance is first proposed (TED)

TSV oxide capacitance (2009)

1) derived from parallel wire model

2) validated by electromagnetic field simulation



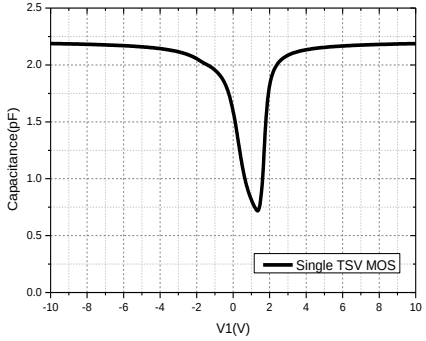
Savidis I, Trans. on Electron Device,2009.

Single TSV MOS capacitance (2011)

1) derived by solving Poisson's equations

2) validated by TCAD or measurement

3) C-V characteristics

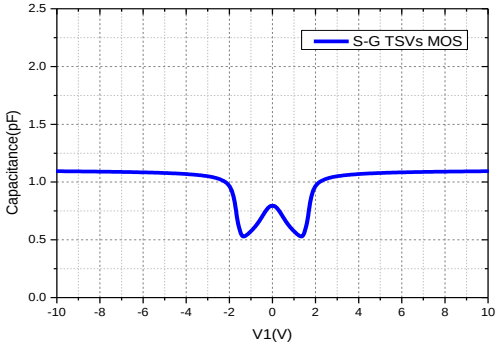


Bandyopadhyay T, Trans on CPMT, 2011.

S-G TSV MOS capacitance model (our group) (2015)

1) Based on the theory of electromagnetic filed / carrier coupling and the analytical model of MOS capacitance\

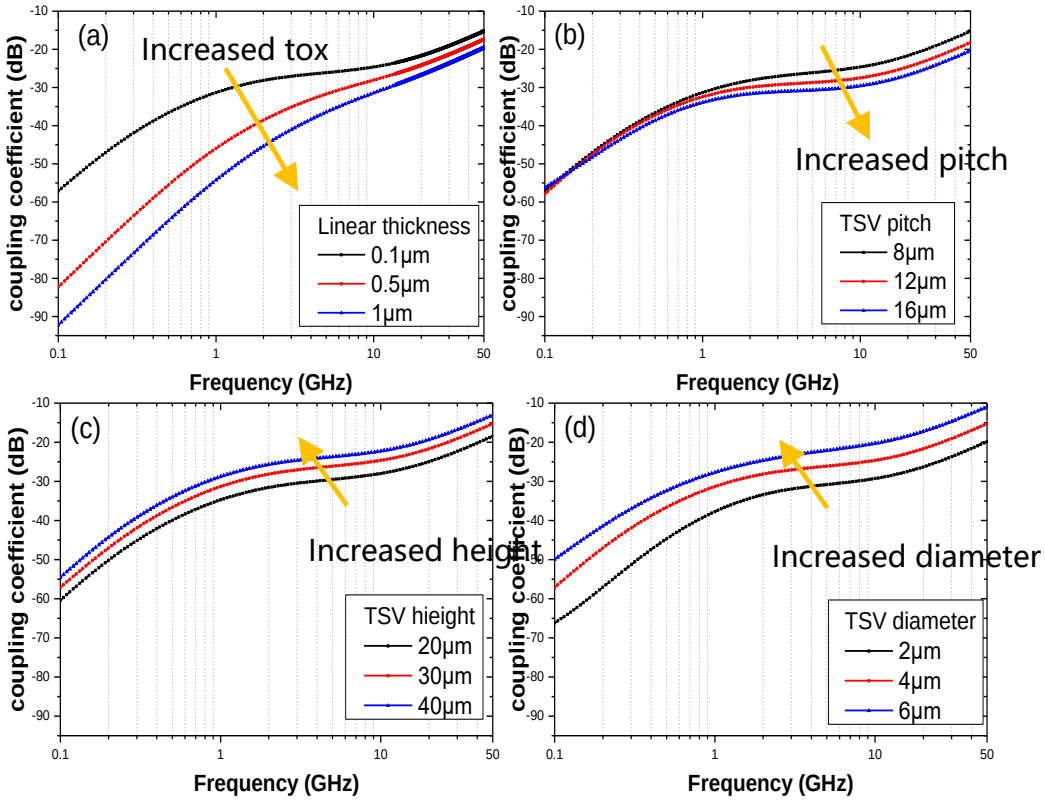
2) validated by measurement



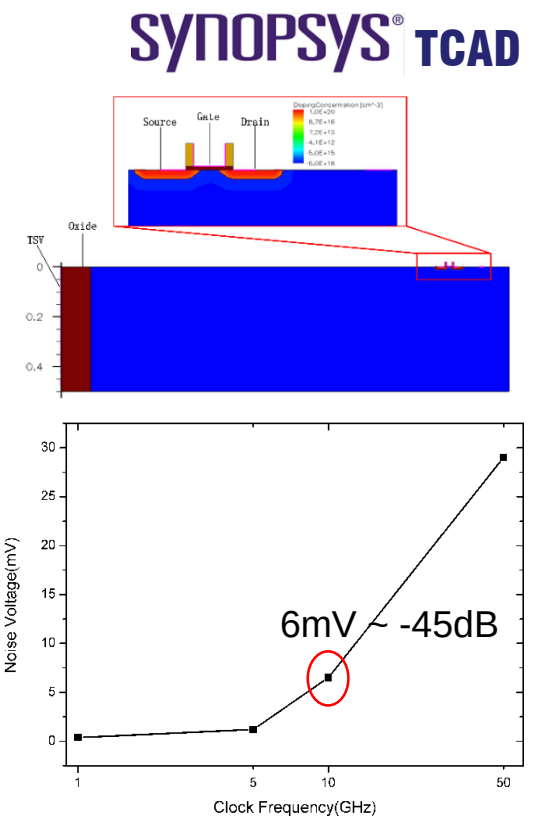
Electron Devices, IEEE Transactions on, 2015, 62(12): 4161-4168.

Research Advancements

2.2 Analyzed noise coupling characteristic between TSV and active device at 20/14nm node



Influence of structural parameters on TSV-TSV coupling coefficients

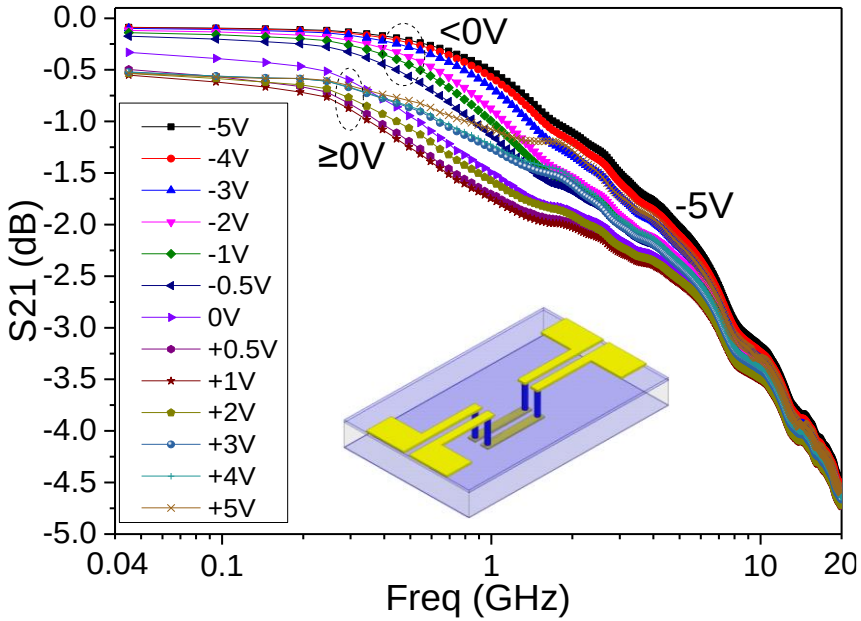


TSV-device coupling simulation with TCAD

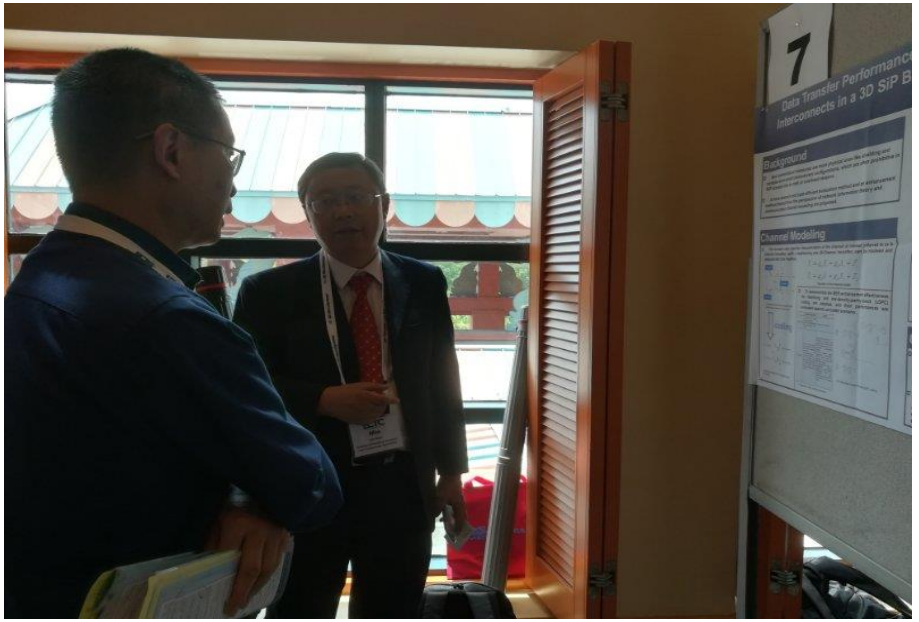
Published @ AIP Advance

2.3 **Verified the influence** of bias voltage on information transmission by experimental results

- At a bias voltage under 0V, transmission characteristics become better, as the signal TSV is in depletion or inversion state. When bias is greater than 0V, characteristics are only slightly improved
- Bias mainly affects characteristics at frequency range less than 5GHz



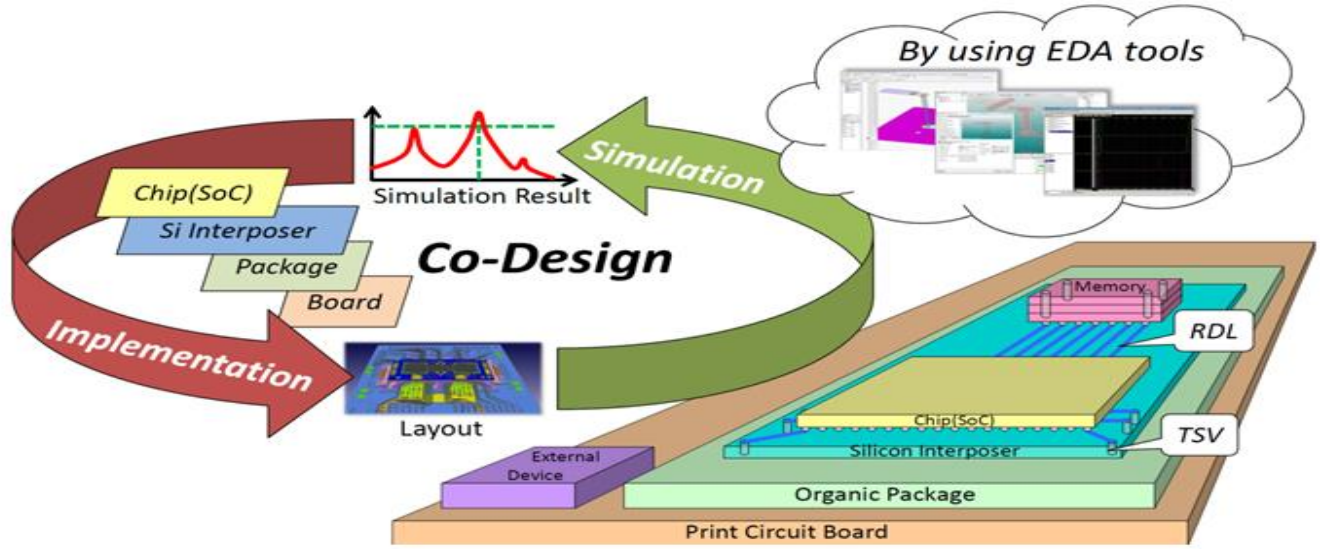
Transmission characteristics of GS-type and GSG-type 3D interconnects



Present @ ECTC 2017

Potential applications

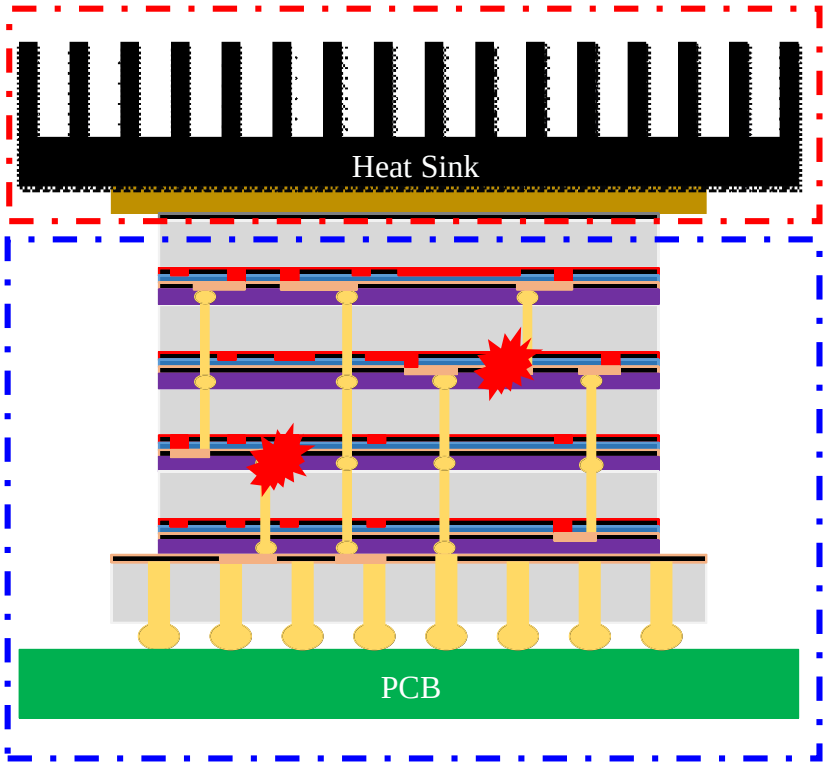
- Integrated into EDA tools to optimize design methodologies of 3D integration system
- Increase yield and reduce costs of TSV thus promoting industrial applications of 3D integration system based on TSV



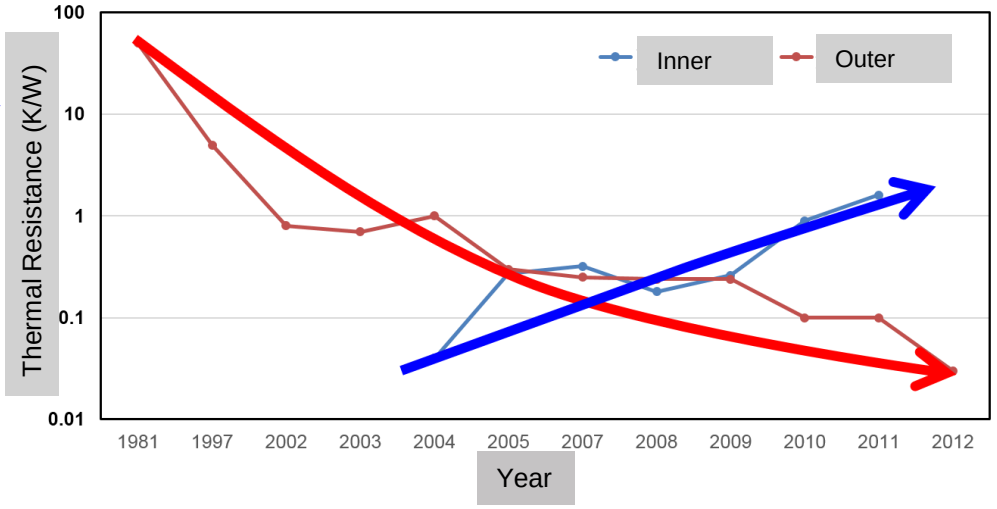
A sample design flow of 3D integration system

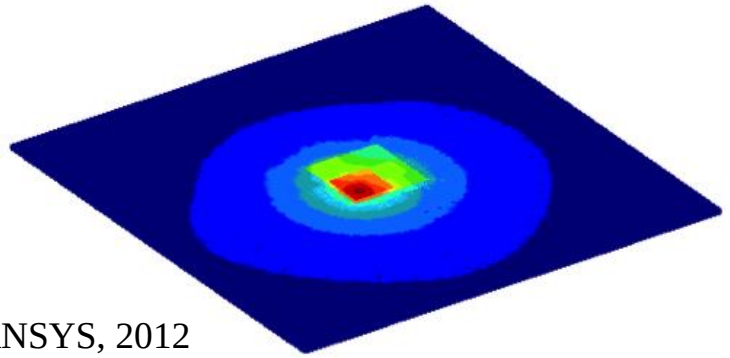
Part 3: Thermal management for 3D Stacked IC

1st: Outer Resistance ↓ Inner Resistance ↑



2nd: Hot-spot problem arises



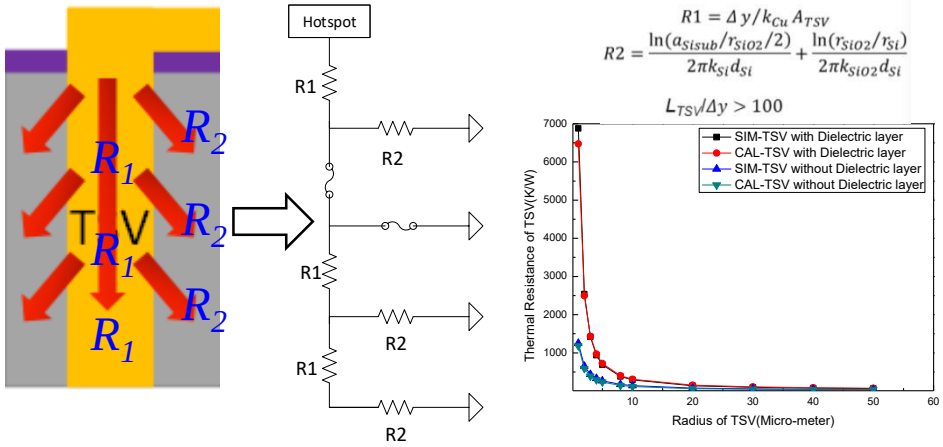


ANSYS, 2012

Hot-spot caused by smaller feature size, temperature map of memory and Logic on Silicon Interposer.

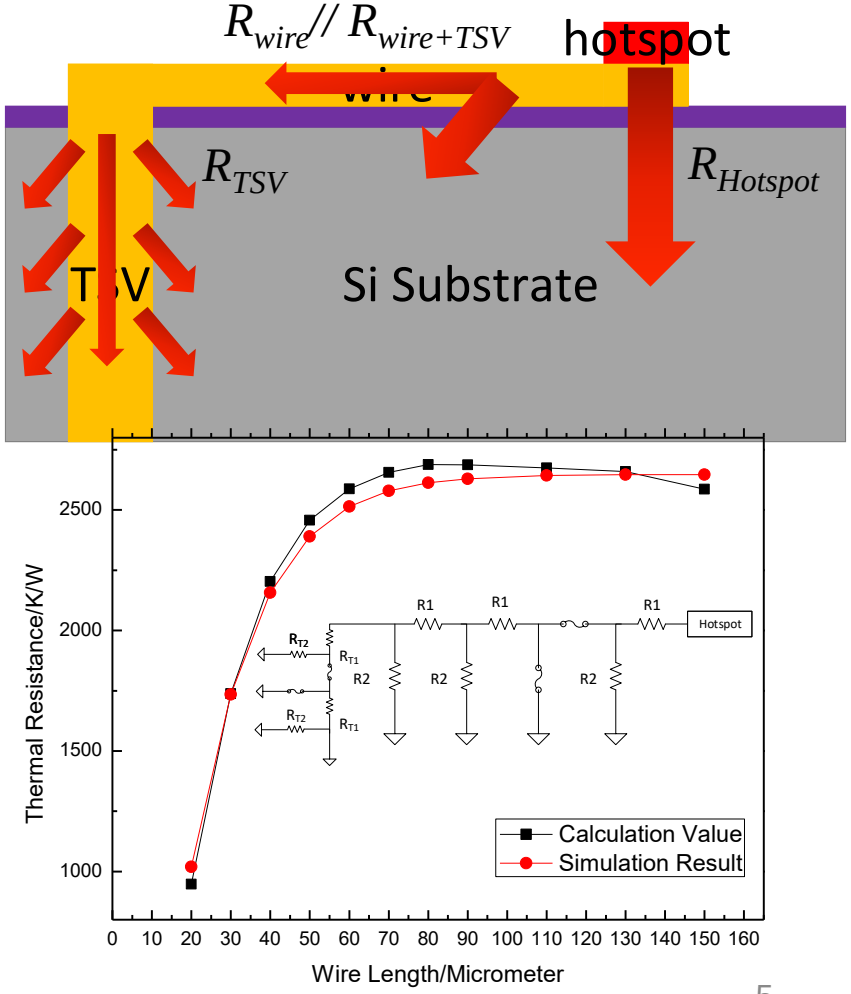
3.1 Proposed an accurate calculation method on thermal effectiveness

With accurate thermal model of TSV and wire, temperature excess of whole chip decreases by 26% compared with old model



Thermal resistance of TSV in Si Substrate

- Thermal Resistance Network of HCP (High Conductivity Path)

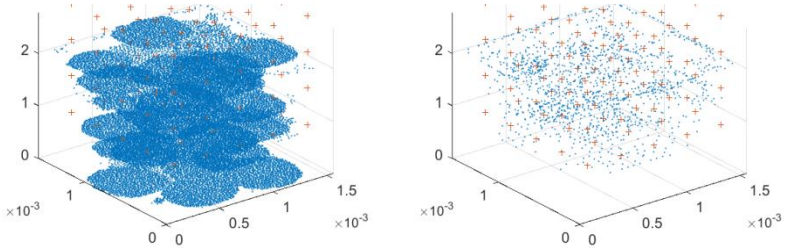


Yudan Pi, Yufeng Jin et, al. An Accurate Calculation Method on Thermal Effectiveness of TSV and Wire, EPTC 2016.

3.2 Study on fast & low computation consumption model

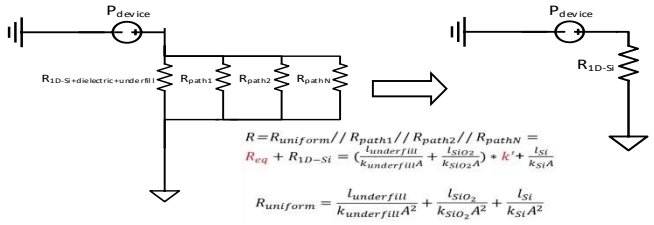
A demo 3D system with 1566 TSVs and 80504 hotspots is successfully simulated within 24 min

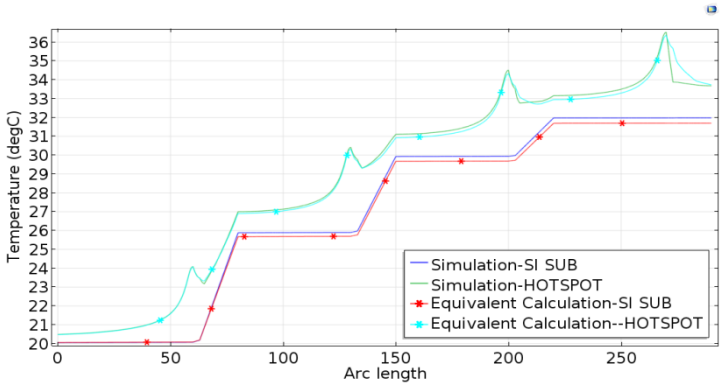
➢ System Level Calculation

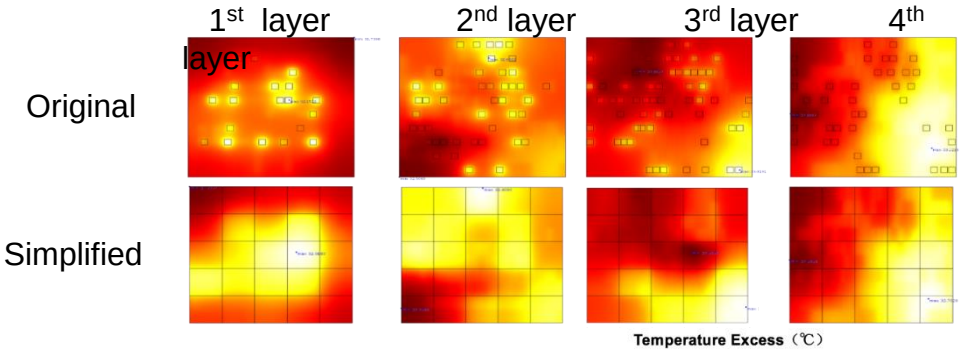


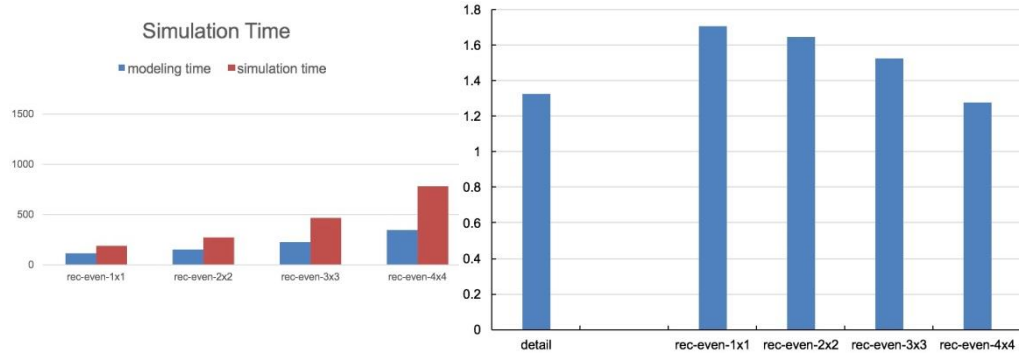
Hot-spot & TSV Distribution

➢ Thermal Conductivity Equivalence





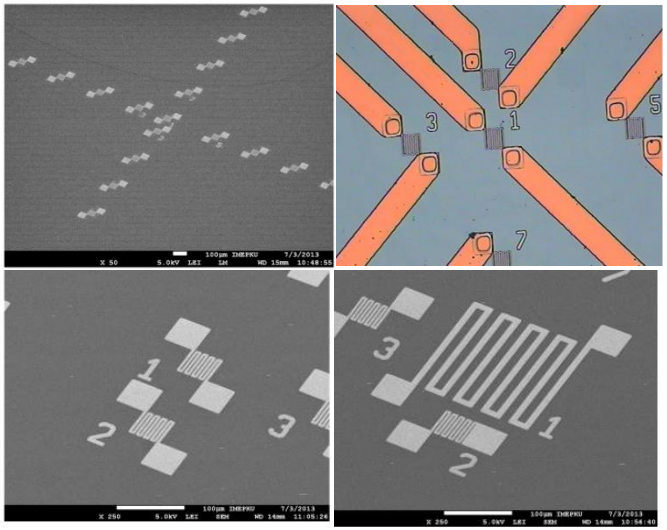




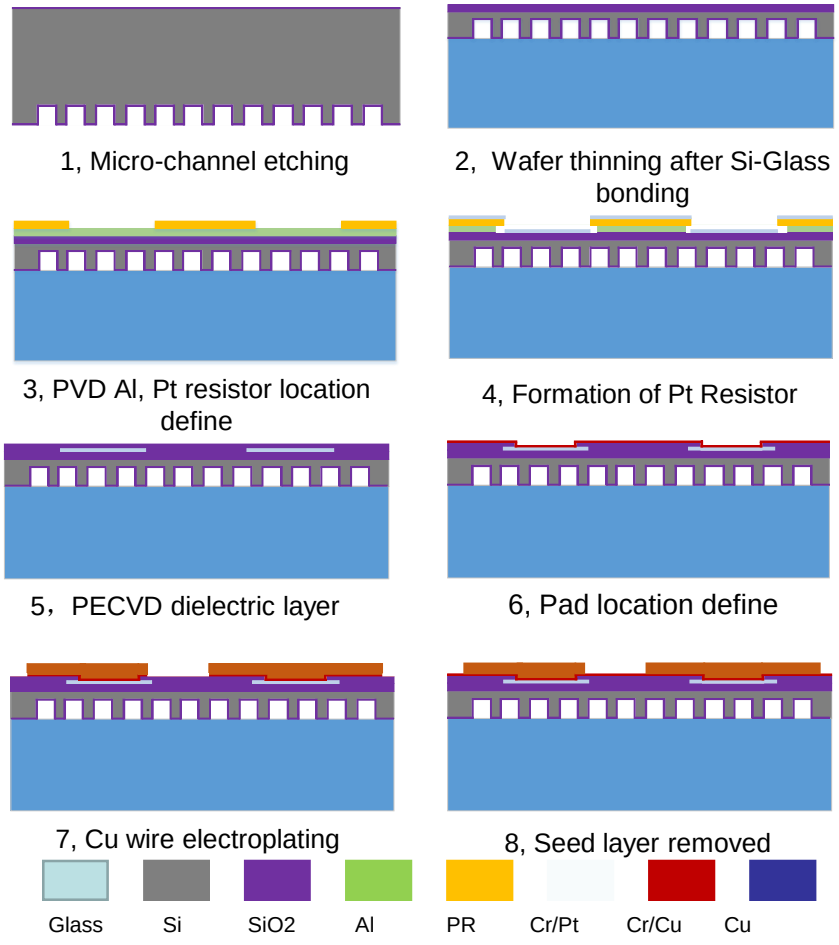
1. Yudan Pi, Yufeng Jin et, al. **A fast and low computation consumption model** for system-level thermal management in 3D IC, ECTC 2016.
2. Ningyu Wang, Yufeng Jin et,al. "**A full chip scale numerical simulation method** for thermal management of 3D IC," ICEPT2016.
3. Ningyu Wang, Yufeng Jin et,al. "Equivalent Thermal Conductivity Model Based **Full Scale Numerical Simulation** for Thermal Management in Fan-Out Packages," ECTC 2017

3.3 Novel micro-cooling for distributed hot-spots

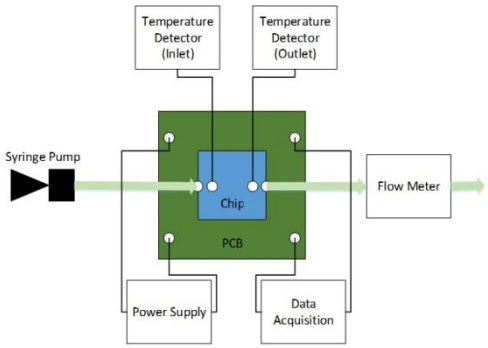
➢ Chip Design



➢ Fabrication process

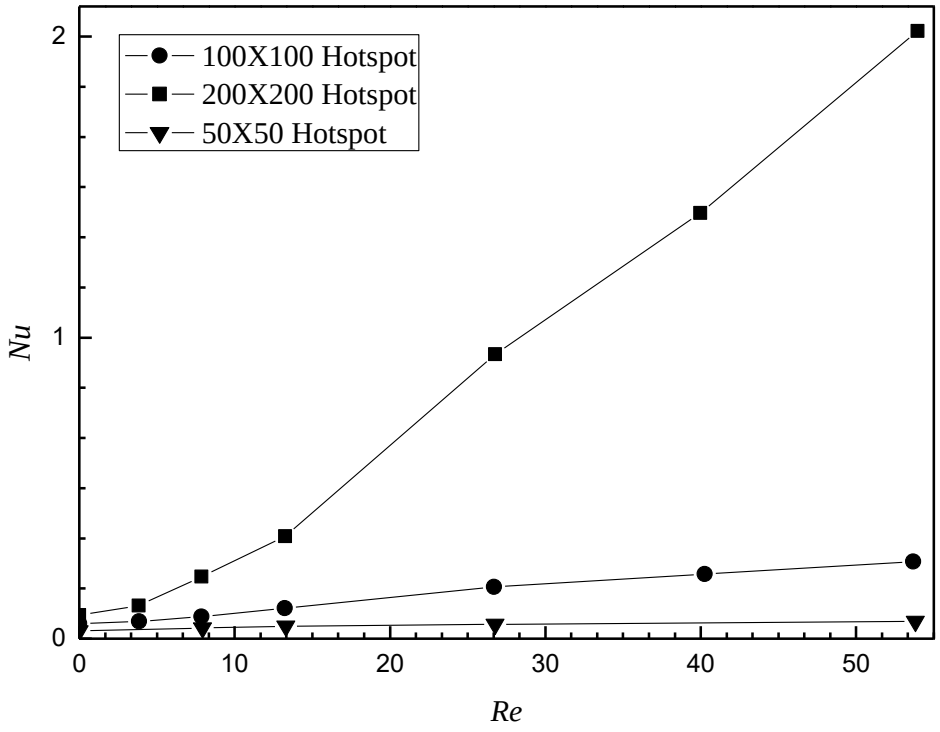


➢ Experiment Setting

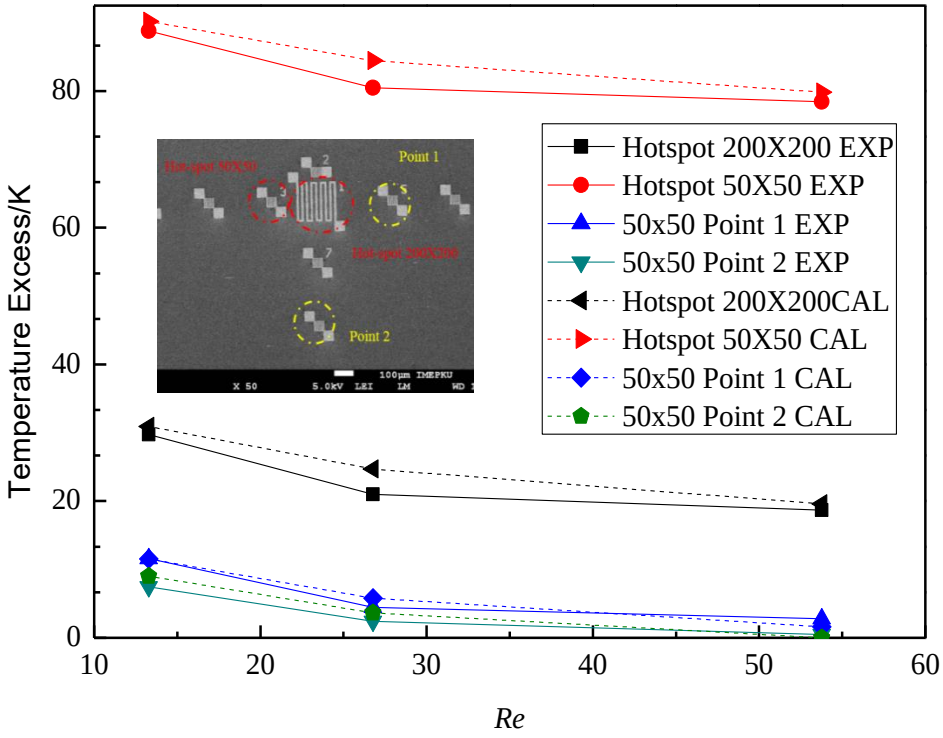


Micro-cooling method for distributed hot-spots

- Re~Nu varies with hot-spot size



- Temperature estimation



CAN BE APPLIED IN MICRO-COOLING OPTIMIZATION AND THERMAL SIMULATION.

1. Liu Kun, Yufeng Jin et, al. A preliminary experimental validation of superposition strategy in thermal management of integrated circuit with multiple hot-spots, SCI CHINA 2014.
2. Yudan Pi, Yufeng Jin et, al. **Microfluidic cooling for distributed hot-spots, ECTC 2016**..

Part 4: packaging for multi-sensor application (smart sensor system)

1970s

2000s

2010s

In the future

Smart phone with multi-sensor included,

Our changing life

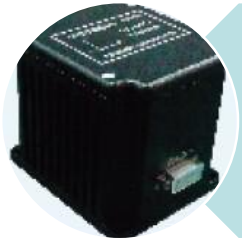
Multi-sensor electronics:

More functions, higher performance, lower cost

Case study: Posture Detection System

Tilt Sensor

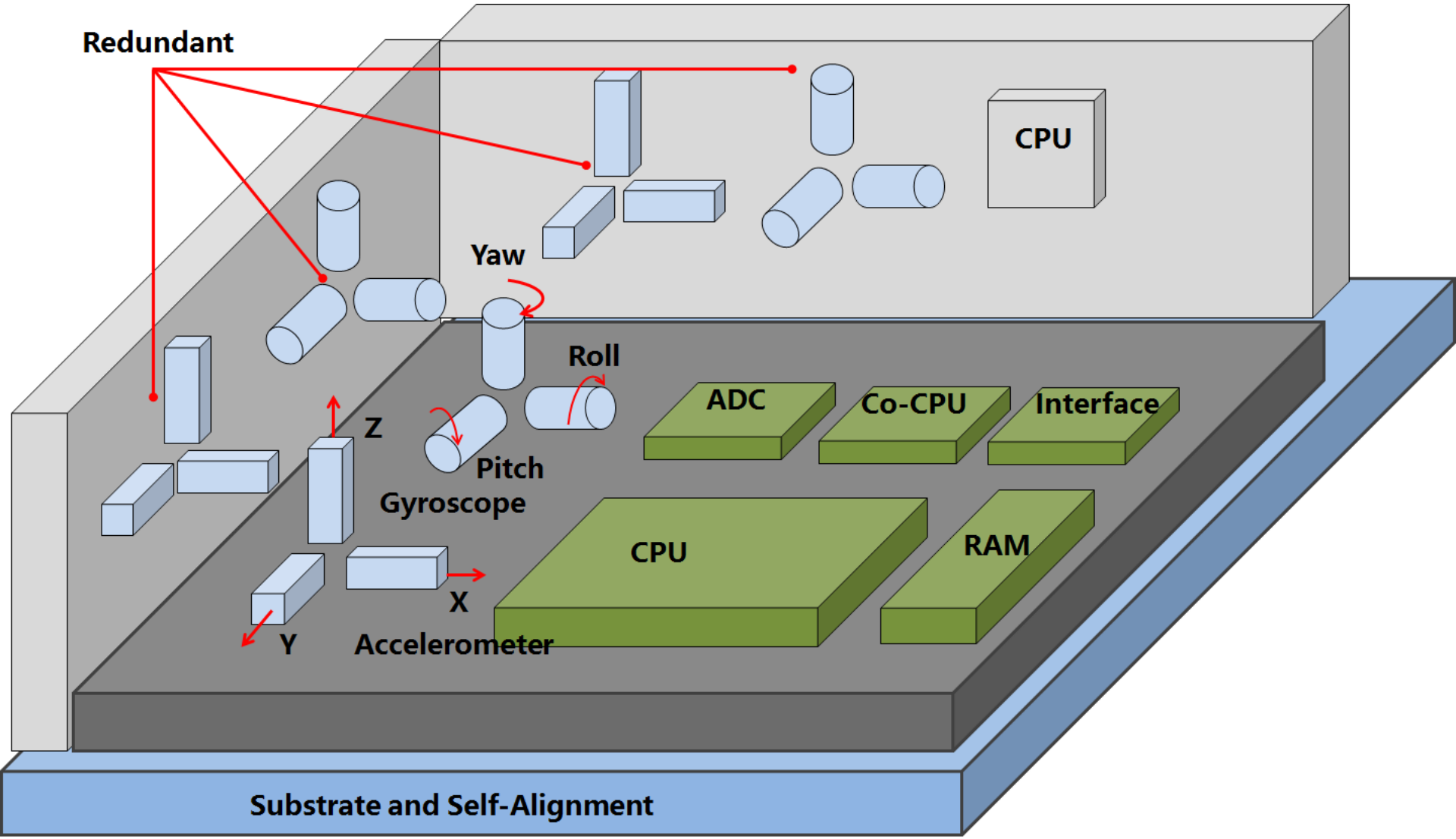
Compass



AHRS

AHRS Attitude and Heading Reference System

Schematic system structure



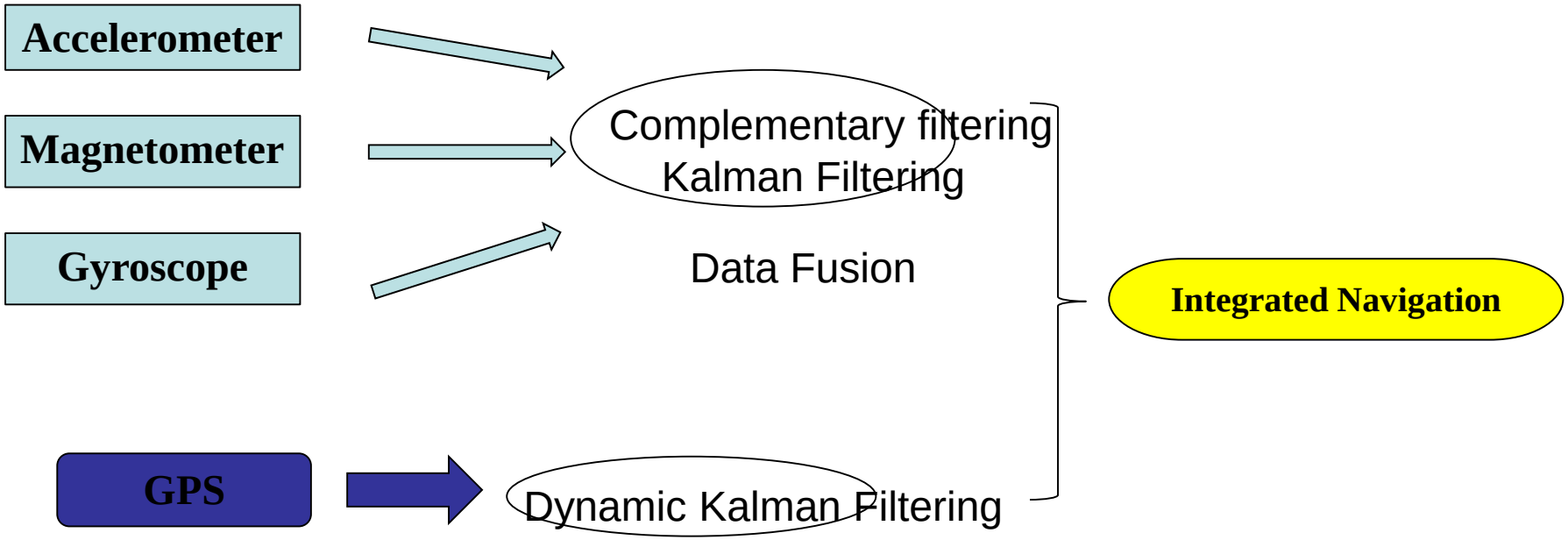
Packaging & Integration technologies developed

Hardware Integration:

- Redundant design
- Integration of MEMS sensors and ICs
- High accuracy calibration
- Self-alignment and adjustment in assembling

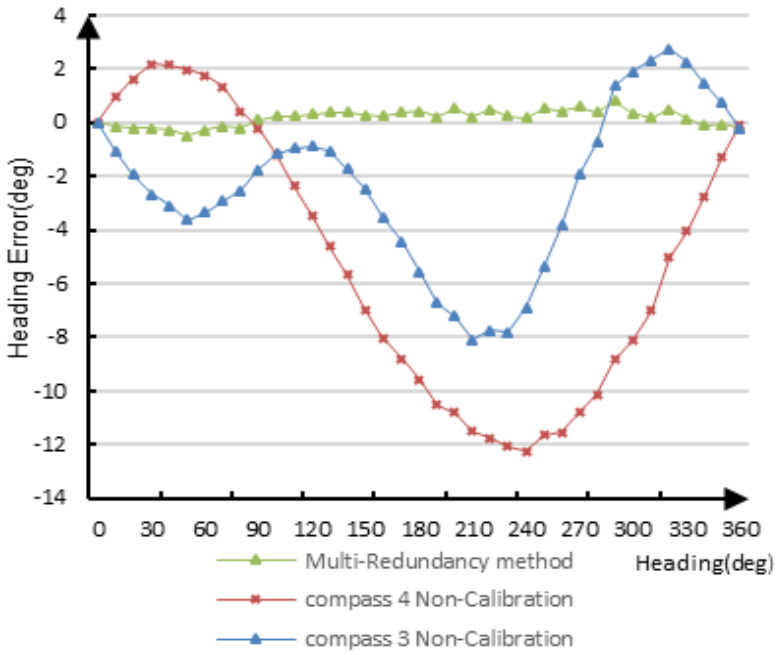
Software (Algorithm and modeling):

- Multi-layer Kalman filter
- Adaptive filter
- Cross-error correction
- GPS-IMU hybrid filter
- Installment error correction


Accelerometer
Magnetometer
Gyroscope
GPS
Complementary filtering
Kalman Filtering
Data Fusion
Dynamic Kalman Filtering
Integrated Navigation

Experiments for different applications

	Three Axes Direction of the Compass			The Value of Three Axes		
Serial number	X	Y	Z	X	Y	Z
1	north	east	down	X1	Y1	Z1
2	south	west	down	X2	Y2	Z2
3	north	west	up	X3	Y3	Z3
4	south	east	up	X4	Y4	Z4
5	east	down	north	X5	Y5	Z5
6	west	up	north	X6	Y6	Z6
7	west	down	south	X7	Y7	Z7
8	east	up	south	X8	Y8	Z8
9	up	north	west	X9	Y9	Z9
10	down	south	west	X10	Y10	Z10
11	up	south	east	X11	Y11	Z11
12	down	north	east	X12	Y12	Z12



The Calibration Sequence of 12-Position Experiment

The heading error of the compass

7 graduated students will present the progress at 2017 IEEE Real-time Computing & Robotics

- 6 Series, 150 type of tilt sensing products developed

- Digital compasses, Dynamic tilt sensors and AHRS

HEC375 磁性连续测斜仪

三维，精度0.5°，里程可调，输出RS232/RS485

SEC225 二维电子罗盘

二维，精度+/-1°，里程可调，输出RS232/TTL/485

HEC365V 高精度全姿态三维电子罗盘

三维，精度0.3°~0.5°，里程可调，输出RS232/RS485

HEC360 全姿态三维电子罗盘（裸板）

三维，精度0.3°~0.5°，里程可调，输出RS232/RS485

SEC385倾角补偿式三维电子罗盘80°

三维，精度0.5°，里程可调，输出RS232/RS485

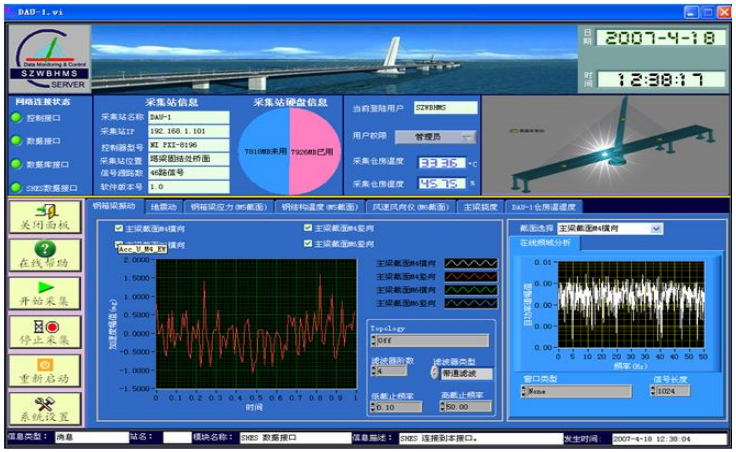
SEC380倾角补偿式三维电子罗盘(80°裸版)

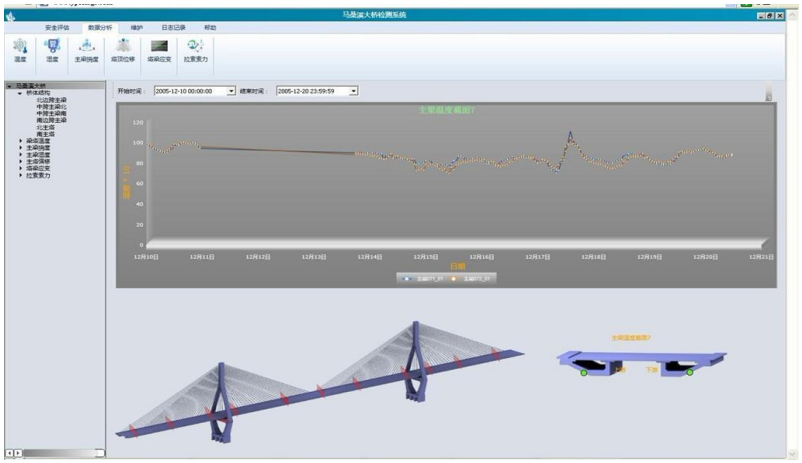
三维，精度0.5°，里程可调，输出RS232/RS485

2000 customers, Many applications from Asian and European countries

Application 1-Bridge Surveillance

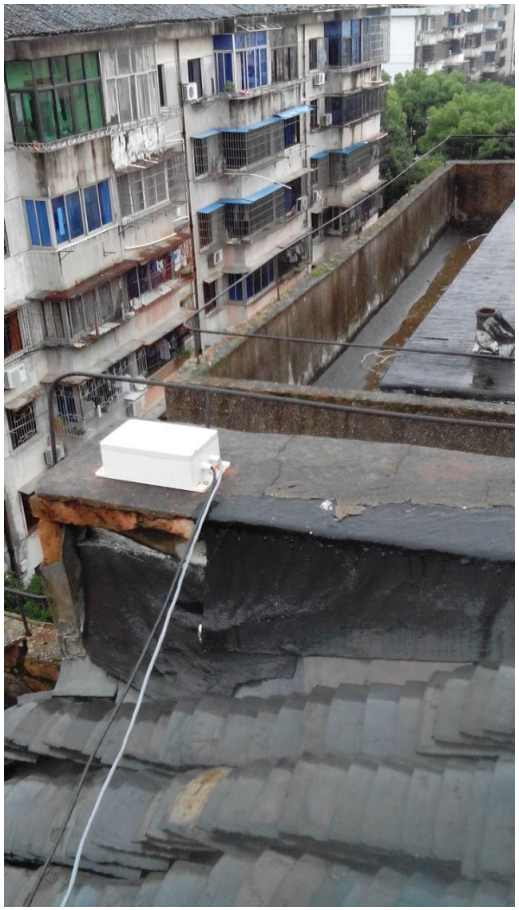
The sensors can be put under bridges and test the changing of the bridges with wireless transmission and computing interface at center.





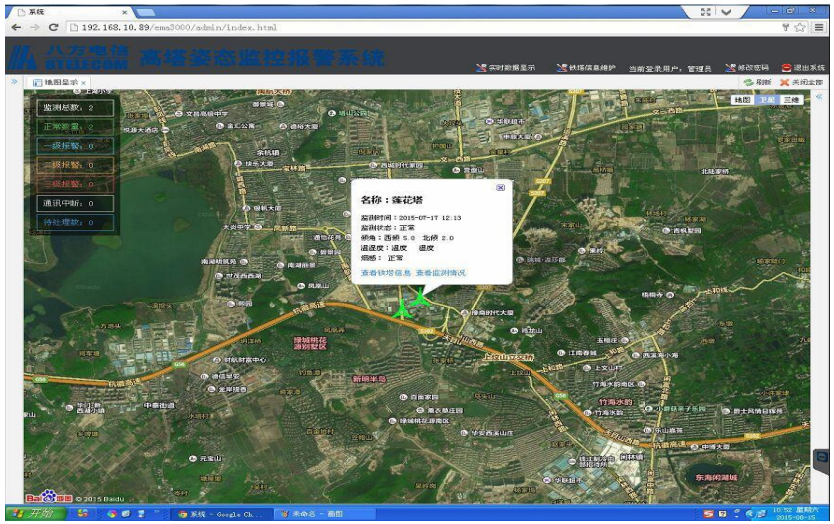
Application 2-Building Surveillance

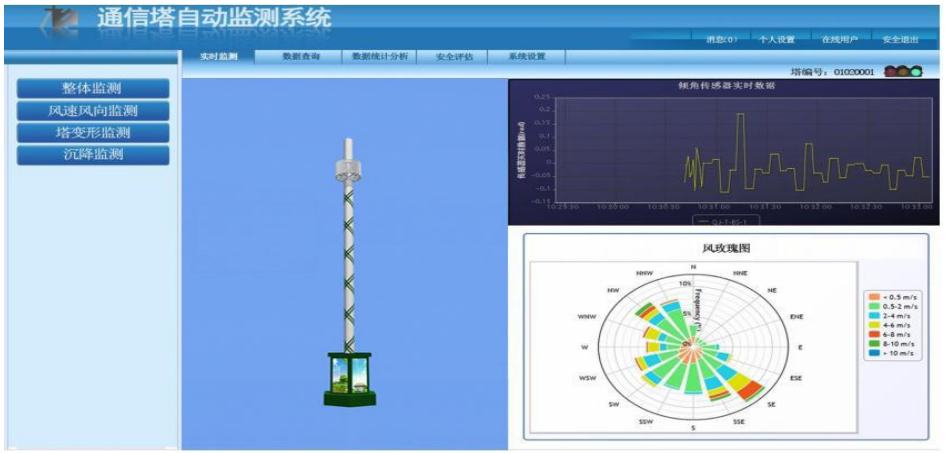
Same application like building surveillance for old building or ancient ones.



Application 3- Tower Safety

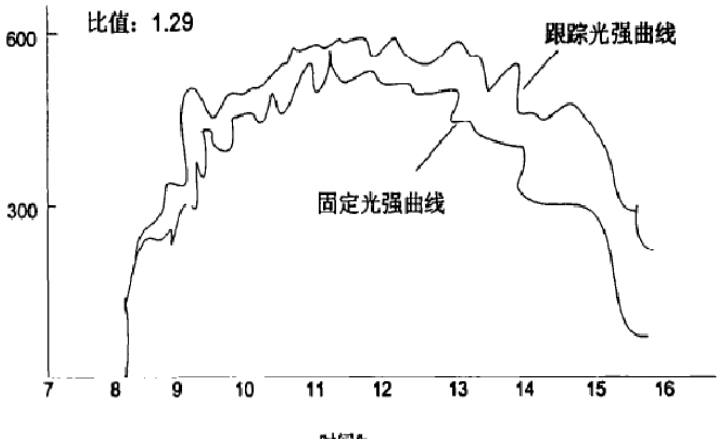
The tall tower for power supplier need real time surveillance for the safety of the signal

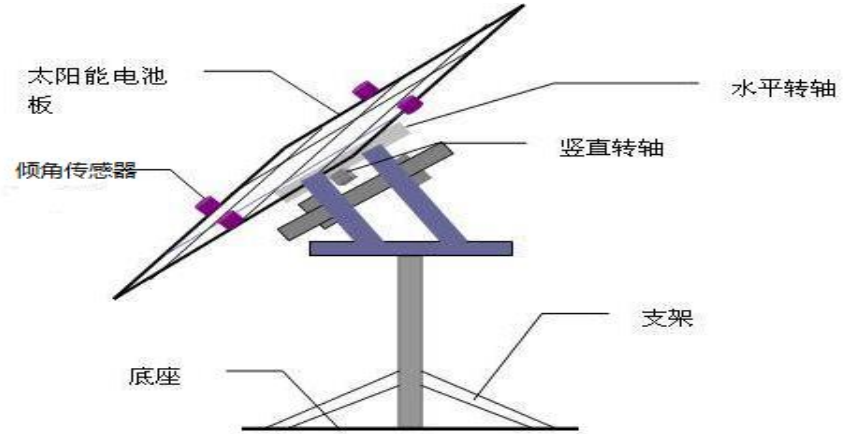


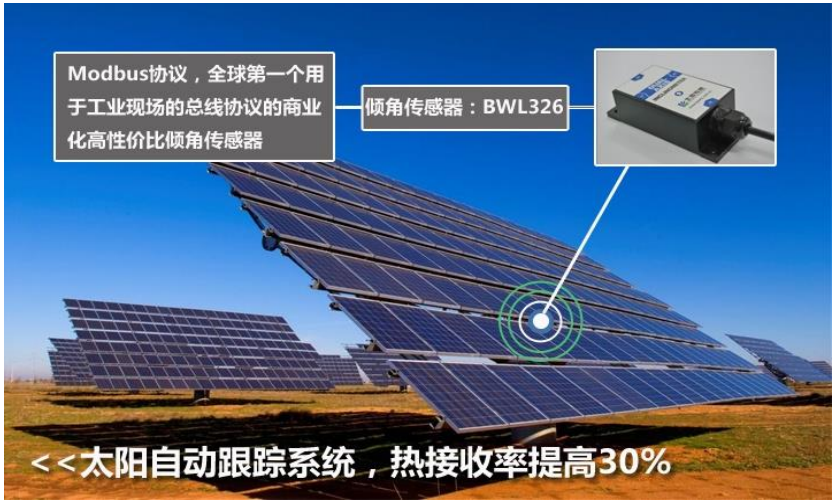


Application 4-Sun Tracking System

Solar energy system need tilt control which will gain better efficiency of the system.





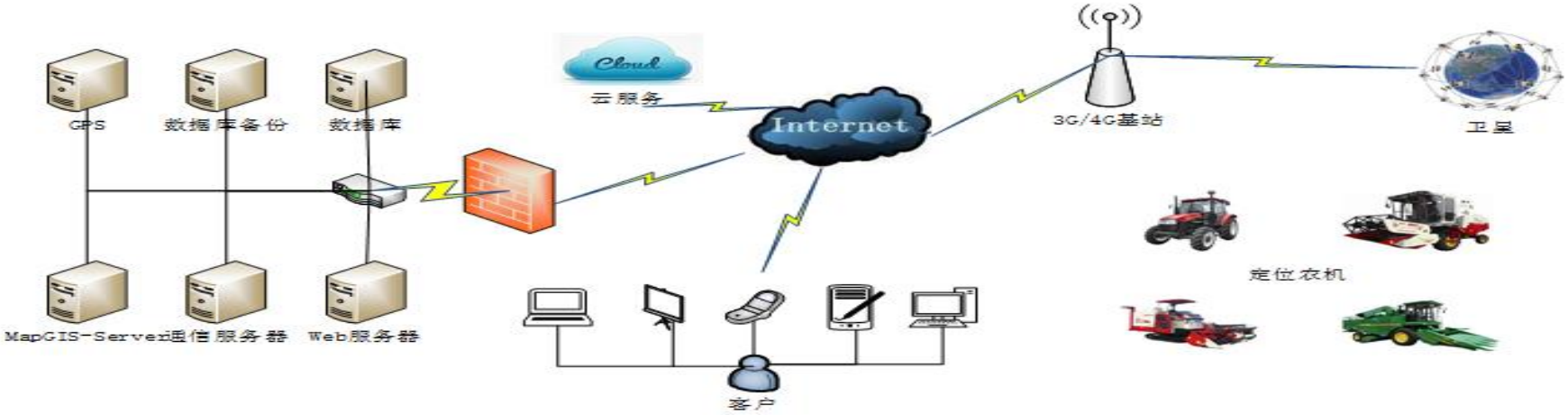


Application 5-Industry Machines

For machines automation control and posture adjustment, tilt sensor offer feedback control.

Application 6-Dynamic Tilt Sensors

Some dynamic posture need to be calculate to control the posture of machines



Application 7-AHRS

AHRS can control the AGV or robots for GPS lost systems.

Application 8-Shipment

Ships, Platform and other posture control systems.

Typical Clients

中国船舶重工集团公司
CHINA SHIPBUILDING INDUSTRY CORPORATION

Summary

Exploring advanced packaging technologies in integrated RF module, nanoelectronics, and multi-sensor system

Market is huge, different packaging technologies are needed.

Funding from Industry partners, National Science Foundation, Ministry of Science and Technology of China, Shenzhen Government, and CSC(China Scholarship Council).

Specially thanks to my colleagues and students

AP. Ma SL and Mr. Guan Y for 3D Packaging of RF Module

Prof. Miao M. and Mr. Liu H. for 3D Packaging of 20/14nm IC

Miss Pi YD for Thermal management of 3D Stacked IC

Bewis CEO, Dr. Shi GY for multi-sensor application