Tamper Respondent Envelope Solutions Realized by Additive Manufacturing

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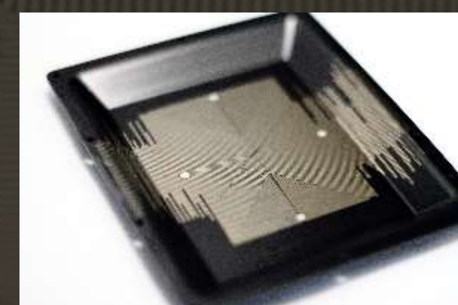
CHEMNITZER SEMINAR
SYSTEM INTEGRATION TECHNOLOGIES

Smart Packaging Solutions for Secure Applications



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Outline

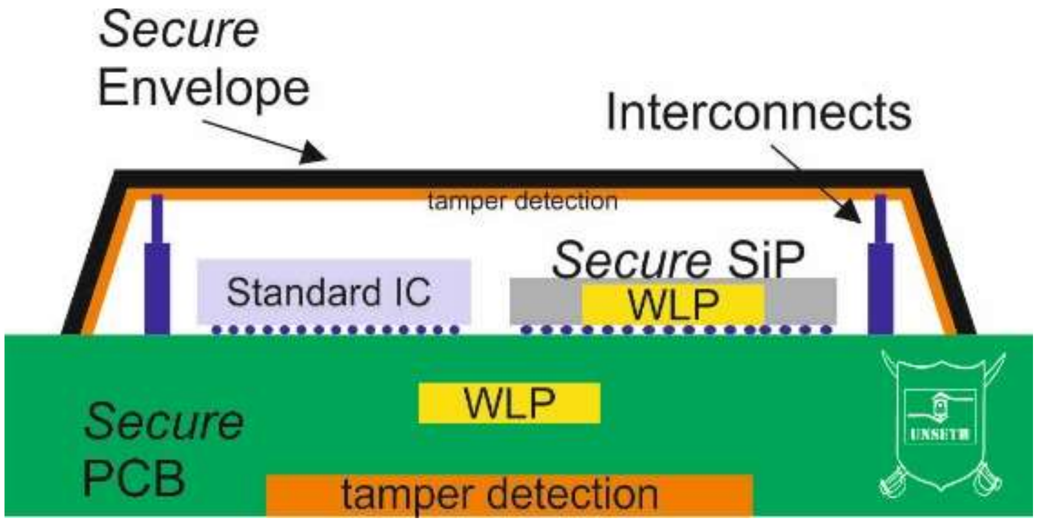
- Motivation for tamper responded envelopes
- Technologies to enable customizable tamper responded envelopes
- Process Chain and build-up insights
- Reliability and security investigations
- Conclusion

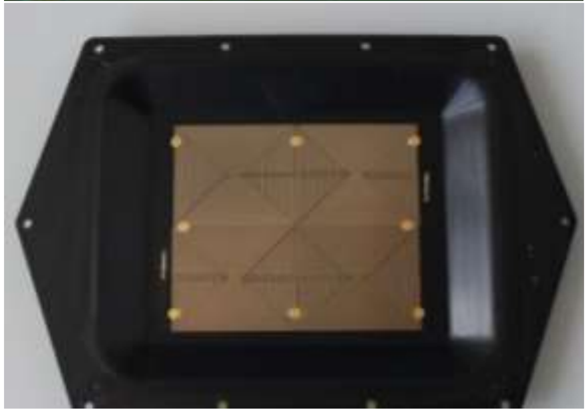
Motivation

Functionalized Packaging Components as tamper responded secure features

A new security tool box for secure electronic systems is introduced by cooperation between

- Thales –System Architecture, Electronic Design, Use Cases and Reliability Characterizations
- AT&S – Embedding of Active and Passive Components into PCB
- Nanium – Secure System in Package Solutions
- Epoche&Espri – Security Evaluation
- **FRAUNHOFER ENAS – Tamper Responded Envelope Solutions**





Combining the Know-How of all partners a novel high-tech security toolbox for electronic systems is presented

Technologies

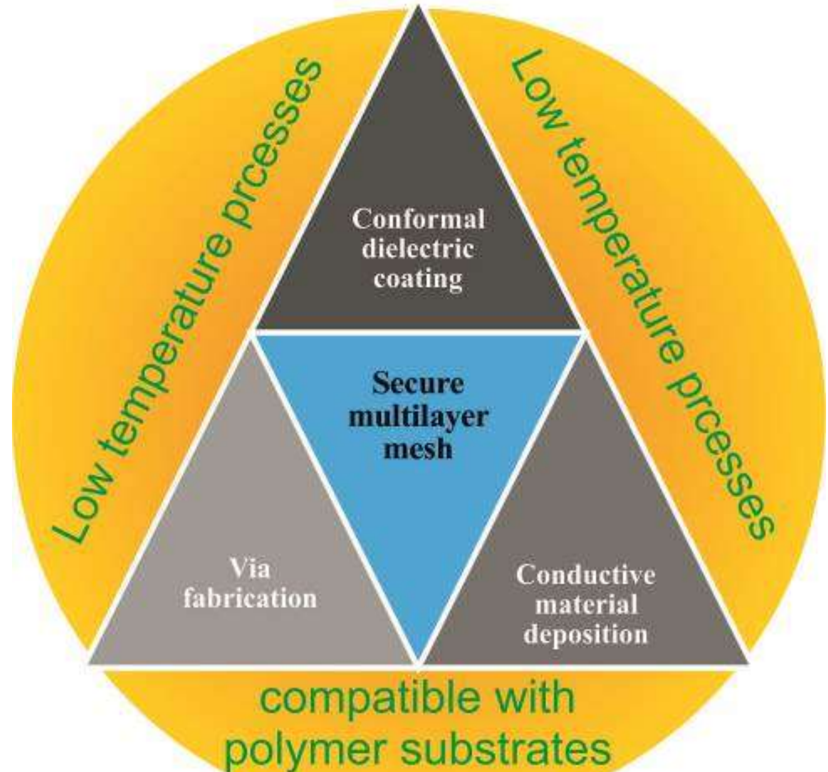
Concept

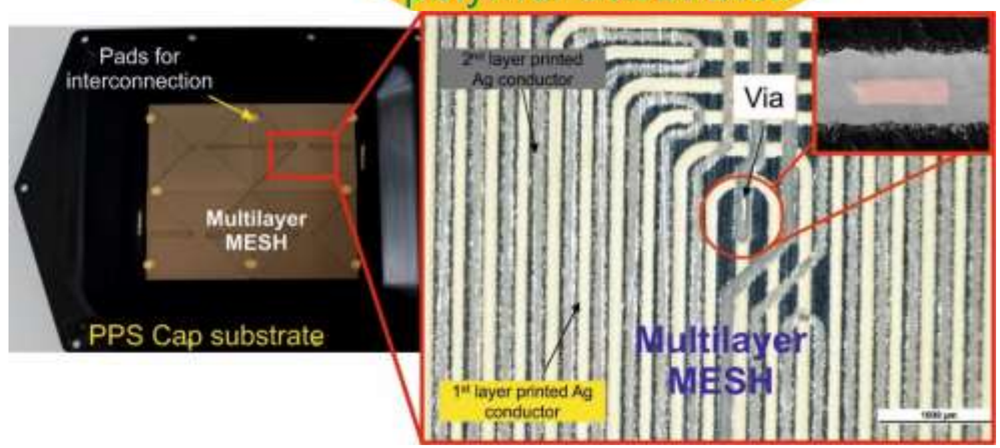
Process development to enable a scalable, **3D ready** process chain capable to fabricate **fine feature tamper detection envelope** solution for electronic system with a **lot sizes from 1-10000 pieces**.

Needed:

- Digital fine pitch, 3D ready deposition process for conductive materials
- Conformal dielectric coating technology for 3D substrates
- Process for via fabrication to enable a multilayer mesh approach

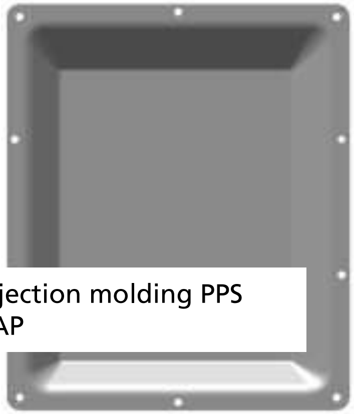
Low temperature processes < 150°C to enable the usage of sensitive / polymer / low cost substrates





Technologies

Concept & Process flow (schematic)



Injection molding PPS CAP

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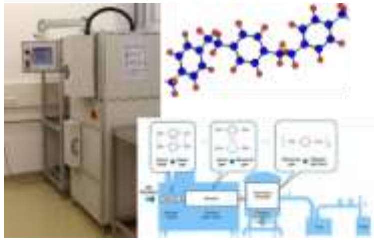
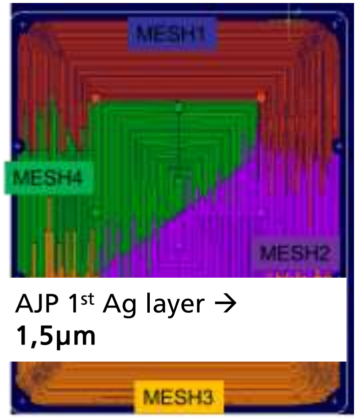


Thin film encapsulation/insulation to build defined surface by CVD –> **~2µm**

\+



AJP 1st Ag layer → **1,5µm**

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Thin film encapsulation/insulation by CVD to passivate 1st Ag layer **(~2µm)** and laser ablation to open vias

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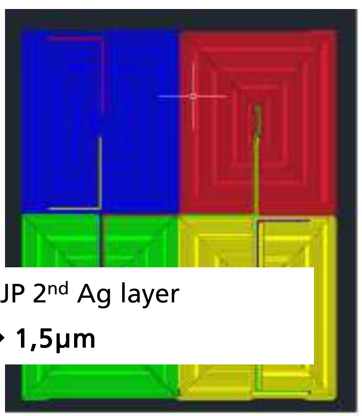
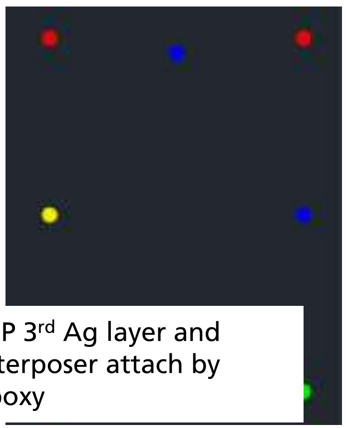


AJP 2nd Ag layer → **1,5µm**

\+

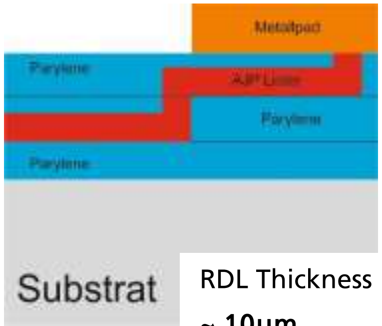
Thin film encapsulation / insulation to passivate 1st Ag layer **(~2µm)** and laser ablation to open vias

\+



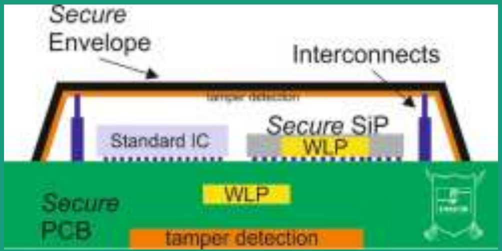
AJP 3rd Ag layer and interposer attach by epoxy

=



RDL Thickness ~ **10µm**

Within UNSETH a **novel process flow** is introduced to fabricate **customized tamper detection** components for electronic packages



Technologies

Aerosol Jet Printing

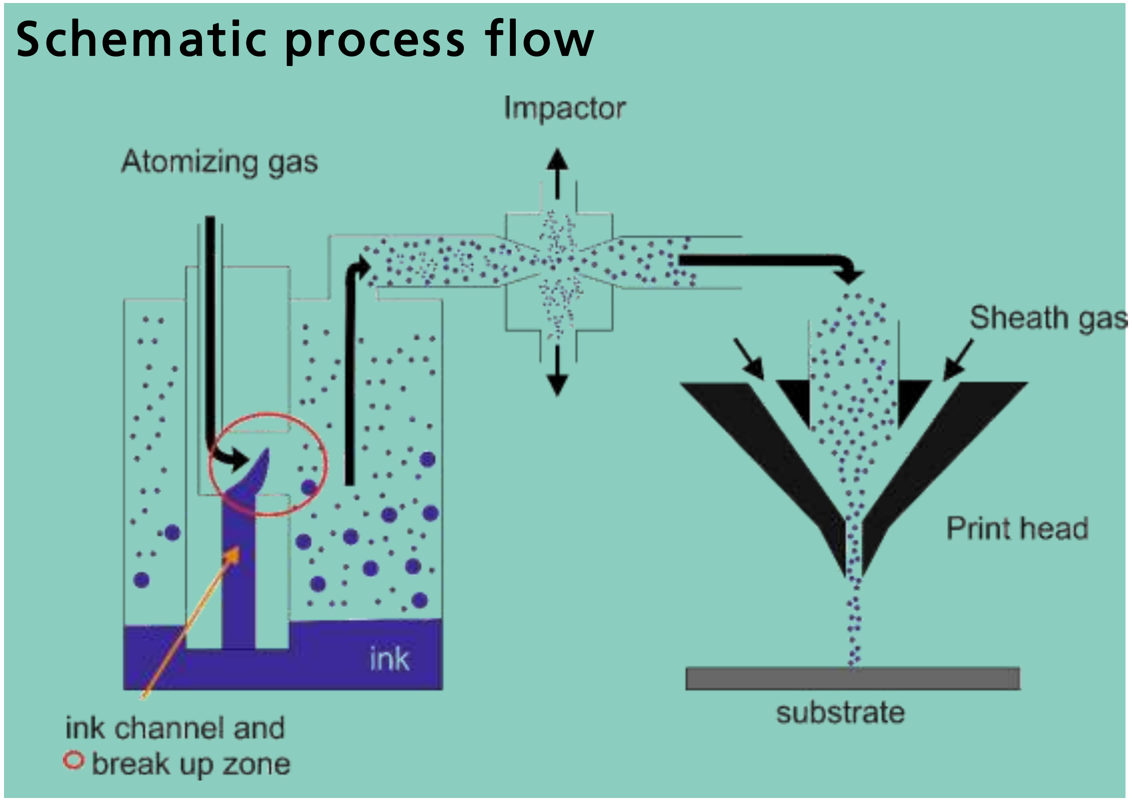
Toolbox

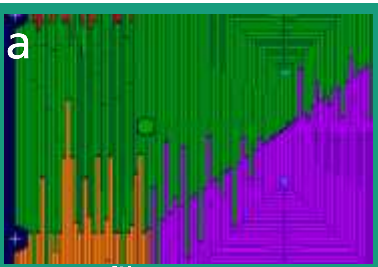
a. Mask: mask less → digital manufacturing using i.e. dxf file

b. Pneumatic or ultrasonic atomizer, impactor, shutter and print head

c. X&Y vacuum table to move the substrate

d. Material: Ink system [colors, insulators, solder, metals, etchants, …]





Layout file

Printhead and shutter

Ink system

Technologies

Aerosol Jet Printing

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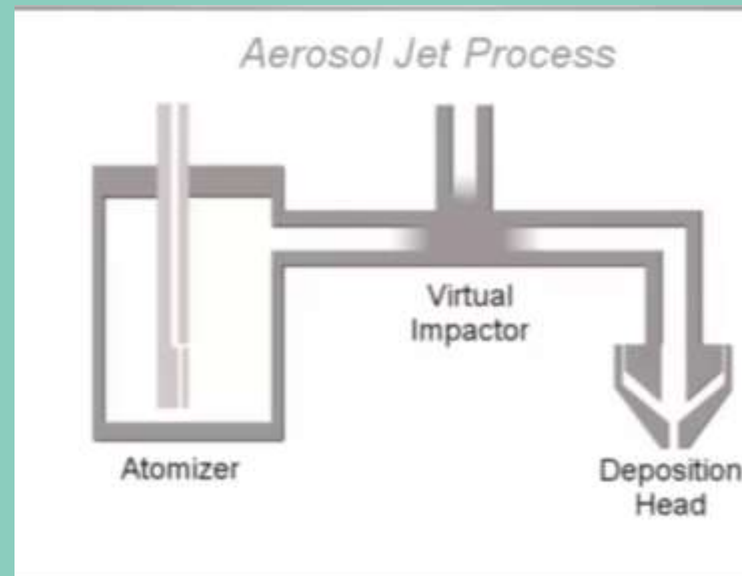
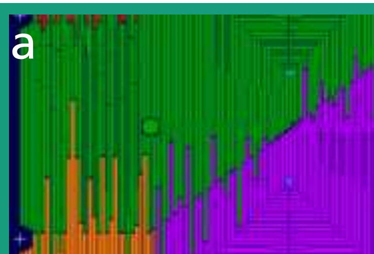
Schematic process flow



Source: Optomec

Aerosol - Jet Toolbox

a

Layout file

b

Printhead and shutter

c


Ink system

Technologies

Aerosol Jet Printing

Toolbox

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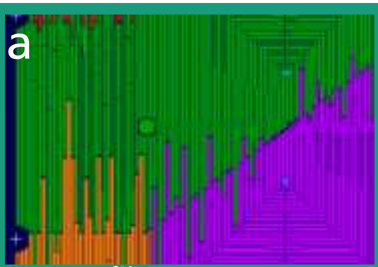
Example / Demo: printing on PCB, overprinting mold

Aerosol - Jet Toolbox



Layout file

Printhead and shutter

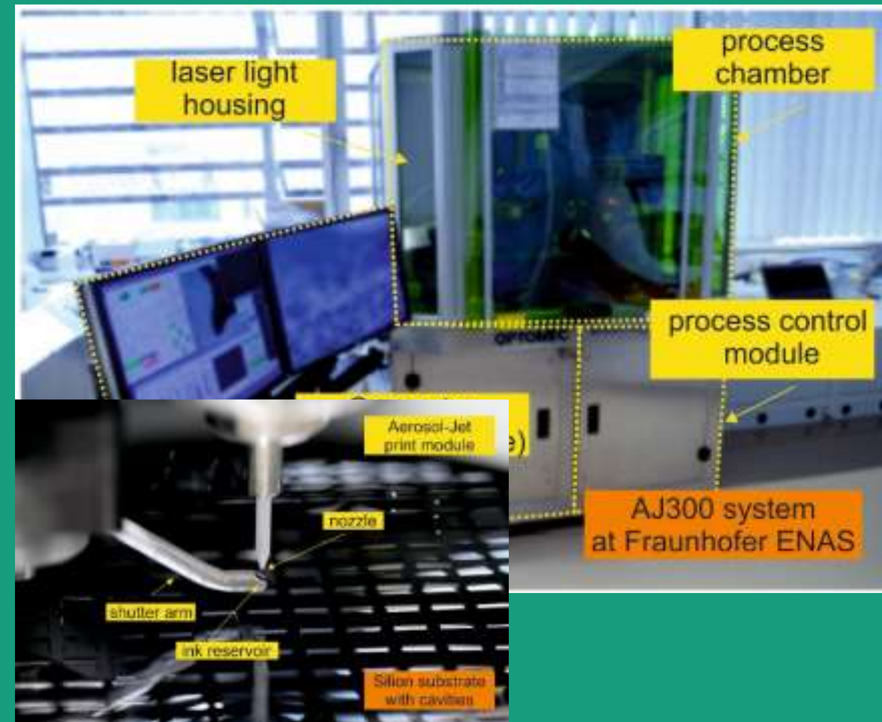
Ink system

Technologies

Aerosol Jet Printing

- 300 x 300 mm x-y-Vacuum stage
- Print Speed: max. 200 mm/s
- 2 Atomizer systems
  - Pneumatic Atomizer [1cP – 1000cP, 15ml fluid]
  - Ultrasonic Atomizer [1cP – 5cP, 1ml fluid]
- Aerosol-, Ink- and substrate heater
- Fine feature print head [min. line width 10 µm]
- Laser-Curing-System [IR Laser, 700mW, 830nm]
- Material in-flight mixing option

Equipment at ENAS



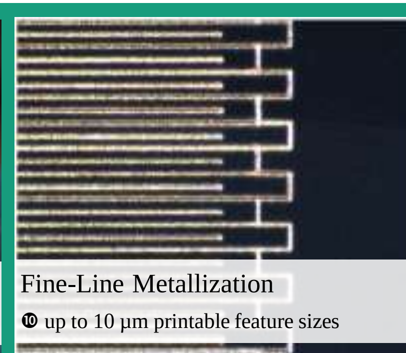
Application Examples

3D Metallization

❿ High resolution Interconnects

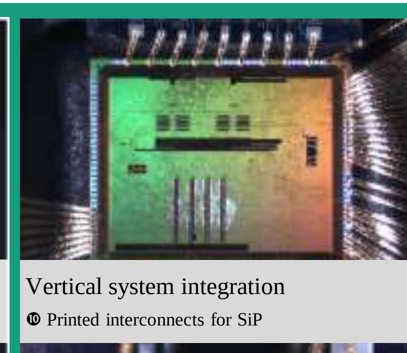
Flexible Packaging

❿ Integration of electrical components



Fine-Line Metallization

❿ up to 10 µm printable feature sizes



Vertical system integration

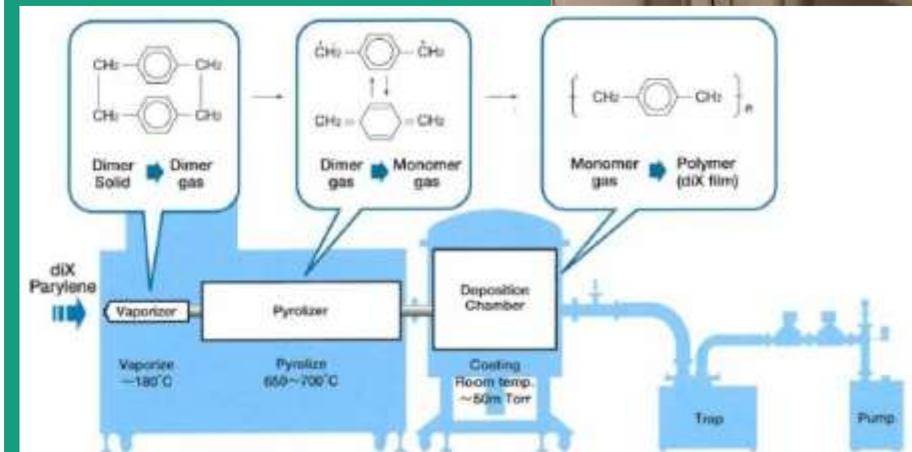
❿ Printed interconnects for SiP

Technologies

Parylene C CVD

- Conformal coating close to room temperature < 5% thickness variation
- Conformal coating for high aspect ratio patterns
- Conformal coating for 3D objects (Chemical vapor deposition)
- Highly transparent (security aspect)
- Good moisture barrier
- Stable $\varepsilon_r \sim 3{,}3$

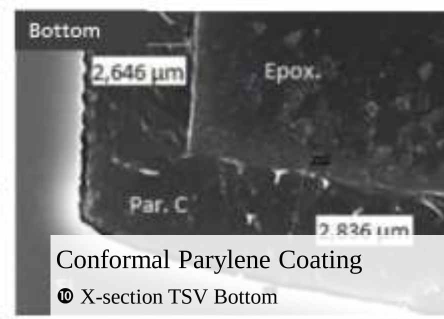
Equipment at ENAS



Properties of Parylene C	
Melting point	290°C
Temperature stability	125°C
Peak Temperature	200°C
Water absorption in 24h	0,06%

Application Examples

Conformal Parylene Coating
⑩ X-section TSV Top

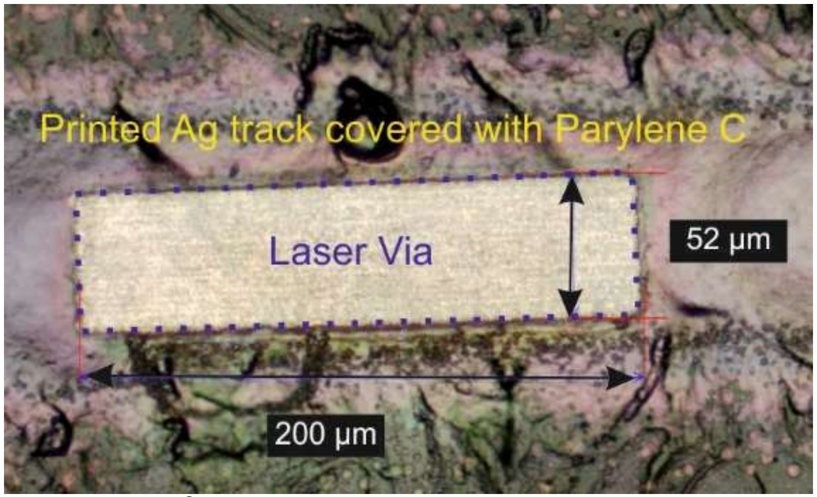


Conformal Parylene Coating
⑩ X-section TSV Bottom

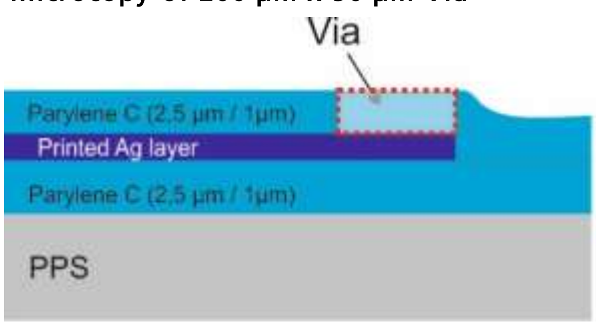
Technologies

Laser Ablation

- 355nm wavelength has been developed for 50 µm x 200 µm vias for 1 µm and 2,5µm thick Parylene C

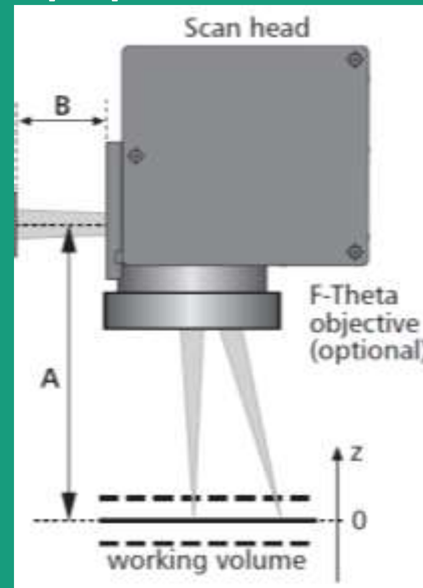


Microcopy of 200 µm x 50 µm Via



Schematic cross section of via process

Equipment at ENAS

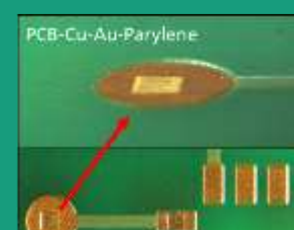


Multi-Wavelenght PS Laser

266nm	355nm	532 nm	1064 nm

Application Examples

µ Fluidic
⑩ patterned glass wafer



PCB
⑩ patterned Parylene on Au

Silicon
⑩ cutting, trechnes, vias

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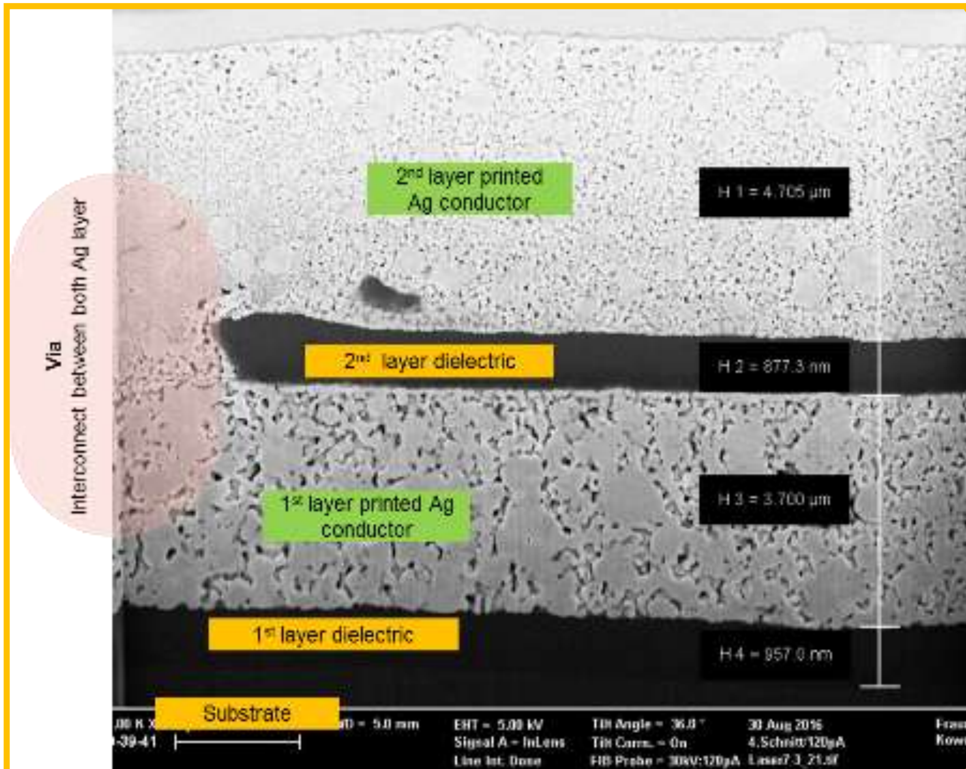
Results

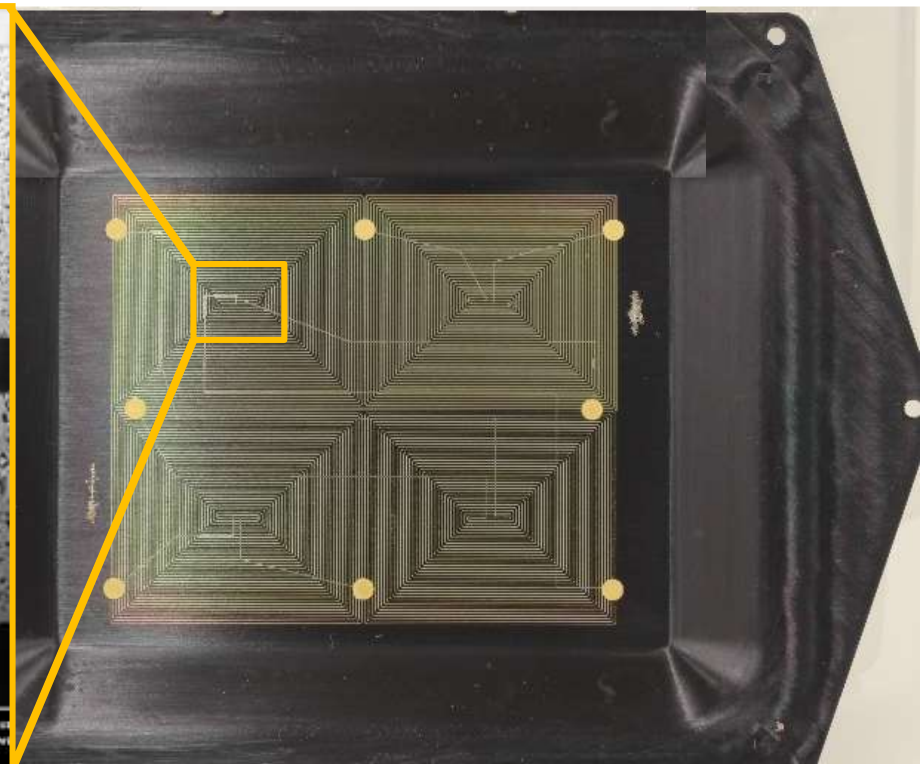
Fabricated Demonstrators

- AJP + Parylene CVD + Laser Via process enables reliable multilayer mesh build

Build up	2 x conductive Mesh layers 2 x dielectric Parylene C layers 1 x via layer
MESH	4 independent loops (each ~ 3m) (Line width ~ 150µm, Spacing ~ 250µm)



FIB cross-sections of via area

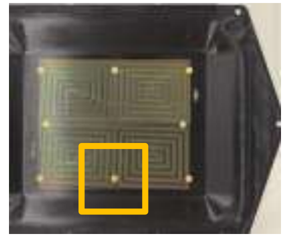


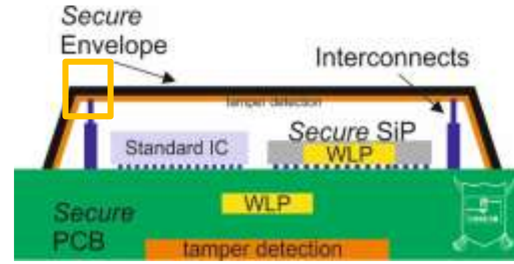
Top View Secure envelope

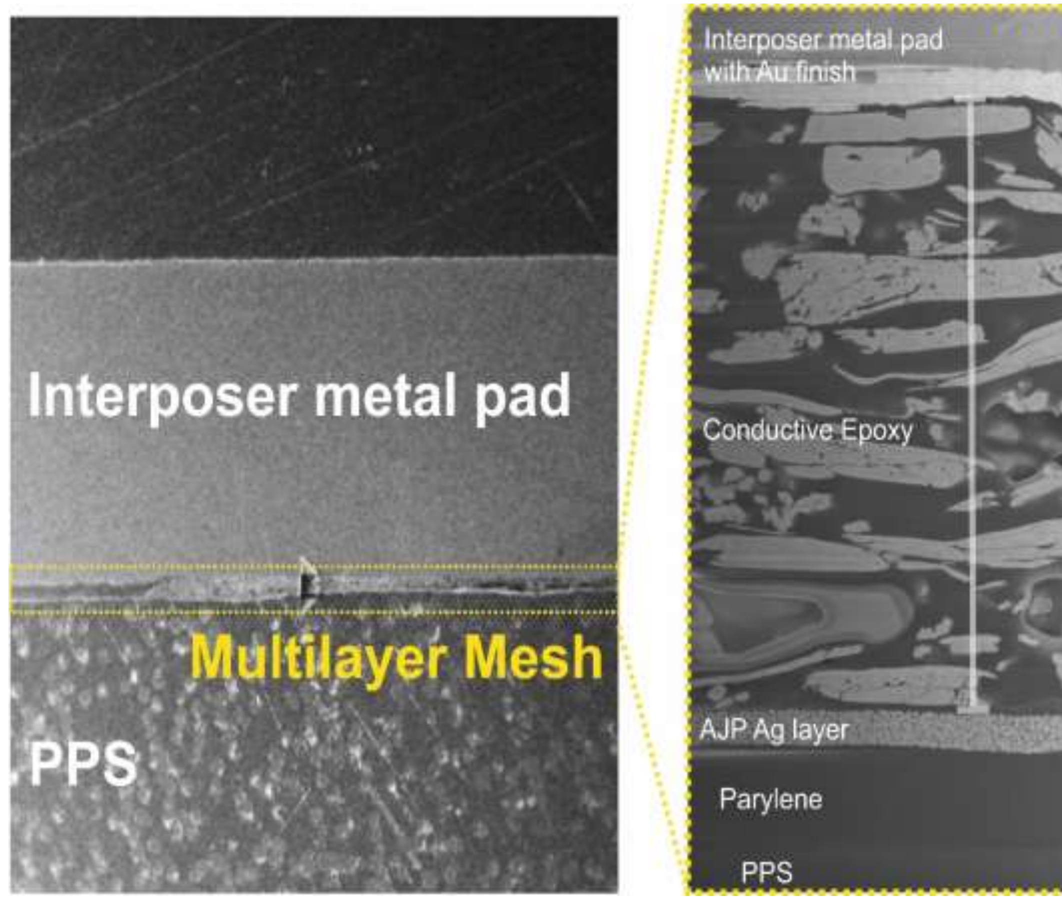
Results

Fabricated Demonstrators

- **Materials**
  - Conductive Mesh: *Ag Nanoparticle Ink*
  - Dielectric: *Parylene C*
  - Substrate: *PPS (GF enhanced)*
- **Fabrication**
  - Combination of AJP, CVD, Laserablation
  - All processes less than 125°C
- **Electrical properties**
  - Via < 5Ω
  - Printed Tracks < 1kΩ/m
- **Security**
  - Line/Space: 150/250µm
  - Evaluation ongoing
- **Reliability**
  - Tested







FIB cross-sections showing the relation of multilayer mesh and metal tap for interconnection towards PCB

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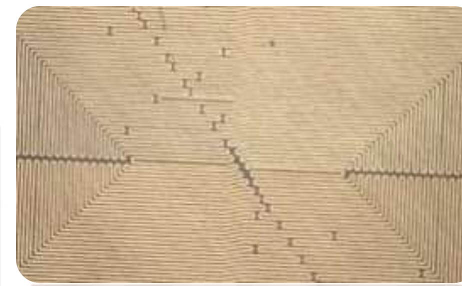
Reliability investigations

Conclusion

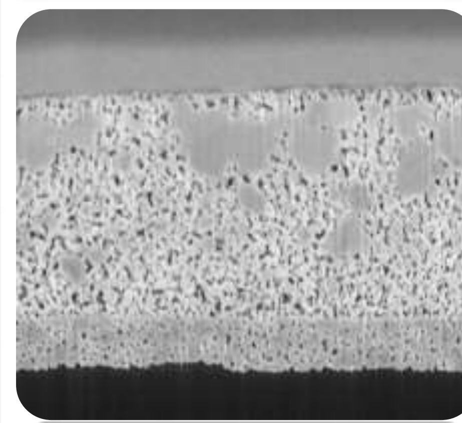
Tested

- Multilayer Build-Up 2xAg layers, 2xparylene layers, laser vias
- Interconnection approach (Pogo pin, metal tap)

→ Combination of printed Ag nanomaterial and Parylene dielectric layer is a reliable material concept



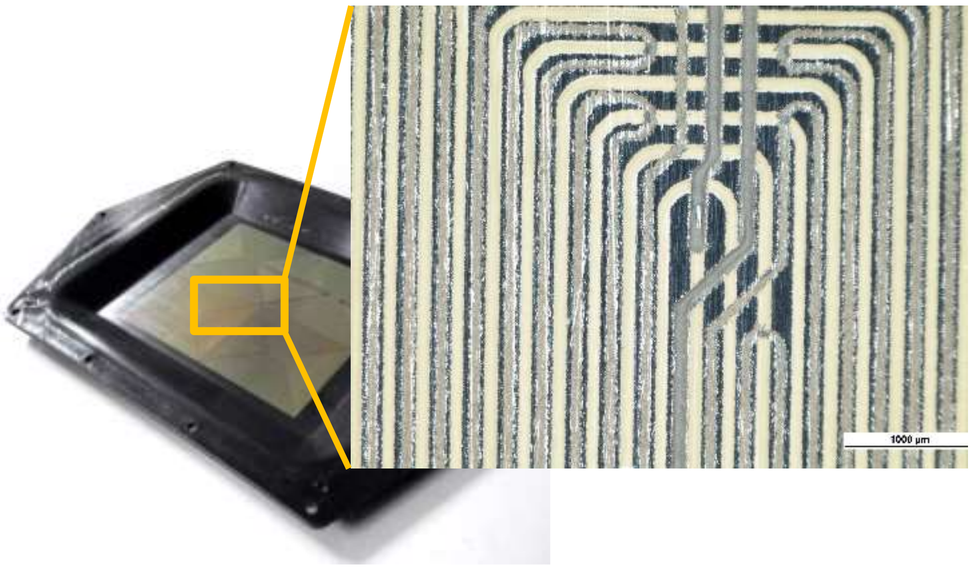
Test	Result	Comments
Thermal Cycling -55°C/125°C, 30min	> 500 cycles passed	No failures detected
Thermal Storage @125°C	1000h passed, within + 5% resistance change	No delamination, no cracks
Torsion Test 7° & 10° at 30°	> 20.000 cycles passed @ 7°	Test performed with CAP on PCB → PCB components will fail 1st
Vibration Test	Passed Step-Stress Test @ resonance frequency	Test mainly dedicated to test the pogo pin interconnection →PCB components will fail 1st
Pull Test & Shear Test	Adhesion for Ag nanoparticle ink on different substrate materials available	Pretreatment procedure developed before the printing step (Ar/O_2plasma treatment)



Reliability investigations
XRAY for security

- XRAY Invisibility for full area cap scan
  - Resolution limited (> 50µm) when analyzing the 164 x 110 CAP substrate

Nanotom® [GEsensing]



Reliability investigations

XRAY for security

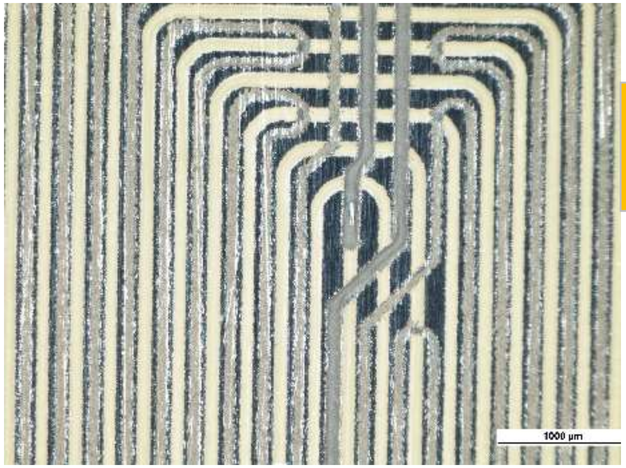
Nanotom® [GEsensing]

- XRAY Invisibility for full area cap scan
  - Resolution limited (> 50µm) when analyzing the 164 mm x 110 mm CAP substrate

- Idea of Mesh Build achievable for small area scan
  - High resolution scan (without damaging/cutting the substrate ~7µm) on 14 mm x 10 mm

Not easy to enter!

Enormous effort is needed to understand the secure mesh build-up even when using HighEnd XRAY Tomography



Conclusion

- Secure tamper respondent envelope presented
  - Realized by digital additive manufacturing
  - Lot size 1 could be realized / design could be changed with each product
- Scalable and customizable process chain developed and tested
  - Process temperatures < 125°C
  - Suitable for low cost polymers
  - Process flow is transferable to other substrates and geometries
- Reliability investigations show that the combination of Ag nanoparticle Ink and Parylene C enables multilayer mesh approach

→ Outlook: full security evaluation for the system (CAP, SiP, PCB)

Thank you for your attention!

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Motivation

Nanoparticle Inks/Pastes – Post-treatment and sintering

- Suspensions of metal particles in solvents and binders
- Pretreatment for dense layer and electrical conductivity:
  - Drying out solvents, burning out organic shells, sintering

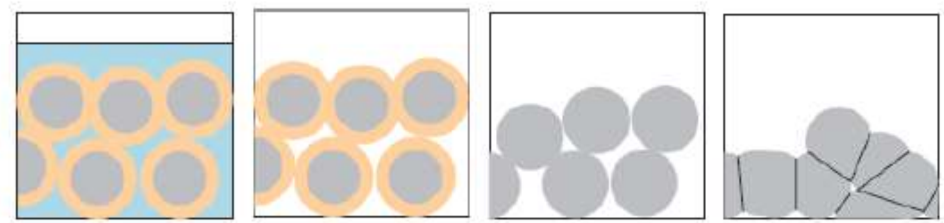


Fig 5: ***Nanoparticle filled Ink, Drying out solvents, burning out organic shells, sintering***

Sintering without pressure

- Particle necking due to diffusion effects

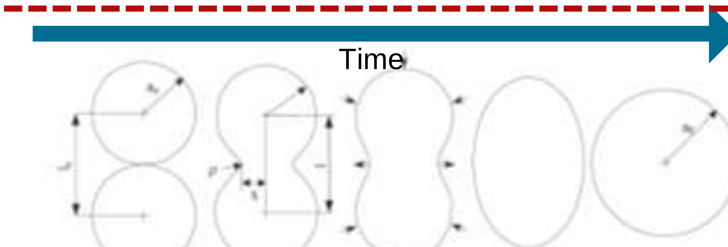
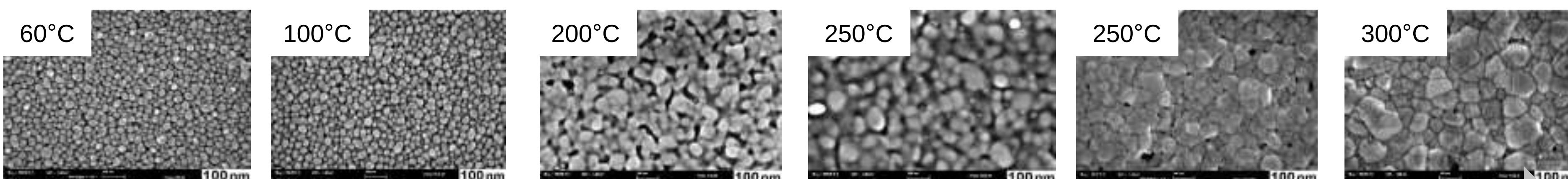


Fig 6: ***2 Particle Model [J. I. Frenkel (1945)]***

Experimental Setup

- Sintering of Ag Nanoparticles and SEM investigation at different temperature steps



SEM Investigation - Sintering of Ag Nanoparticles and grain size at 60°C, 100°C, 200°C, 250°C, 300°C

Technologies

Concept & Process flow (schematic)