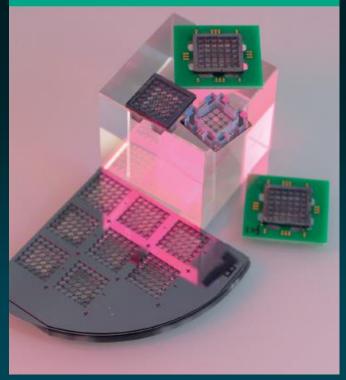


FRAUNHOFER INSTITUTE FOR ELECTRONIC NANO SYSTEMS ENAS

JUNE 14 AND 15, 2016 | FRAUNHOFER ENAS TECHNOLOGIE-CAMPUS 3 | 09126 CHEMNITZ

CHEMNITZER SEMINAR SYSTEM INTEGRATION TECHNOLOGIES





Beyond State-of-the-Art:

Integration of MEMS in Fan-Out Wafer-Level Packaging Technology based System-in-Package (WLSiP)

Steffen Kröhnert, Director of Technology André Cardoso, Senior R&D Integration Engineer

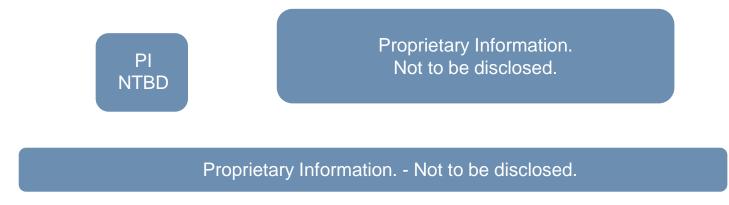
June 2016 - V1.0 - EXT





• NANIUM is highly committed to IP protection.

- Therefore, this hand-out of the presentation has been modified from the original presented.
- Some sections have been covered with blue boxes and "Proprietary Information. Not to be disclosed." remark, as it is shown in the examples below.
- In case of questions, please contact the author and/ or speaker directly.
- We apologize for any inconvenience caused by that and thank you for your understanding.



The Future: A MEMS/ Sensors Enabled World

Vision and Projections

- In 2020, 300 billion sensors are making lifestyle enhancements in our daily lives.*
- The intelligent sensor market is a \$10.5 billion industry in 2020.**
- The market for printed and flexible sensors reaches \$7.3 billion in 2020.***



<u>loT / loE</u>

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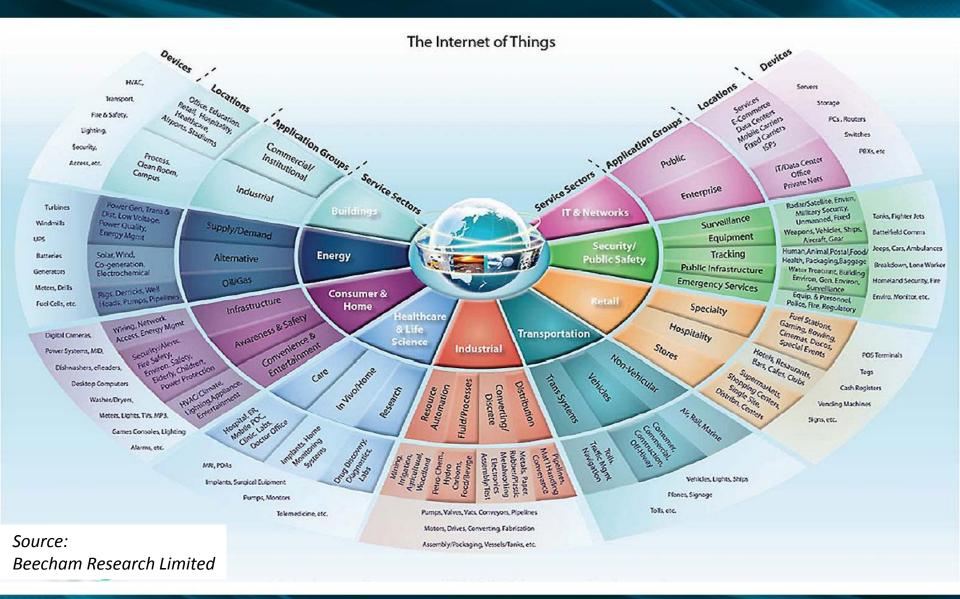
Internet of Things Internet of Everything

- *) "Emergence of Trillion Sensor Opportunity," SemiconWest, <u>http://www.semiconwest.org/sites/semiconwest.org/files/docs/SW2013_Janusz_Bryzek_Fairchild Semiconductor.pdf</u>.
- **) "Smart/Intelligent Sensor Market worth \$10.46 Billion by 2020," Military and Aerospace Electronics, <u>http://www.militaryaerospace.com/news/2014/03/12/smart-intelligent-sensor-market-worth-10-46-billion-by-2020.html</u>.
- ***) "IDTechEx: Printed sensors market will increase by more than \$1 billion by 2020," Drupa, http://www.drupa.com/cipp/md_drupa/custom/pub/content,oid,30443/lang,2/ticket,g_u_e_s_t/local_lang,2.

The Internet of Things/ Everything

Wearable Electronics is only one Part of this Big Wave





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The Internet of Things/ Everything

Wearable Electronics is only one Part of this Big Wave



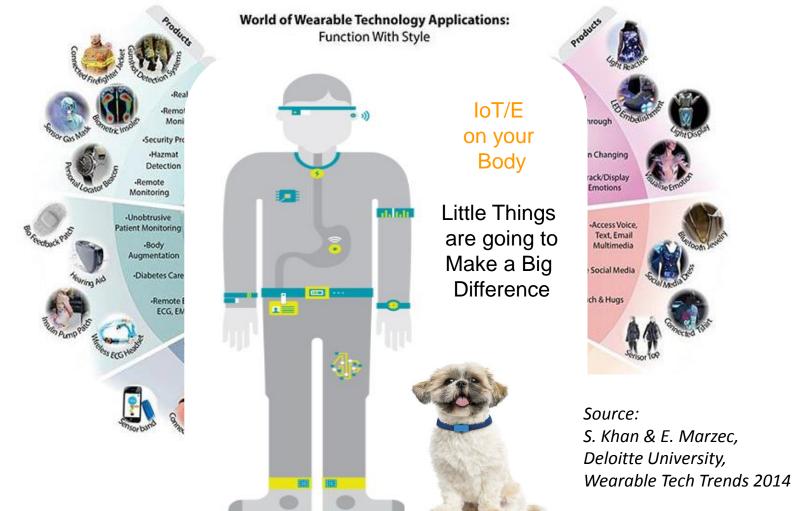


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The Internet of Things/ Everything

Wearable Electronics is only one Part of this Big Wave

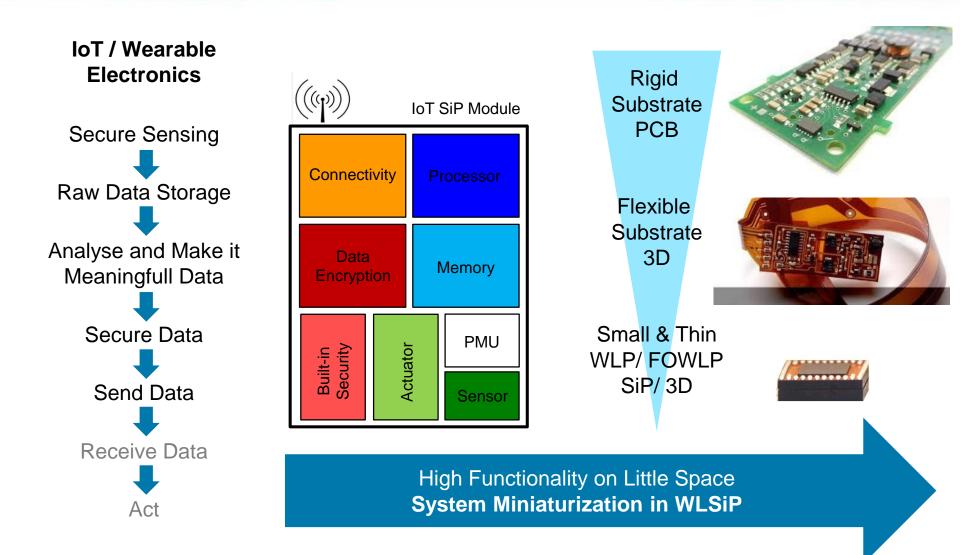




Source: Beecham Research Limited

Functionality Integration in Package → WLSiP

The Critical Triad of Packaging: Performance - Form Factor - Cost



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The Future: A MEMS/ Sensors Enabled World

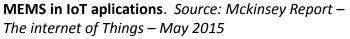
MEMS/ Sensor Market

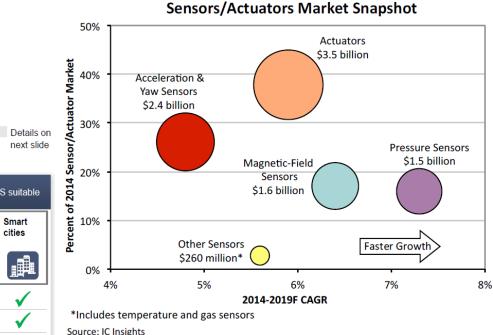


MEMS/ Sensors market is growing fast...

F MEMS are replacing most conventional sensors needed in IoT devices at a lower cost and better performance

Key trends in MEMS MEMS can be used across all loT verticals						✓ MEMS suitable	
 Cost and size of MEMS are decreasing while performance is 		Wear- ables	Smart home	Medical electro- nics	Indus- trial auto- mation	Connec- ted cars	Smart cities
increasing	Microphone	\checkmark	\checkmark	\checkmark	\checkmark	\checkmark	\checkmark
 Integration of MEMS into 1 building block is on-going (e.g., IMU¹ combos) 	BAW filter ²	\checkmark	\checkmark	\checkmark	\checkmark	\checkmark	\checkmark
	Pressure sensors	\checkmark	\checkmark	\checkmark	\checkmark	\checkmark	\checkmark
	Accelerometer	\checkmark		\checkmark	\checkmark	\checkmark	
 Integration of MEMS with logic expected in next 5 years 	Magnetometer	\checkmark			\checkmark	\checkmark	
	Gyroscope	\checkmark			\checkmark	\checkmark	
	Lab-on-chip			\checkmark	\checkmark		
	Flow sensor			\checkmark	\checkmark		
	Temperature	\checkmark	\checkmark	\checkmark	\checkmark	\checkmark	\checkmark





... in ever increasing application fields

Wearables, IoT, Biomedical...

The Future: A MEMS/ Sensors Enabled World



Which Packaging Technology for IoT/ IoE Modules?

Target:

• 300 billion MEMS/ Sensors by 2020 for IoT/ IoE Enabling

Packaging Requirements:

- Small Form-factor/ Miniaturization of IoT/ IoE Modules
- High Volume Manufacturability, High Performance at Low Cost

\rightarrow Solution:

- System Integration and effective Sensor Fusion in the Modules
- The right Packaging Technology: WLP/ FOWLP = "Active Interposer"

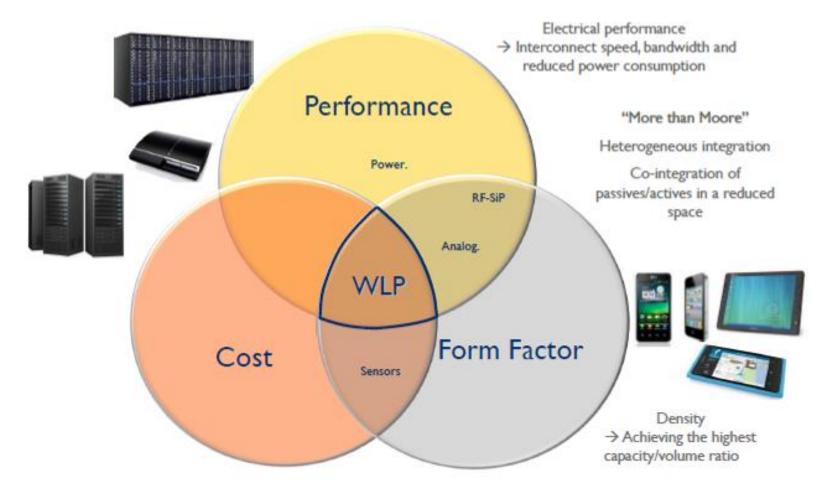
\rightarrow Challenges:

- Electrical and Thermal Performance of Miniaturized Systems
- MEMS/ Sensor Design and Robustness → Co-Design with Packaging
- MEMS/ Sensor Integration in High Volume/ Low Cost Packaging Process
 - Mold Embedding/ Encapsulation
 - Batch Processing in Large Panel Format

Which Packaging Technology for IoT/ IoE Modules?



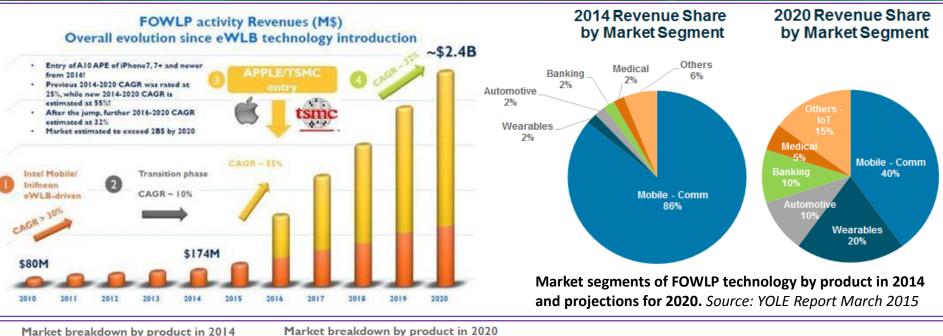
FOWLP offers best trade between performance, cost, and form factor



Source: "Fan-out and Embedded Die: Technology and Market", Yole Développement Report, 2015.

The Future: A MEMS/ Sensors Enabled World

Which Packaging Technology for IoT/ IoE Modules?



Market breakdown by product in 2014 Stacked Memories Bluetooth/GPS Processors Module 5% Audio Codec (APE/GPU/...) Analog Specific 2% 5% **ICs** 7% MEMS _8% Wireless Bluetooth/GP Baseband SOC; Module... Total 2014 Total 2020 Wireless Baseband SOC \$174M Higher integration

NANIUM's anual revenue projection by market segment 2014/ 2020 – Higher integration capability of FOWLP will give access to markets where nowadays FCBGA-based PoP/SiP are dominating

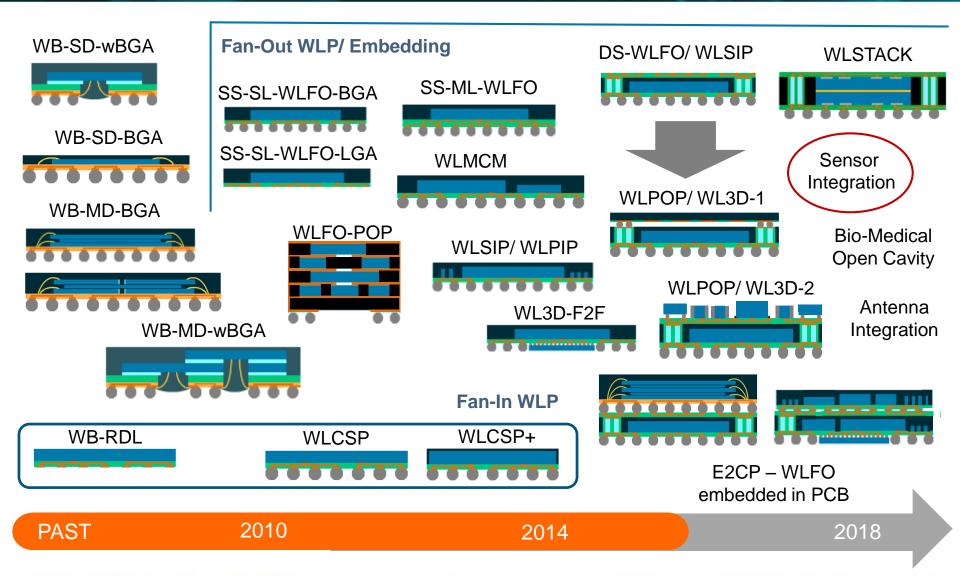
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MEMS will represent \$54M market for NANIUM

NANIUM Package Roadmap

From WB-SD-wBGA to System Integration on Wafer-Level

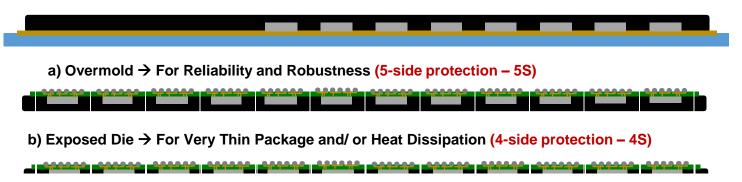




Introduction to NANIUM's WLFO Technology

Basic Process Flow for Single Die, Single-Sided Package





Compression Molding Die Placement Thermal Release Tape

Metal Mold Carrier

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Marking, Singulation Solder Ball Drop Thin Film Processing

Introduction to NANIUM's WLFO Technology

Basic Process Flow for Single Die, Single-Sided Package



Interesting Facts about NANIUM's WLFO:

- Based on Infineon's/ Intel's eWLB (embedded Wafer-Level Ball Grid Array);
- First 300mm round panel based eWLB realization for HVM in 2010;
- Production line running HVM since Q3/2010;
- Shipped more than 600 million WLFO packages in the last 5 years;
- Proven mature WLP technology with 99.5% plus (99.8% in HVM) yield levels.

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- Reconstituted mold panel size independent of incoming wafer diameter;
- Independent of material (Si, GaAs, SiGe, Glass, Passives, Packaged Parts);
- Adaptable fan-out area, and solution for I/O gap between die and board;
- Substrate-less package, the interposer is built-up in Thin-Film Process;
- Smaller footprint, and thinner (!) compared to WB and FC packages;
- Superior electrical and thermal performance due to short connections;
- Lower unit cost due to large format batch processing;
- Simplified Bill of Material (BOM), low inventory, and short Supply Chain;
- Enabler for heterogeneous dense system integration on Wafer-Level driving system miniaturization.

→ WLSiP and WL3D

→ Sensor Integration ?!

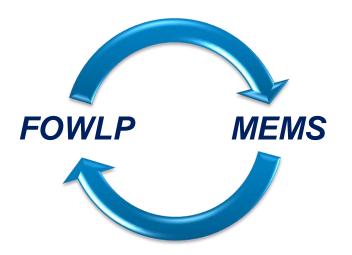
MEMS in FOWLP – Closing the Gap

Two fast growing markets



How does each world contributes to the other?

Technology Partner, Application Enabler



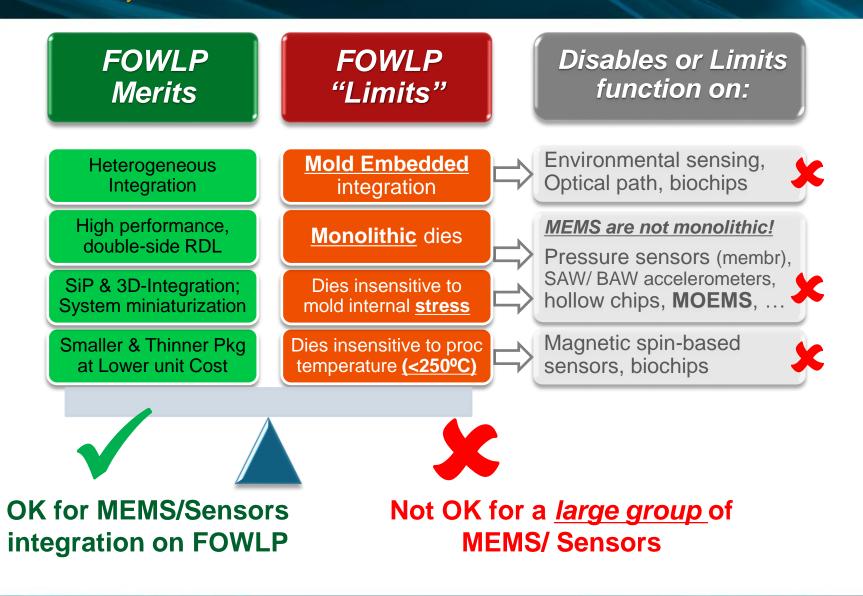
Is FOWLP ready for MEMS/ Sensors?

Market Opportunity, Catching "MEMS-Train"

MEMS in FOWLP – Closing the Gap

FOWLP ready for MEMS?

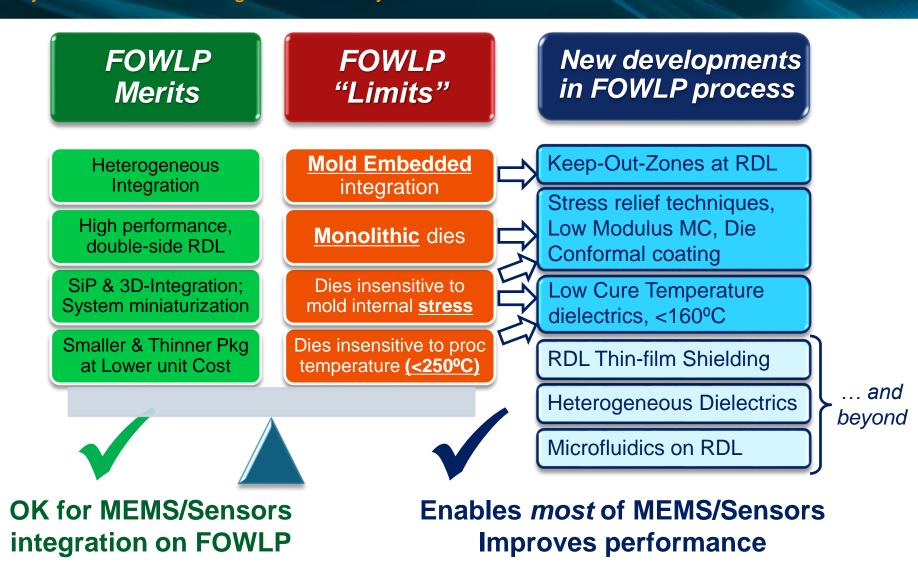




MEMS in FOWLP – Closing the Gap

Beyond the SoA - Making FOWLP ready for MEMS





MEMS in FOWLP – Developments 1/4

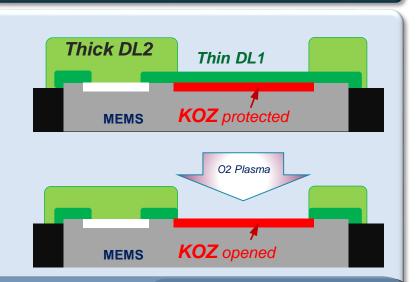
Enabler: Keep-Out-Zones



* <u>Keep-Out-Zones</u> – Protection of Sensitive Areas during FOWLP process

How:

- DL1 protects KOZ against RDL process (Sputtering, Wet Etch, ...)
- □ A thick DL2 exposes DL1 at KOZ
- KOZ opened with O₂ Plasma Ashing, for very low damage
- DL1/DL2 Ashing discrimination:
 - Thickness ratio > 4:1
 - Different Dielectrics
- ✓ Using existing RDL structure
- ✓ Process line compatibility
- ✓ All at wafer-level 12" process



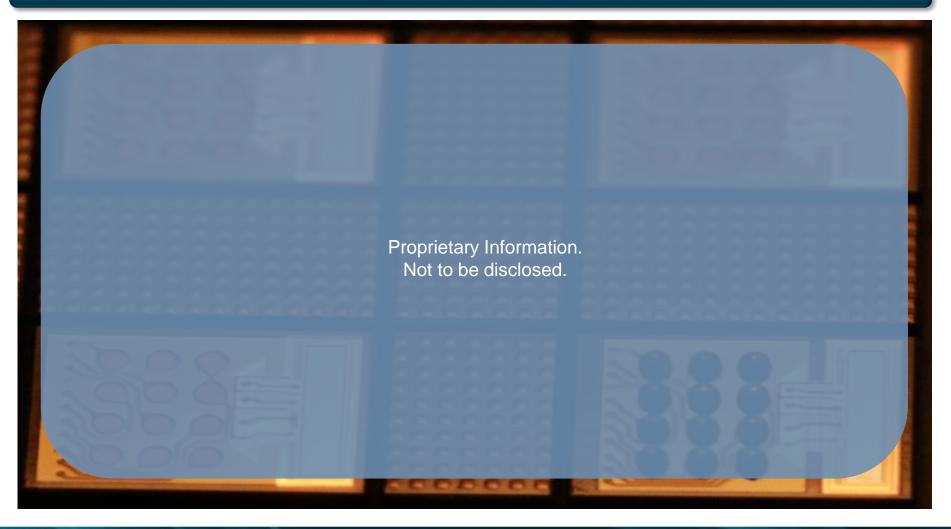
Proprietary Information. Not to be disclosed.

. e.g. optical path

MEMS in FOWLP – Developments 1/4

Enabler: Keep-Out-Zones

Keep-Out-Zones – Protection of Sensitive Areas during FOWLP process



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MEMS in FOWLP – Developments 2/4

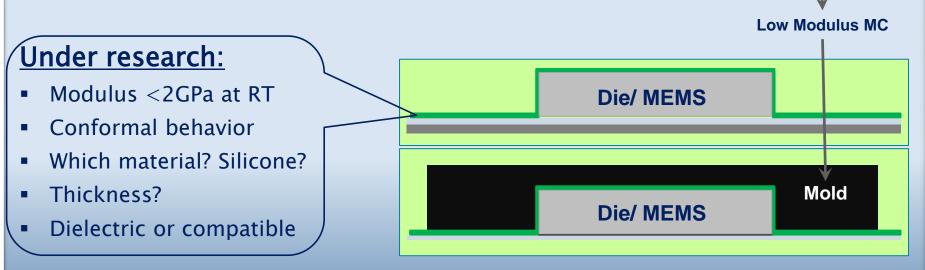
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Enabler: Mold Stress Relief

Stress Relief on Dies for mold pressure sensitive devices

How:

- □ Low Modulus Mold Compound \rightarrow Flexible Packages?
- Conformal coating of dies prior to molding
 - Deposition via vacuum lamination or spray coating
- Also: Positive effect from Low Cure temperature dielectrics



MEMS in FOWLP – Developments 3/4

Enabler: Shielding

Thin-Film Shielding – Seed Layer as a Functional Player!

How:

 Partial remove of Seed Layer (Ti or TiW) after Electroplating process, with a mask for wet-etch shaping

Advantages:

- Electrical performance improvement
 - ✓ EM protection; Noise decoupling
 - ✓ Moisture uptake effect mitigation
- ✓ Capacitive effect is possible
- ✓ Semi-additive process, no waste
- ✓ All in 12" FOWLP standard process
- ✓ Very low cost!!

Thin-film Shielding

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Proprietary Information. Not to be disclosed.

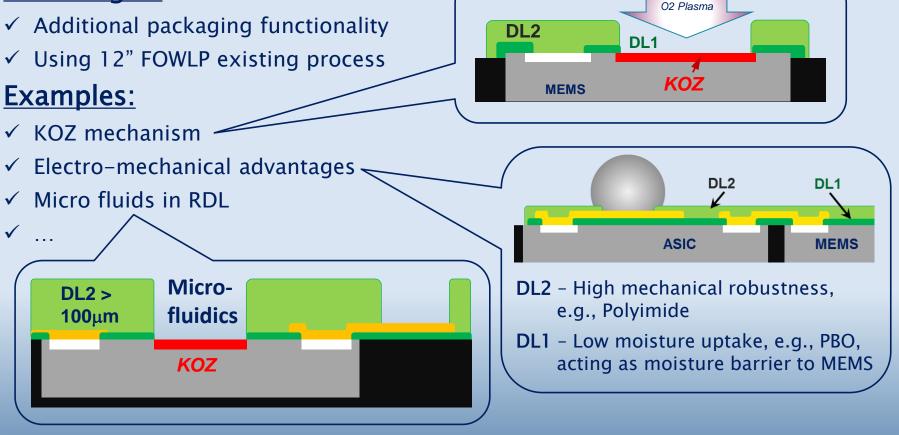
MEMS in FOWLP – Developments 4/4

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Enabler: Heterogeneous Dielectric Stacking

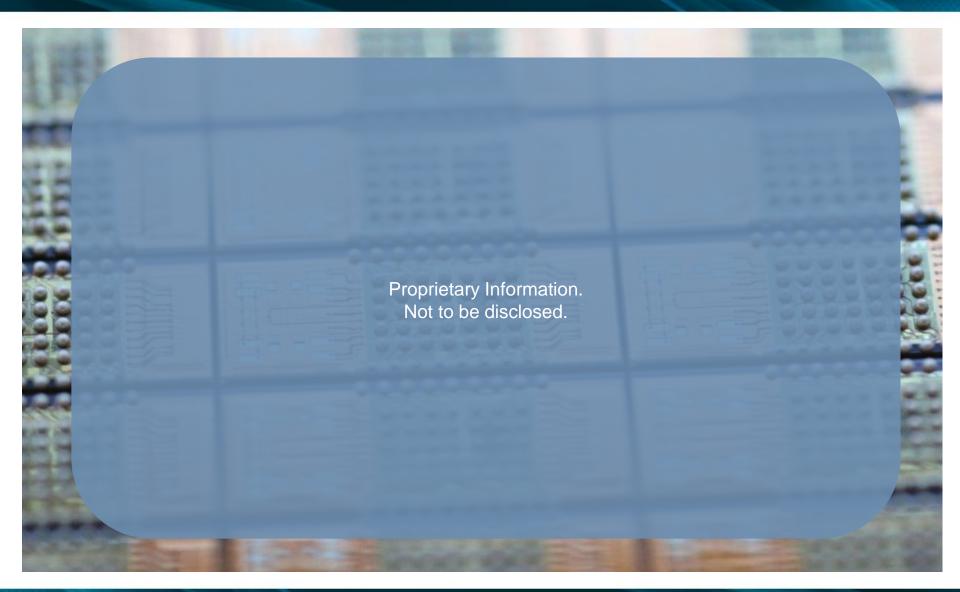
Heterogeneous Dieletrics – Symbiotics effect

Advantages:

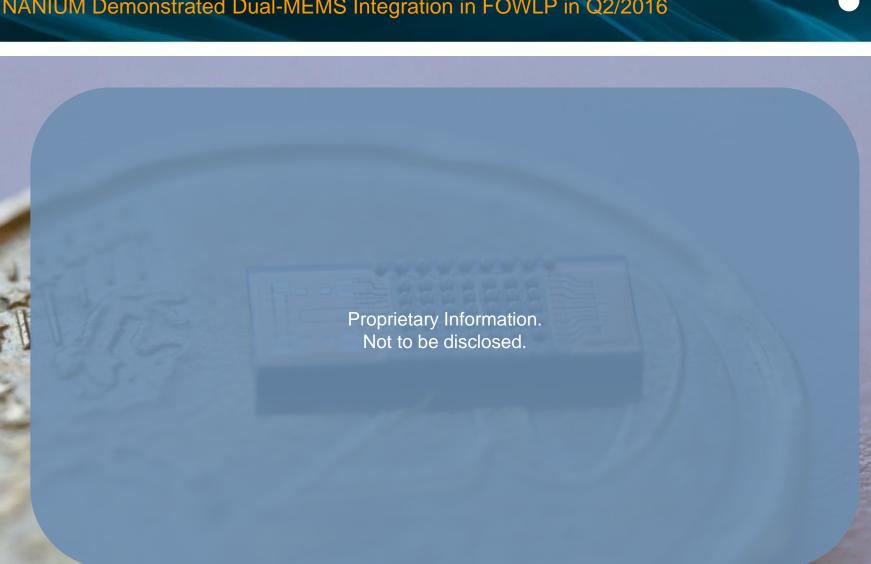


What's Next? NANIUM Demonstrated Dual-MEMS Integration in FOWLP in Q2/2016





What's Next? NANIUM Demonstrated Dual-MEMS Integration in FOWLP in Q2/2016



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Summary and Conclusions



- Billions of IoT/ IoE Modules require single or multiple MEMS/ Sensors integration
- Success of IoT/ IoE Modules will also depend on the selection of the right PACKAGING Technology offering the following key capabilities:
 - Miniaturization by dense System Integration
 - Effective MEMS/ Sensor Fusion into the systems
 - Manufacturability of High Volume and Low Cost
- Wafer-Level Packaging (WLP), namely **Fan-Out WLP Technologies** such as eWLB/ WLFO, RCP, M-Series, InFO, NTI, SLIM and SWIFT, are **showing great potential**
- FOWLP is growing with forecasted CAGR between 50-80% until 2020
 - System Integration solutions (WLSiP and WL3D) will dominate volumes in future compared to current single die FOWLP packages for mobile communication
- Recent developments for eWLB/ WLFO Technology to overcome current limits for MEMS/ Sensor Integration related to FOWLP technology merits have been shown
 - Processing Keep-Out Zones for MEMS/ Sensor access to environment in molded packages
 - Mold Stress Relief on dies, MEMS/ Sensor die decoupling from internal package stress
 - Thin-Film Shielding using PVD seed layer for ECD as functional layer (is there anyway)
 - Heterogeneous Dielectrics Stacking (different materials fulfilling different functions)



Thank you for your attention

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