#### microDICE<sup>™</sup> System for Separation of SiC Wafer Using Thermal Laser Separation

- System Integration Technologies – Fraunhofer ENAS -(Ronny Neubert, 3D-Micromac AG)



#### 3D-Micromac – At a Glance

- Manufacturer and service provider for
  - Laser micromachining systems and
  - Production equipment for printing and coating technologies
- Design of complete machining systems including process development and service in-house
- Founded in 2002
- Founded US subsidiary in 2014



1. Thermal Laser Separation (TLS-Dicing<sup>™</sup>)

- 2. Application examples
- 3. microDICE<sup>™</sup> system
- 4. Conclusion



## **Thermal Laser Separation (TLS)**

Starting point (and optional straightness) defined by scribe



TLS is a cleaving process, initiated by

heat and cooling

## **TLS-Dicing**<sup>™</sup> Technology



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#### Main Properties of TLS-Dicing<sup>™</sup>

- Residue-free
- Zero kerf
- No chipping
- Nearly perfect sidewalls
- Works for back-side metal
- Works for:
  - SiC
  - Si (Semi & PV)
  - GaAs / Ge



JFET on 4H-SiC-Wafer, thickness 160  $\mu m$  with PCM (left upper rim) and back side metal, Dicing speed 200 mm/s



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## **TLS-Dicing<sup>™</sup> for SiC – Exemplary Results**

- Special USPs for SiC:
  - Dicing speed 200 mm/s
  - One cleaving pass per street
  - PCM in street acceptable (no design rules)
  - No tool wear
  - Perfect side wall
- Further USPs:
  - Back-side metal is separated w./o. pealing
  - Tape not damaged



SiC-JFET, Wafer thickness 160  $\mu m$ , Die size 3.16 X 3.16 mm², Back-side metal, mounted on DCB



#### TLS-Dicing<sup>™</sup> – Electrical Parameters for SiC



SiC-JFET, Wafer thickness 160  $\mu$ m, Die size 3.16 X 3.16 mm<sup>2</sup>, Back-side metal, mounted on DCB

20 \*2 SIC JFET 1 SIC JFET 2 SIC JFET 3 SIC JFET 4 15 SIC JFET 5 Current (mA) 10 5 -500 -1000 -1500 -2000 0 Voltage (V)

I-V blocking characteristics

 $\rightarrow$  No impact on electrical perfomance by TLS



## TLS-Dicing<sup>™</sup> – Electrical Parameters for Si

Project "A" – cutting solar cell



Project "B" – Dicing of power-diodes



Leakage current of diodes is significantly reduced

Electroluminescence measurement

 $\rightarrow$  Damage free cutting through pn-junction is possible



Resizing-ring (ø 300 to 200 mm, Si 775 µm)

#### Comparison to ablative laser dicing



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## TLS-Dicing<sup>™</sup> – Separation of Back Side Metal

- Works with back side metal (up to 10 μm)
- Recommended: ratio metal to bulk: < 1 : 100
- No peeling!



Si-Wafer with back side metal

## **TLS-Dicing<sup>™</sup> – Optical Properties**

- One NIR cleaving-laser for all substrates
  - For Si / Ge / GaAs / doped SiC a NIR-laser is optimal
  - Different dopants are acceptable
- Scribing process option for PCM available



## TLS-Dicing<sup>™</sup> for Other Materials







Ge

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## **TLS-Dicing<sup>™</sup> - Motivation**

 SiC Dicing is a hard job (hardness 9.2 on Mohs scale)



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# Our Solution – microDICE<sup>™</sup> System for TLS-Dicing<sup>™</sup>



Lower cost, excellent cleaving results, and higher throughput

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#### microDICE<sup>™</sup> System

- Up to 300 mm (12") wafer size
- Integrated laser sources with long lifetime
- Integrated patented micro stretching function
- Automated wafer handling
- SECS / GEM interface
- Compatible with common SEMI standards
- Consumables: only DI-water



microDICE<sup>™</sup>



## microDICE<sup>™</sup> - Major Components

- Processing unit (left side)
  - Scribing function (by pulsed fiber laser)
  - Cleaving function (cw laser and cooling)
  - Alignment system
  - Vacuum chuck
- Handling unit (right side)
  - 2 x 200 mm or 1 x 300 mm cassette
  - Fault detection



Major components



## TLS-Dicing<sup>™</sup> on microDICE<sup>™</sup> - a Case Study for SiC

Current trends for SiC-products:

- The market volume of SiC is growing with CAGR of 25%
- One saw blade can't saw one 6 inch wafer



Transition from 4" to 6" has been started









#### **Assumptions for Cost Calculation**

- Considered:
  - Throughput: 4 wafer per hour
  - Consumables (saw blades)
  - Invest/depreciation for tool
  - Footprint
- Not considered:
  - Benefit in terms of yield
  - Reduced operator costs



mechanical saw: 37 € TLS-Dicing<sup>™</sup>: 2.40 €



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#### Conclusion

- Minimal cost of ownership
- Clean process
- Better electrical properties
- High throughput
- Less breakage
- Increased yield
- Damage-free backside metal

TLS-Dicing provides excellent cleaving results in combination with high yield and throughput.





# TLS-Dicing<sup>™</sup> - Cooperation with Fraunhofer IISB

- More then 8 years of successful cooperation
- Experienced scientists
- Wide range of measurement tools
- Equipped with the latest version of TLS-Dicing<sup>™</sup> tool in clean room





#### TLS-Project partly funded by European – contract 611332 "SEA4KET"

#### Image sources

- \*1 Courtesy Fraunhofer Gesellschaft
- \*2 Dohnke et. al: Comparison of different novel chip separation methods for 4H-SiC, Proceedings of ECSREAM conference, Grenoble 2014
- \*3 Koitzsch et. al.: Improving Electric Behavior and Simplifying Production of Si-Based Diodes by Using Thermal Laser Separation, Proceedings of ASMC2013, Saratoga Sprigs, (NY) 2013.
- \*5 Karl Dohnke
- \*4, 6 -10 Courtesy Fraunhofer Gesellschaft

3D-Micromac AG Technologie-Campus 8 09126 Chemnitz, Germany

#### http://3d-micromac.com

Phone: +49 371 400 43 0 E-Mail: info@3d-micromac.com

