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Thales vision & needs in advanced packaging for high end applications

M. Brizoux, A. Lecavelier
Thales Global Services / Group Industry

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- Packaging trends driven by mobility / IoT

Advanced packaging needs & vision for high end applications

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Thales products & mission profiles

Main product characteristics

- ➢ Low volume (10-10k pcs/year)
  - Heterogeneous
  - Complex
  - Dense

  } boards
  - Advanced technology as key differentiator
- ➢ Reparability
- ➢ Reliability
  - Long mission profile
  - Harsh environment

Constraints

- ➢ Dependency of civil market: dual technologies
  - Need to launch manufacturing spread over long period → Management of obsolescence
  - Sourcing (PCB, EMS …): New technologies, specific processes & Export control

N°1 worldwide

Payloads for telecom satellites

Air Traffic Management

Sonars

Security for interbank transactions

N°2 worldwide

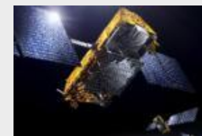
Rail signalling systems

In-flight entertainment and connectivity

Military tactical radiocommunications

N°3 worldwide

Commercial avionics


Civil satellites

Military surface radars

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Thales products & mission profiles

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Reliability in harsh environment & long mission profiles

- Up to 35 years operation
- Harsh thermo-mechanical environment
- Harsh mechanical environment
  - Mechanical shocks & vibrations

Constraints far from consumer electronic

Use Category	Typical years of Service	Accepted Cumulated Failure within Lifetime	Tmin [°C]	Tmax [°C]	Delta T [°C]	Mechanical Shock and High Vibration Level	Repair Needs	Typical Volume per Product Batch
Space (leo / geo)	5 to 30	0.001%	-55	95	3 / 100	Yes	Yes (rework)	3
Military Avionics (a / b / c)	10	0.01%	-55	95	40 / 60 / 80	Yes	Yes	10
Commercial Avionics	20	0.001%	-55	95	20	Yes	Yes	200
Military Ground & Ship	10	0.1%	-55	95	40 (+60)	Yes	Yes	50
Telecom	7 to 20	0.01%	-40	85	35	Yes	Yes (rework)	1000
Automotive under Hood	5	0.1%	-55	125	60 (+100;+140)	Yes	No	100 000
Industrial & Automotive Passenger Compartment	10	0.1%	-55	95	20 (+40;+60;+80)	Yes	No	100 000
Computers	5	0.1%	15	60	20	No	No	100 000
Consumer	1 to 3	1.0%	0	60	35	No	No	1 000 000

Classification based on IPC-SM-785

High-Reliability Requirements | Harsh Thermo-mechanical Environment | Harsh Mechanical Environment | Repair-ability | Low Volume

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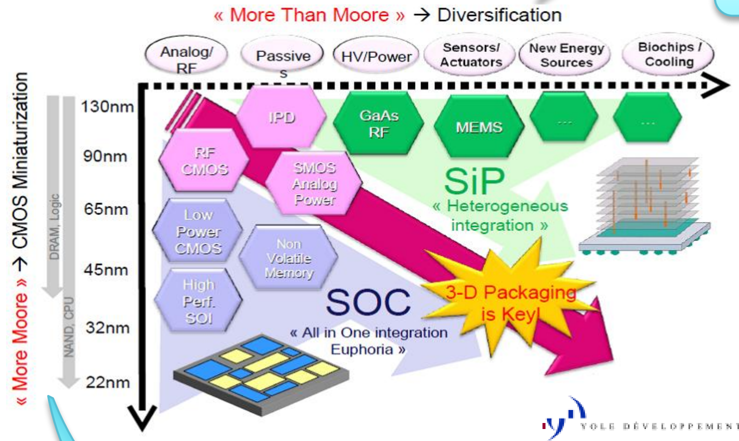
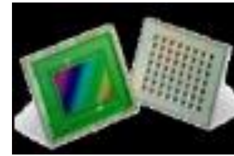
Packaging trend driven by Mobility / IoT

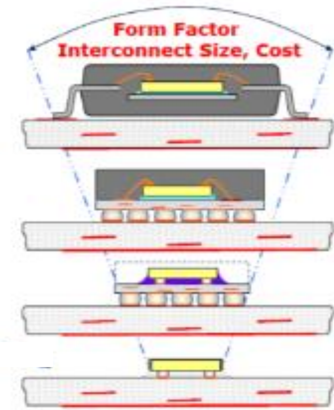
Heterogeneity & density



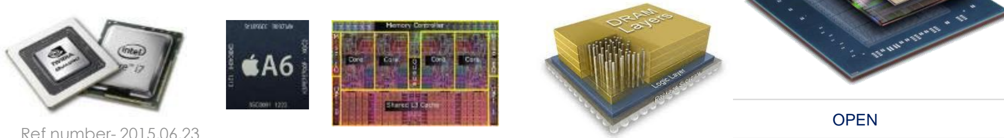
Sense, interact, power…:
complex heterogeneous integration



PACKAGE key to adapt



Compute & storage: complex design
Agressive dimension reduction



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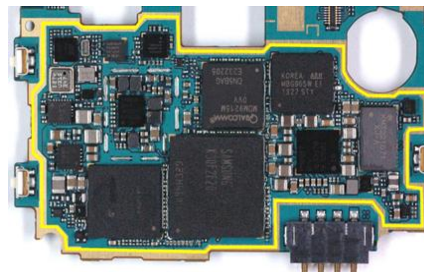
SiP modules: key for complex/dense electronics

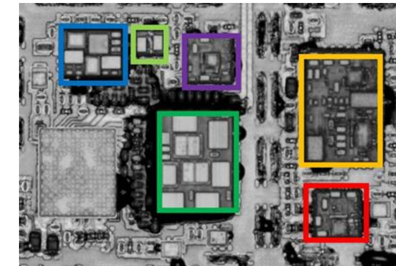
SiP modules : paramount solution to make testability easier & improve yield

- **Advantages**
  - Significantly increased board density
  - Heterogeneous functionalities in a package
  - Improved technical performances
  - Reduced mother board complexity
  - Re-usable module & reduction of development time

- **Constraints**
  - NRE in low volume
  - Thermal management
  - Complex supply chain management
  - Obsolescence management
  - Multi-sourcing

	Nb of Pts	Aera mm²	Nb of Pts/ dm²
Top board	1984	2156	9200
With SIP	1984+230		10500
Bottom board	2921		13900
With SIP	2921 + 9438		57300





Total density	23100 Pts /dm²
Total density with SIP	67800 Pts/dm²

SIP increase the total density by ~3

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PCB and assembly trend

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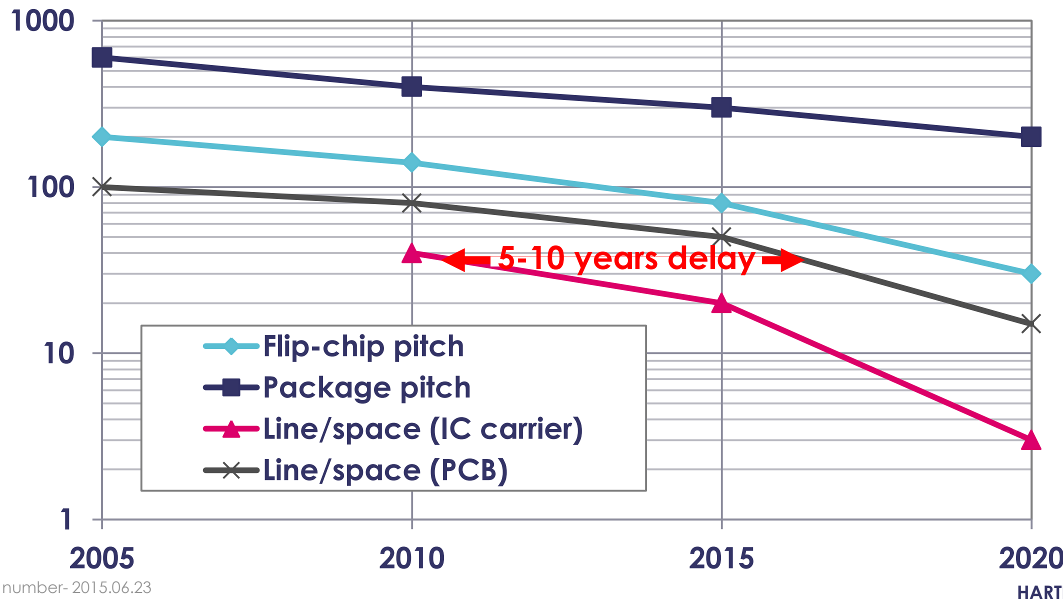
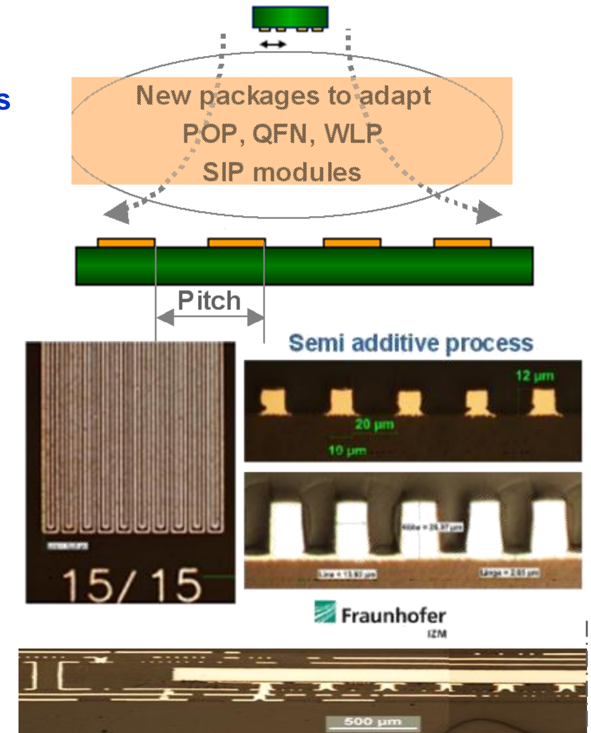
PCB design trends driven by IC carrier

- PCB has to accommodate the latest packaging trends
  - Finer pitch, increased I/O count: BGA, QFN, WLP packages, SiP modules
  - Increased density by embedding components into PCB or Si carriers
  - Increased challenge for solder mask





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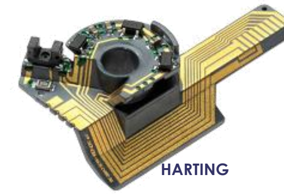
Conductor deposition on polymer

Different processes like

- Molded Interconnect Devices
  - Address the coupling electrical/mechanical
    - Mature with one layer

CITEC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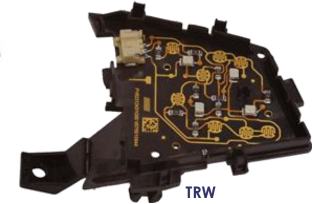
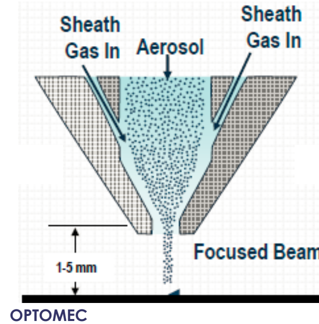
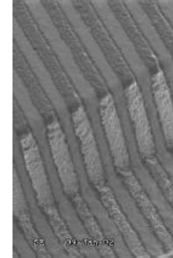
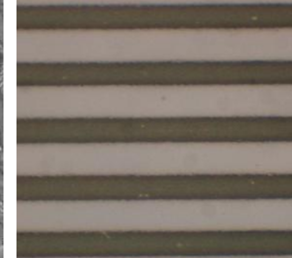

TRW

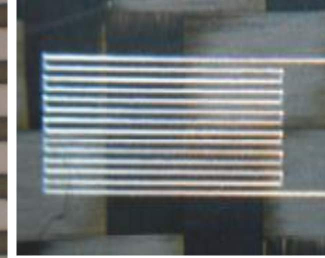
- Aerosol jet printing
  - Fine line (typically 100µm)
    - Multilayer under development



OPTOMEC

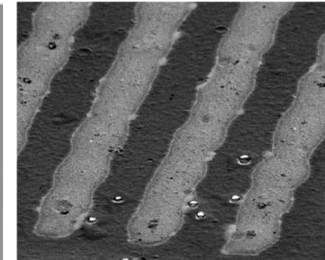

OPTOMEC




OPTOMEC

- Ink jet printing (2D)
  - Fine line (typically 100µm)
    - Line definition function of drop size & surface energy

NY Industries


NY Industries

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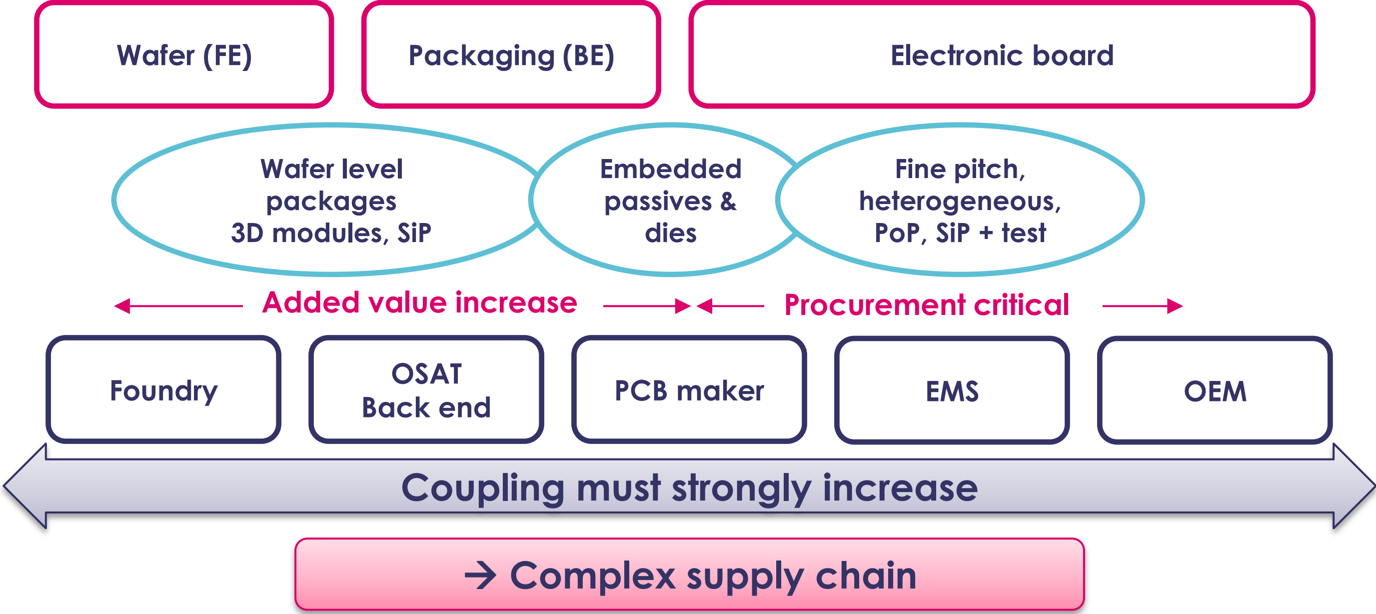
Supply & value chain evolutions

Added value in packaging development

- Strong competition between IC foundries & PCB makers

Heterogeneous integration at board level

- Increase the complexity of supply chain



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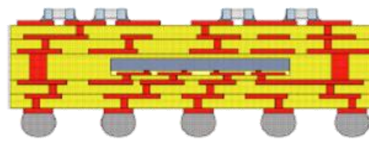
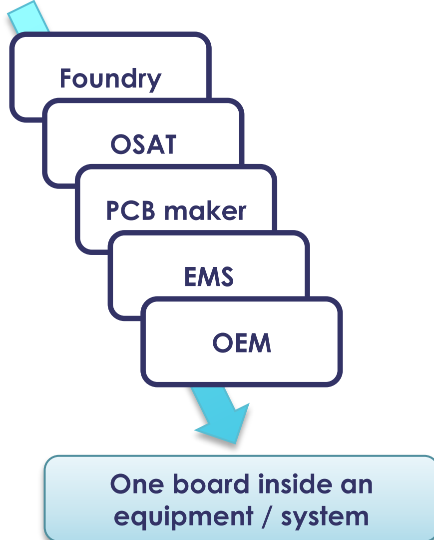
Example of PCB embedding: complex supply chain

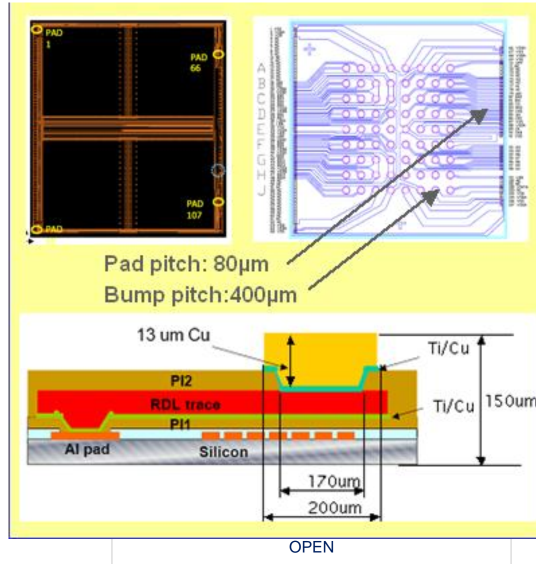
Chip / wafer post-process required for PCB embedding

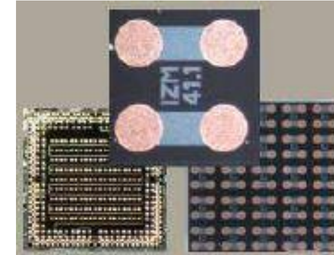
- RDL to adapt the die pitch to the PCB scale
- Wafer thinning
- Cu plating: Pad finish must be copper
- Thermal management can require 2 Cu faces metallization

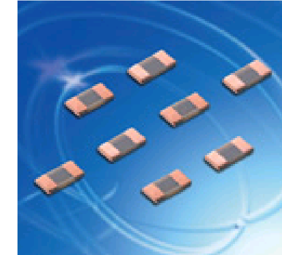


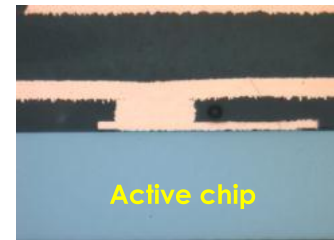
Si dies procurement hard point for low volume











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3D IC packaging supply chain

Fast evolution in service offered, from SME to large providers
Partner selection must fit with roadmap

Based on YOLE DÉVELOPPEMENT

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Focus on examples: PCBA technology / Lead-Free assembly

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Lead-free assembly

- July 2006 entry into force of EU directive
- Long transition period
  - Reballing & backward solution
- LF not yet used in harsh environments & for long mission profiles

Joint Group on Pollution Prevention

PCB material LF compatible

elfnet

Interposer

SAC reliability under thermomechanical loading (thesis)

COSAC project - mechanical

2002, 2003, 2004, 2005, 2006, 2007, 2008, 2009, 2010, 2011, 2012, 2013, 2014

Technology watch

Early assessment (Eolane)

Qualification fluxes, solder (pastes, wires) …

Backward (Celestica corporate)

Reballing

Backward solders (low voids)

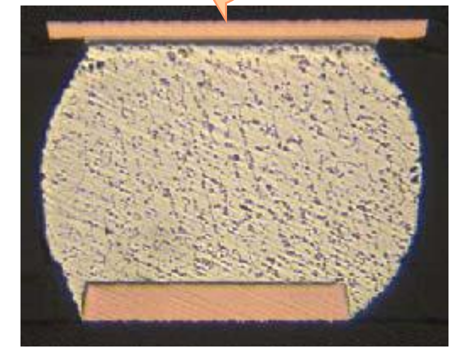
Cu dissolution

Backward (mechanical stresses)

CATS project (French MOD)

Backward SAC low Ag

Deployment of SnPb+ backward process



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Focus on examples: PCB technology / HDI boards with µvias

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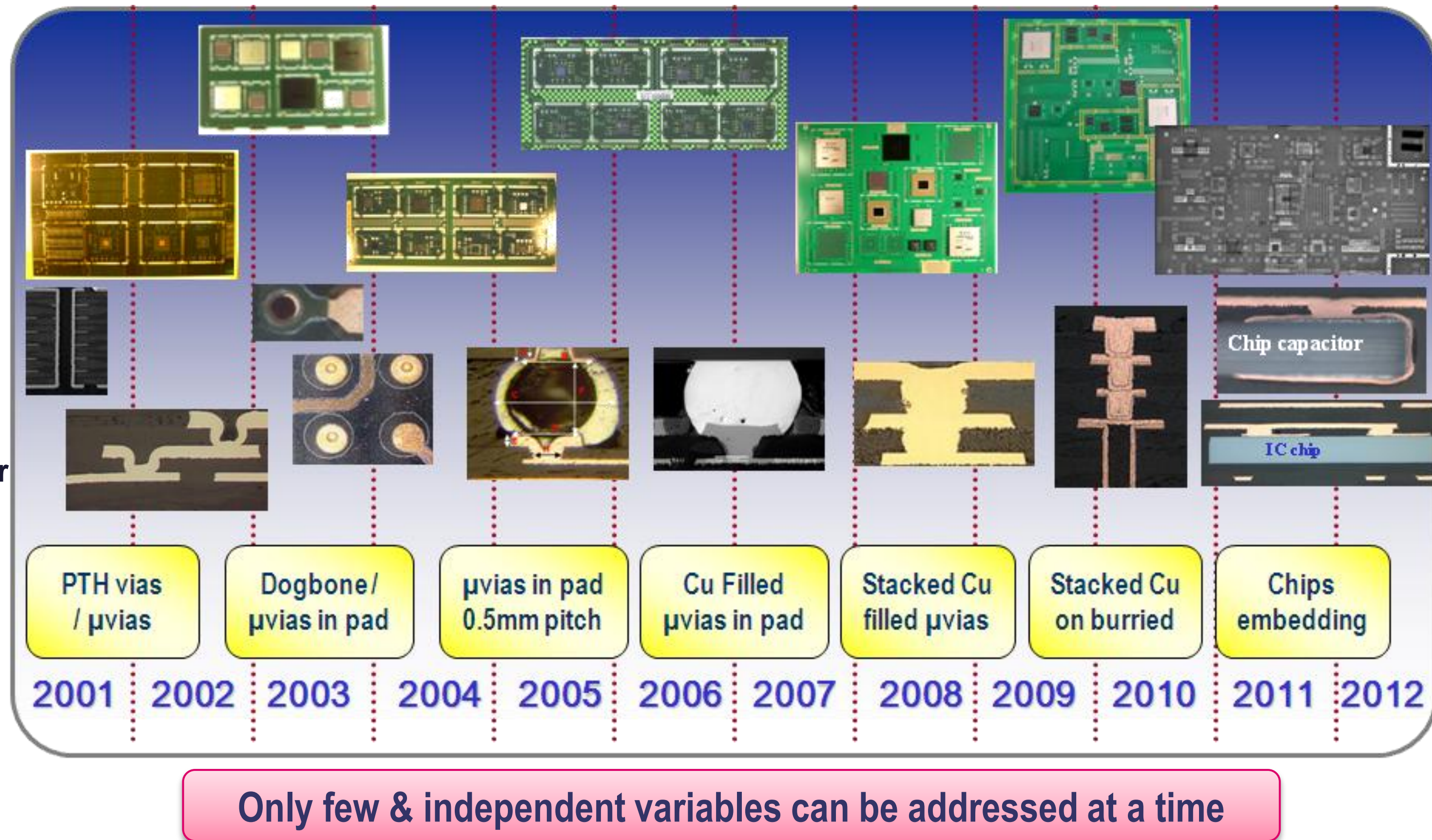
HDI boards

- ➢ Development of test vehicles
- ➢ Incremental learning
- ➢ DfM & DfR establishment
- ➢ Collaboration with industrial & academic partner

Long development time for high-end applications

- ➢ Stacked µvias used in Thales products



Only few & independent variables can be addressed at a time

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Technology/process introduction into new products

Reliability risk management is crucial before releasing a technology / process

- **Strong coupling with partners**
- **Process maturity required before reliability assessment**
- **Dedicated toolbox & methodologies to evaluate technologies & processes**

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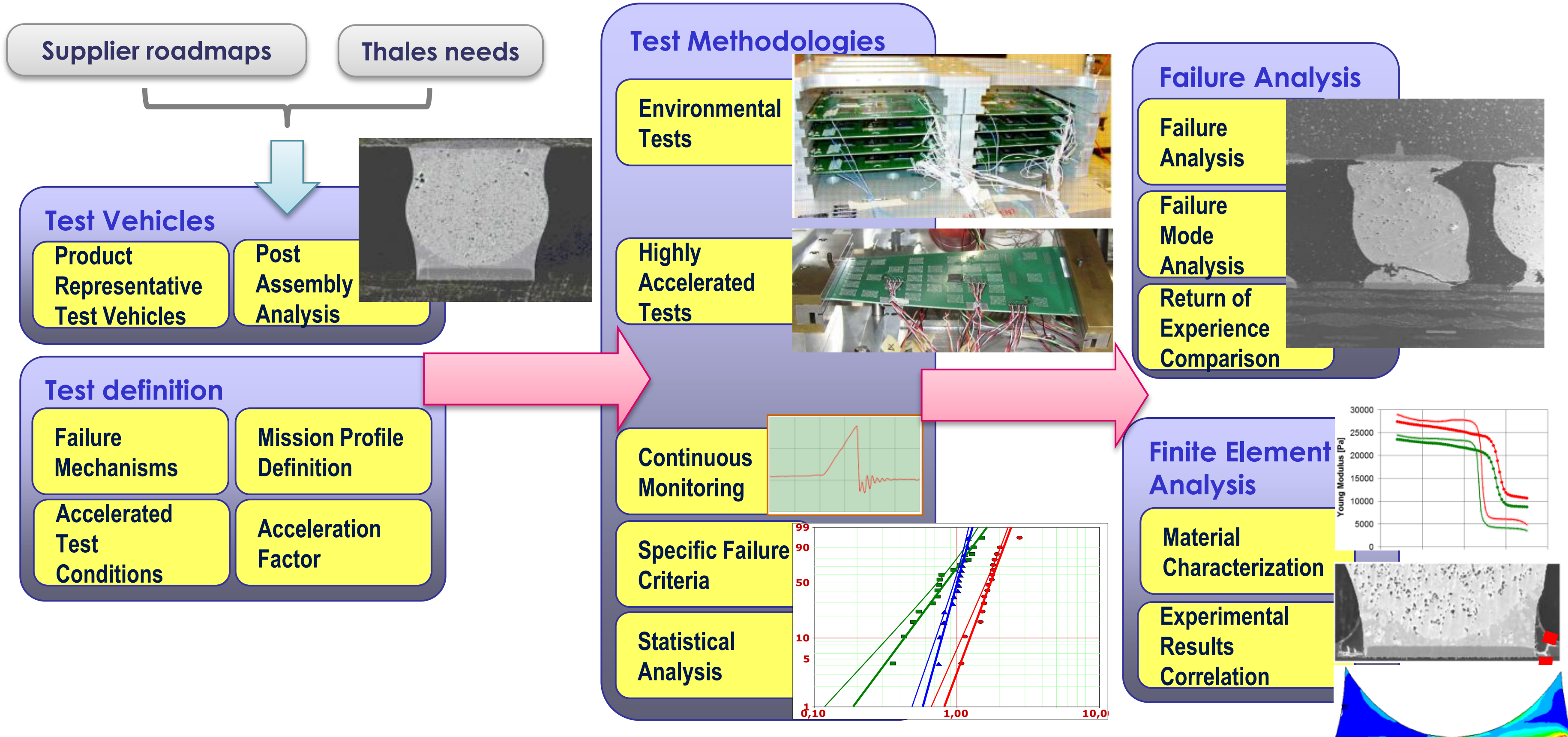
Tool box for advanced technologies / processes evaluation



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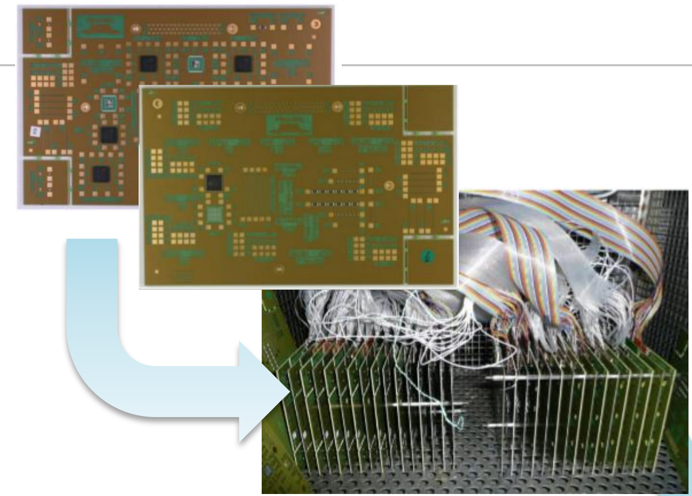
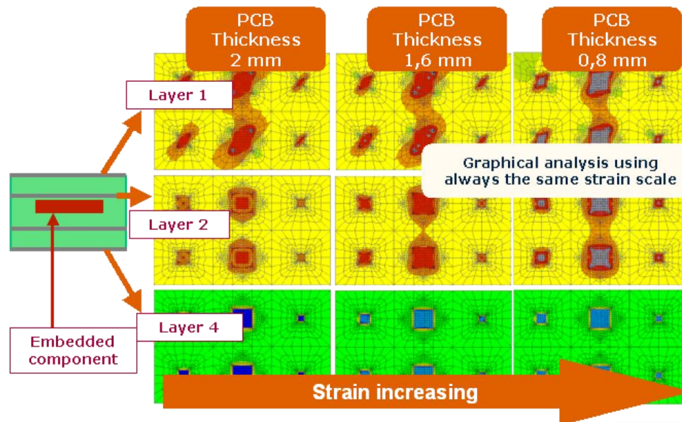
Establishment of DfM & DfR rules

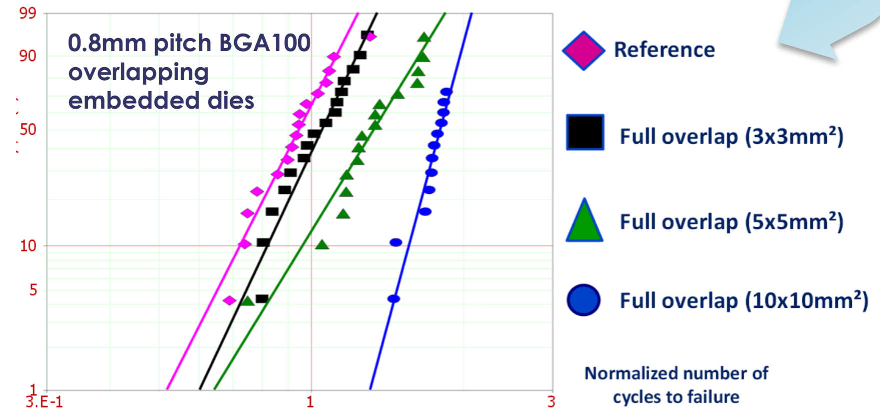


DfM & DfR rules establishment is performed through DoE

Simulation is a very useful tool for

- To understand failure mechanism in complement to experimental DoE results
- To vary key parameters in a shorter time with a calibrated simulation model
- To substitute by sensitivity analysis an unknown physical parameter value





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Conclusions

Packaging is a key differentiator for high density electronics & high reliability to:

- New generation of SIP are extremely complex
  - Take the benefit of the huge evolution of the Si and III-V
  - Mix technologies (MEMS, sensors, digital, analog, power…)
  - Couple electronics & mechanics
    - Manage the reliability risk including thermal management in harsh environment
- SIP / module using heterogeneous Technologies/Processes become mandatory
  - Therefore:
    - The supply chain is extremely complex
      - Management of Heterogeneous bricks linked with different "MRL"
      - In low volume, bare dies is a blocking point regarding procurement & Known Good Die

For High end electronics

- Considering the fast evolution of T/P driven by mass product
  - There is a strong need to develop T/P based on roadmap & in a frame of a network
    - In partnership with labs, institutes, spin off, SME…

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Thank you

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