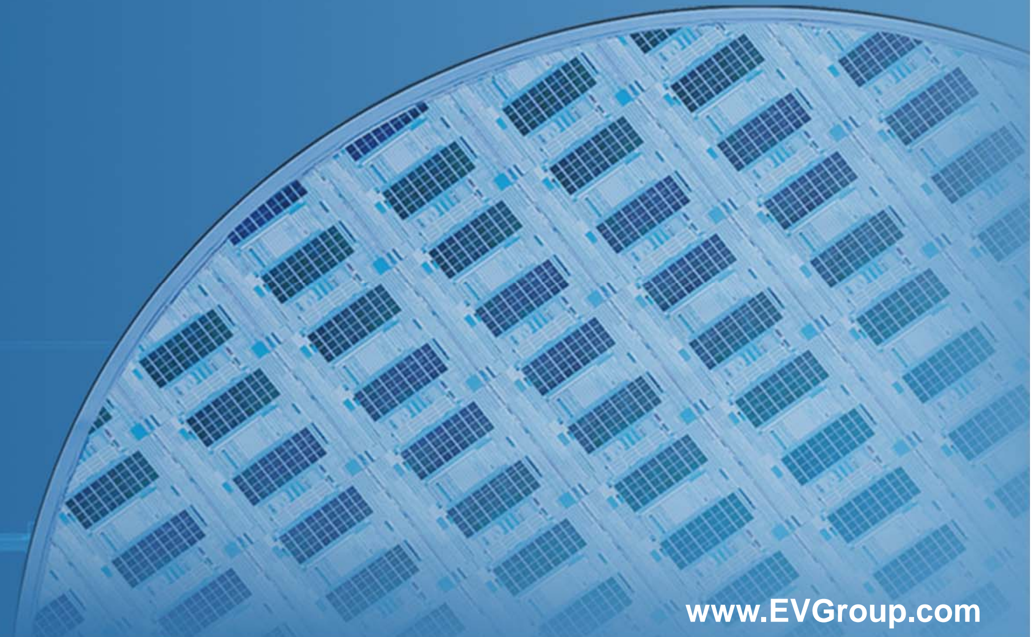
Prepared for and presented at Chemnitzer Seminar "System Integration Technologies", June 23-24, 2015

Oxide Free Direct Wafer Bonding

Anneliese Pönninger



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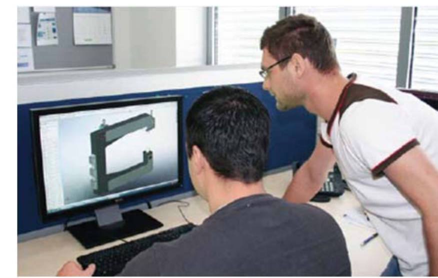
EVG

Outline

- Introduction
- Direct Wafer Bonding
- Oxide-free Direct Wafer Bonding
  - ComBond® Technology
- EVG®580 ComBond® Equipment
- Applications

EVG – At a glance

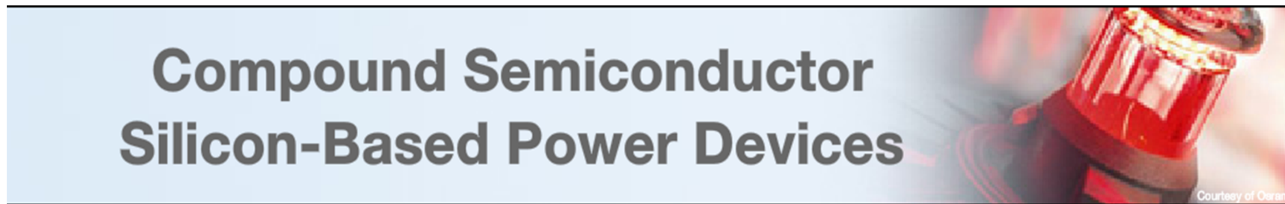
- Founded in 1980 by DI Erich and Aya Maria Thallner as an engineering partner for the semiconductor industry.
- Headquartered in Austria, with fully owned subsidiaries in the USA, Japan, South Korea, China and Taiwan; worldwide network of representatives.
- More than 700 employees globally, approx. 600 at EVG headquarters in Austria.
- Recognized technology and market leader in wafer processing solutions for semiconductor, MEMS and nanotechnology applications.
- Installed base in excess of 2,000 tools in high volume production as well as university and industrial R&D institutions worldwide.
- EVG continues to invest a large double digit percentage of its revenue in application-oriented research and development.



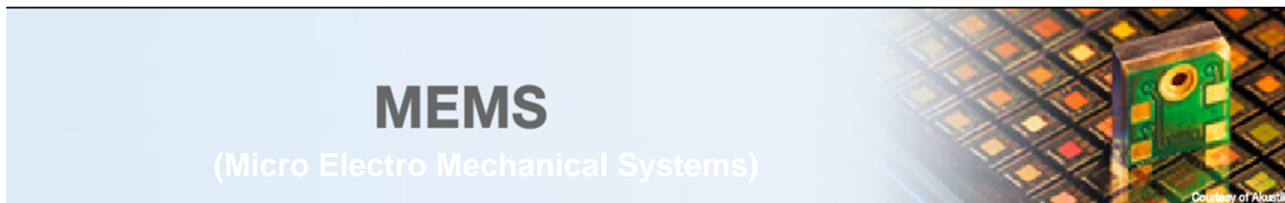
Markets and Typical End Products

EVG

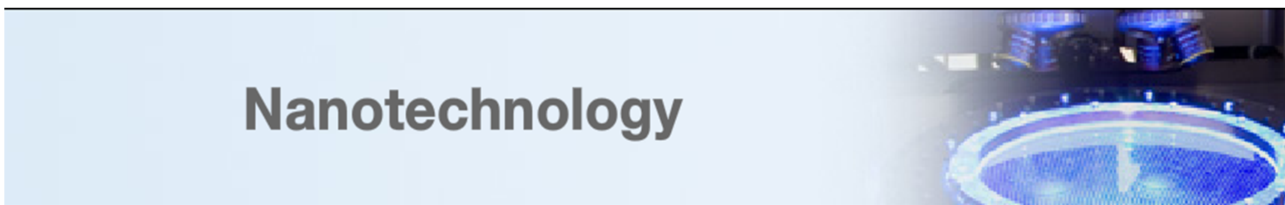
CMOS Image Sensors

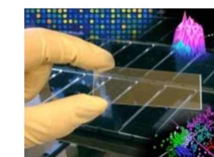


LEDs

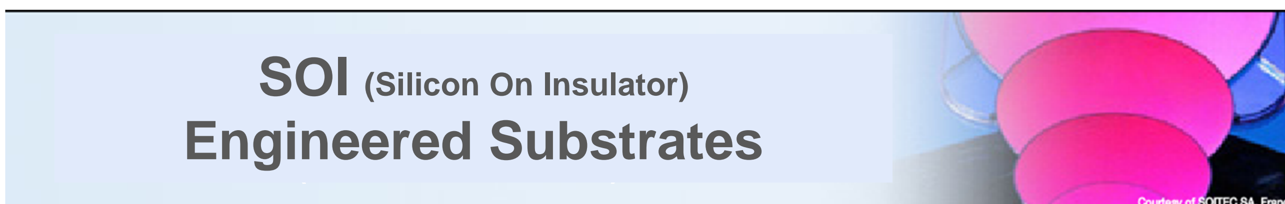


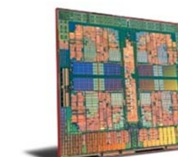
Motion sensors





DNA chips / micro labs





Micro processor wafers

Direct Wafer Bonding

Wafer Bonding: Overview

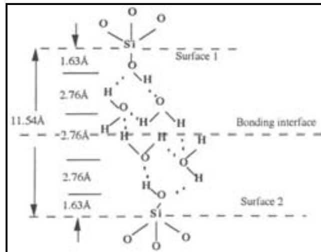
- WAFER BONDING
  - Direct Bonding
    - Molecular Bonding
    - Anodic Bonding
  - Bonding with Inter-Layers
    - Metal Bonding
      - Eutectic Bonding
      - Solder Bonding
      - Metal Thermo-Compression Bonding
    - Glass Frit Bonding
    - Adhesive Bonding
      - UV Cured Polymer
      - Thermally Cured Polymer

Direct Wafer Bonding Characteristics

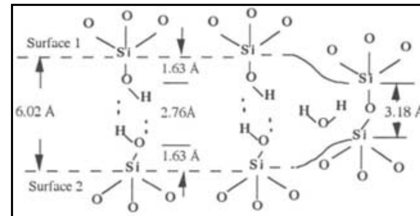
- Initial spontaneous bonding occurs when surfaces are brought into physical contact.
- Covalent bonds between surfaces formed during application of heat.
- The resulting bond strength is as high as the bulk fracture strength.
- The resulting bond is permanent.

Classical and Plasma Activated Fusion Bond

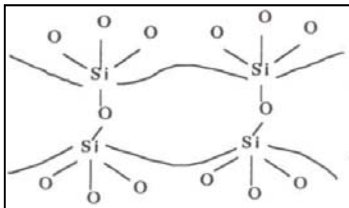
1 Van-der-Waals bonds



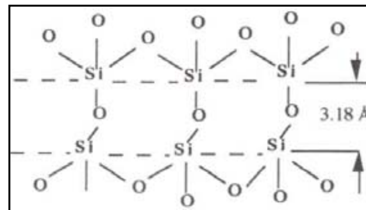
2 Water diffusion

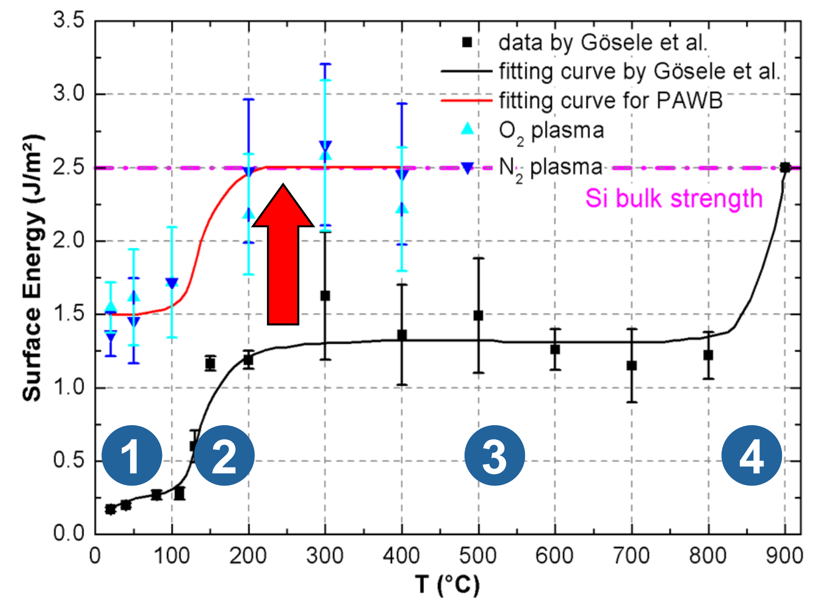


3 Formation of covalent bonds



4 Closure of nano-gaps





- Classical:
  SiO_2 viscosity due to high temperature annealing
- Plasma activated:
  Enhanced diffusion at low temperatures

Plasma Activated Wafer Bonding

- **Requires thick oxide** in the interface

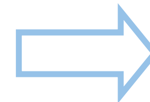
Thick oxide →

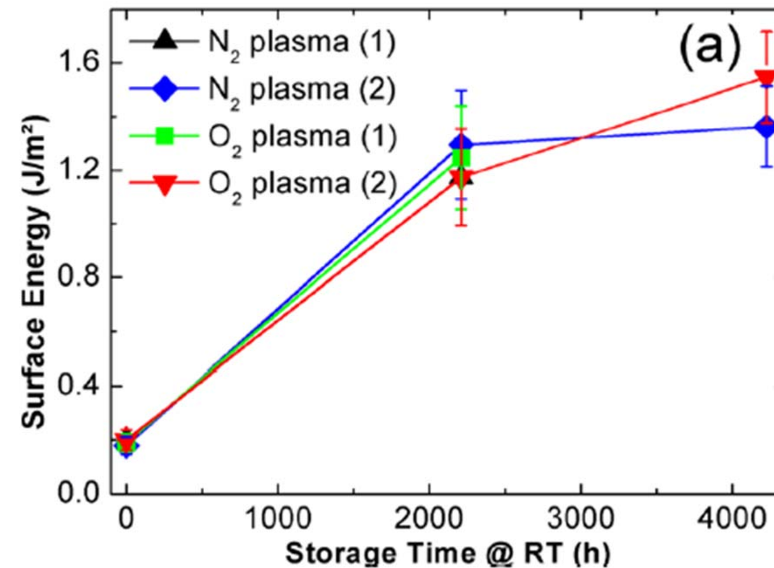
Electrical resistance →

Conductive interfaces not possible

- **RT** covalent bonding **possible**, but industrially **not practical**

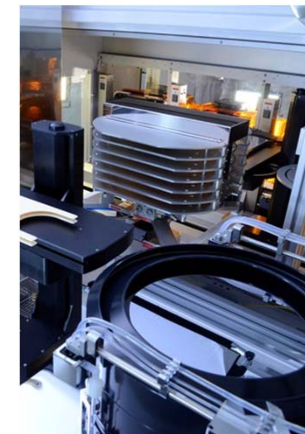
Room temperature process not viable





EVG®810LT LowTemp™
Plasma Activation System

Gemini ® FB
Automated Production
Fusion Bonding System



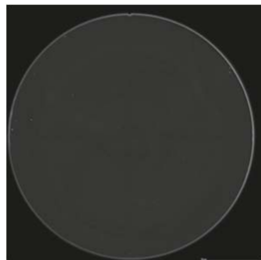
See: T. Plach, K. Hingerl, S. Tollabimazraehno, G. Hesser, V. Dragoi and M. Wimplinger, *J. Appl. Phys.*, **113**, 094905 (2013).

Oxide-free Direct Wafer Bonding

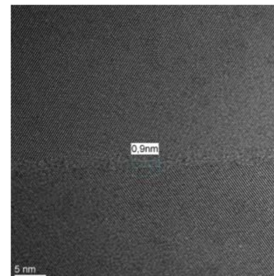
ComBond ® Technology

Motivation for ComBond®

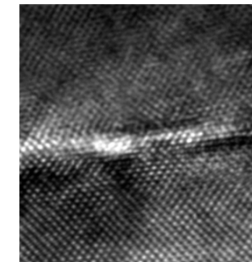
- Motivation
  - Covalent bonding technology
    - Oxide-free, conductive interface
    - Room temperature or low temperature process
  - Applications
    - Heterogeneous integration
    - Layer transfer for advanced substrates
    - Improved metal/metal bonding
    - High vacuum encapsulation (MEMS)



Particle-free and void free bonding



Si/Si bond interface – minimum amorphous layer



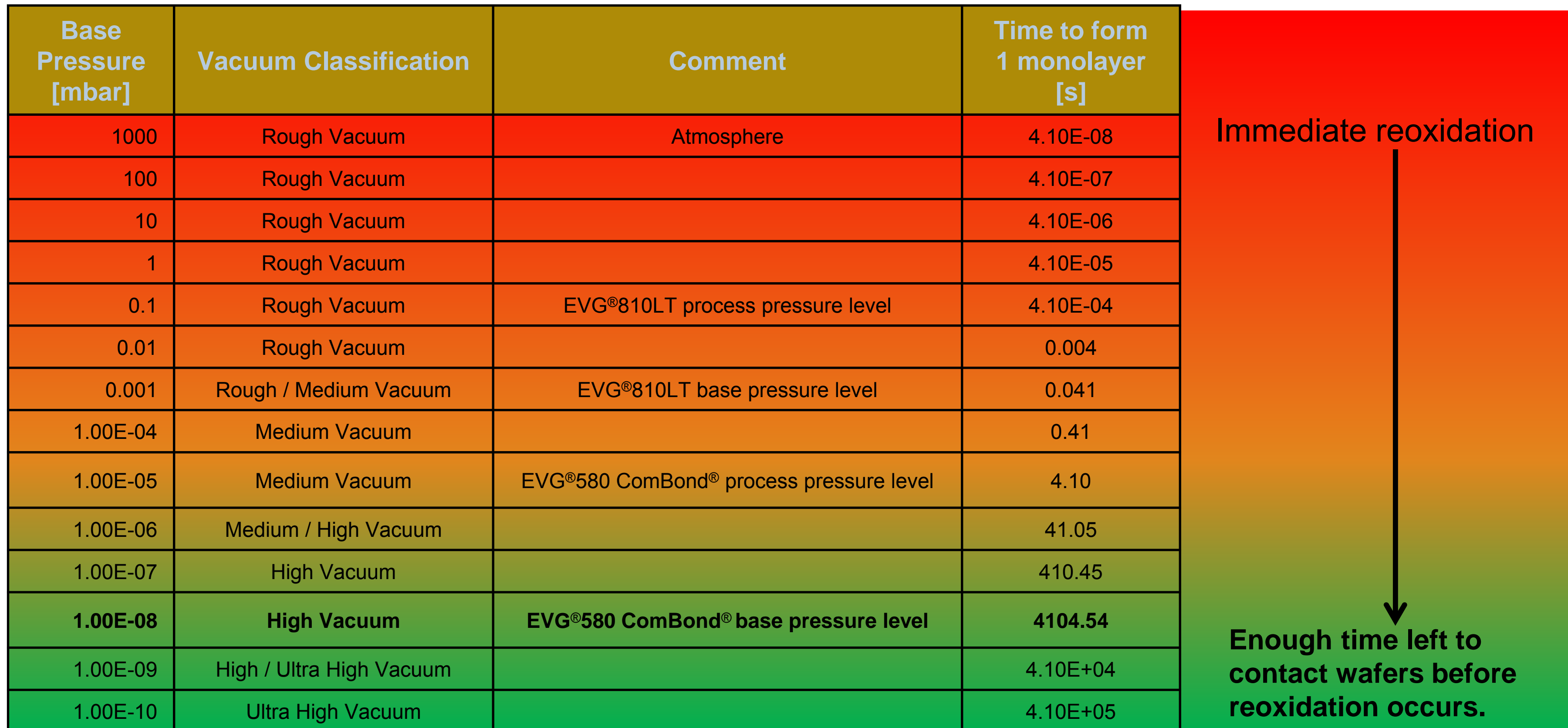
GaAs/InP bond interface – minimum amorphous layer

ComBond® Process

- Requirements
  - Surface activation (oxide removal, avoid roughness increase)
  - High vacuum (retain oxide-free surface)
  - Low (room) temperature bonding process (retain crystal structures, minimize amorphous layer growth, avoid stresses due to CTE mismatch)
- Solutions
  - **ComBond®:** Gentle surface sputtering using energized projectiles of an inert gas effectively removes oxides and other molecular contaminations. Re-oxidation is prevented by processing in high or ultra high vacuum.

ComBond® Process

- ***Why does ComBond® require high vacuum?***
  → If an oxide-free interface is required, it is not enough to remove the oxide. Re-deposition of oxide needs to be prevented, as well.



Base Pressure [mbar]	Vacuum Classification	Comment	Time to form 1 monolayer [s]
1000	Rough Vacuum	Atmosphere	4.10E-08
100	Rough Vacuum		4.10E-07
10	Rough Vacuum		4.10E-06
1	Rough Vacuum		4.10E-05
0.1	Rough Vacuum	EVG®810LT process pressure level	4.10E-04
0.01	Rough Vacuum		0.004
0.001	Rough / Medium Vacuum	EVG®810LT base pressure level	0.041
1.00E-04	Medium Vacuum		0.41
1.00E-05	Medium Vacuum	EVG®580 ComBond® process pressure level	4.10
1.00E-06	Medium / High Vacuum		41.05
1.00E-07	High Vacuum		410.45
1.00E-08	**High Vacuum**	**EVG®580 ComBond® base pressure level**	**4104.54**
1.00E-09	High / Ultra High Vacuum		4.10E+04
1.00E-10	Ultra High Vacuum		4.10E+05

Assumptions:

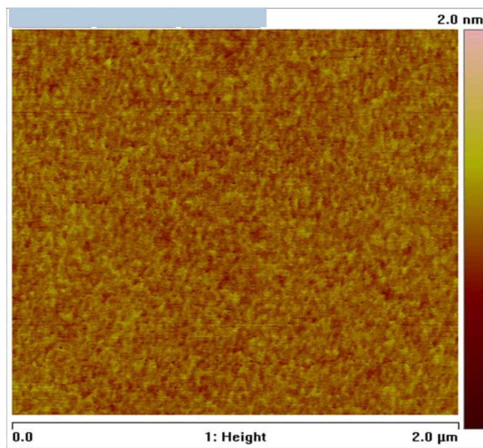
- Each H_2O molecule from background contamination that hits the Si surface will stick.
- H_2O partial pressure is 10 % of base pressure.

ComBond® Achievements

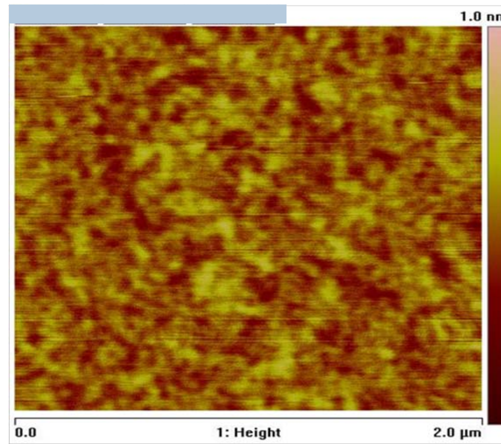
- High vacuum process (<10^{-8} mbar)
- Surface activation and oxide-removal
- Room (low) temperature bonding
  - Oxide-free interface
  - Minimum thickness of amorphous layers
  - Minimum crystal dislocations

ComBond® Process Results

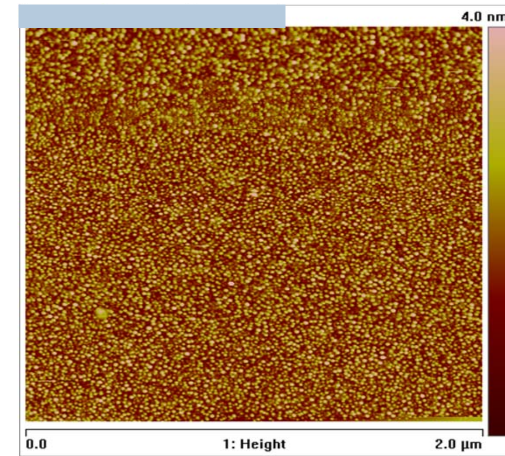
- Surface activation
  - Dry etching with energized particles
  - Uniform oxide removal
  - Low surface roughness increase



Silicon: Roughness RMS(R_q) <0.1nm



GaAs: Roughness RMS(R_q) <0.1nm



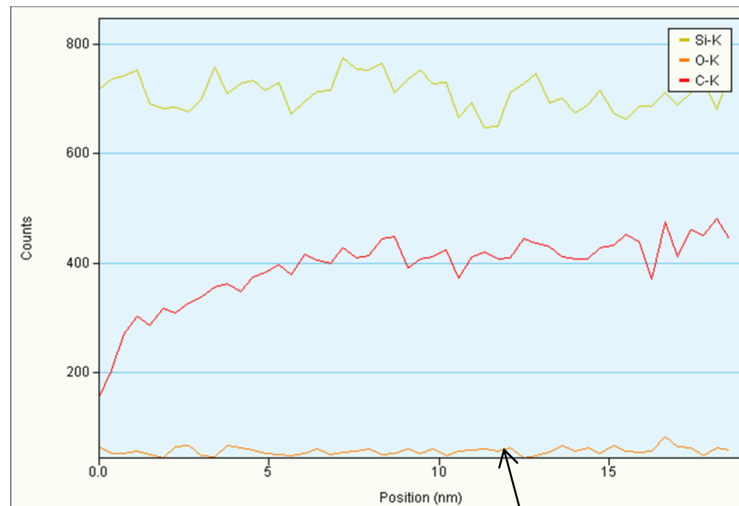
InP: Roughness RMS(R_q) <0.6nm

ComBond® Process Results

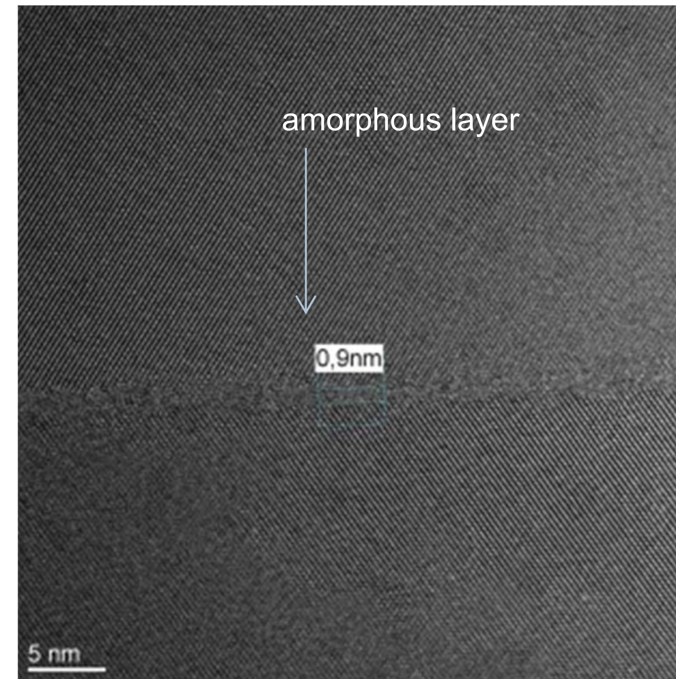
- Si-Si Bond

HR-TEM image reveals an amorphous layer of <1 nm thickness in the bond interface.

Oxide-free!



Oxygen signal



Si/Si: amorphous layer thickness <1nm

ComBond® Process Results

★ ComBond®

HB:hydrophobic

HL:hydrophilic

HL Si/Si

HB Si/Si

Surface energy (mJ/m²)

3000
2500
2000
1500
1000
500
0

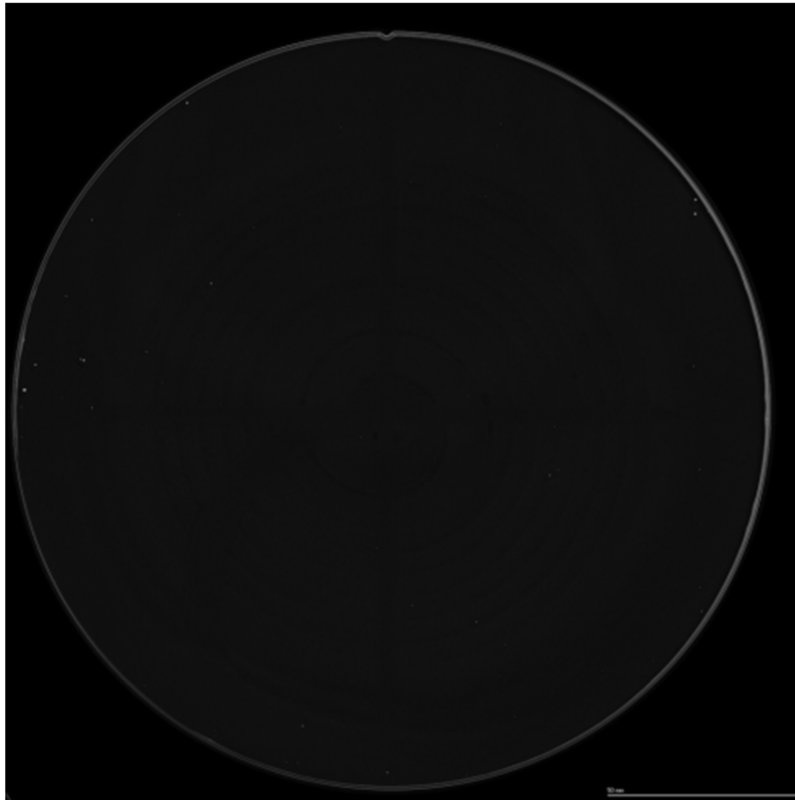
0 100 200 300 400 500 600 700 800 900

Annealing temperature (°C)

ComBond® Process Results

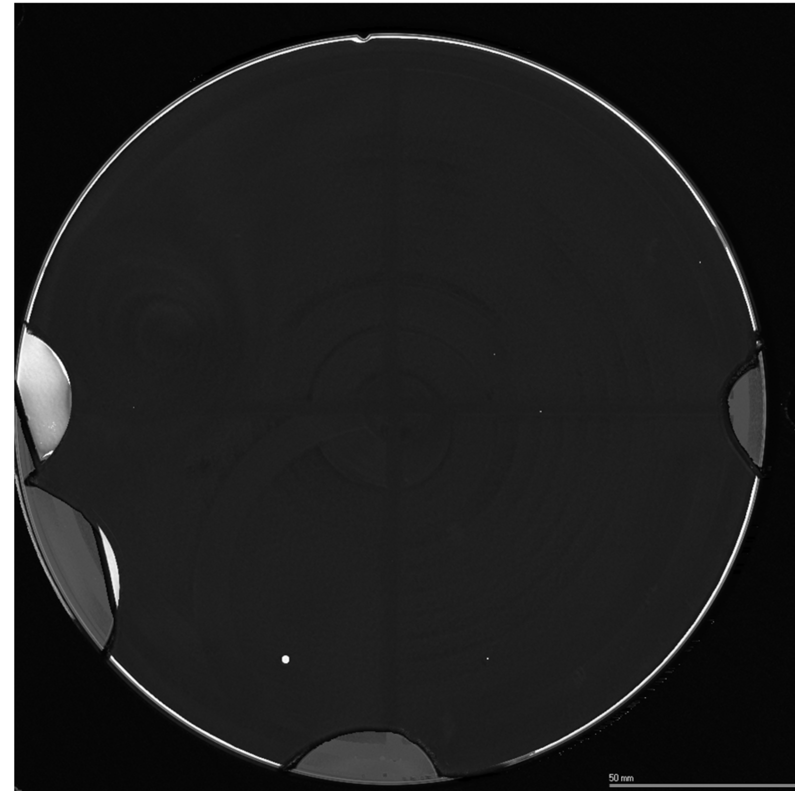
C-SAM scan

Example 1



Si/Si

Example 2

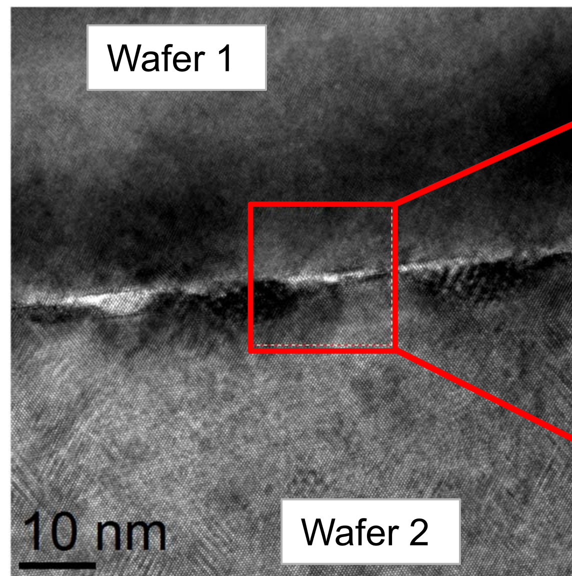


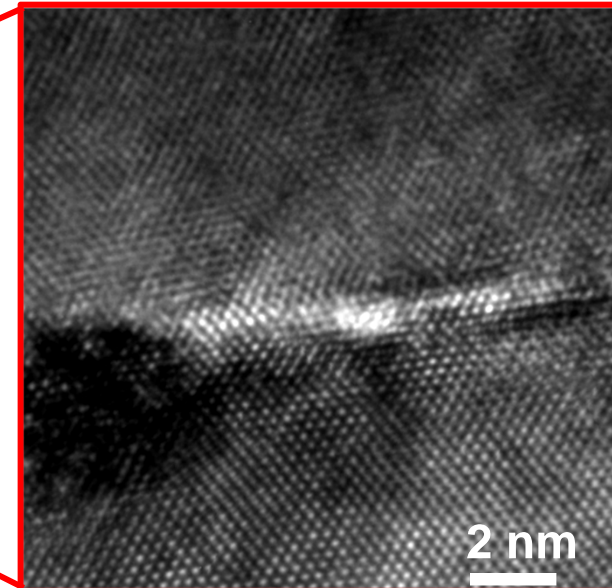
Si/Si

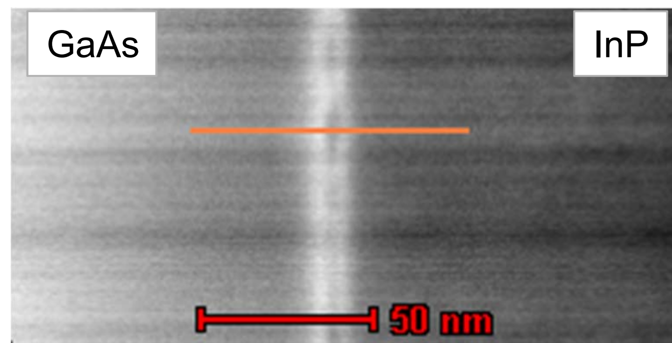
Bond strength > 2.5 J/m² (all measurement positions broken)

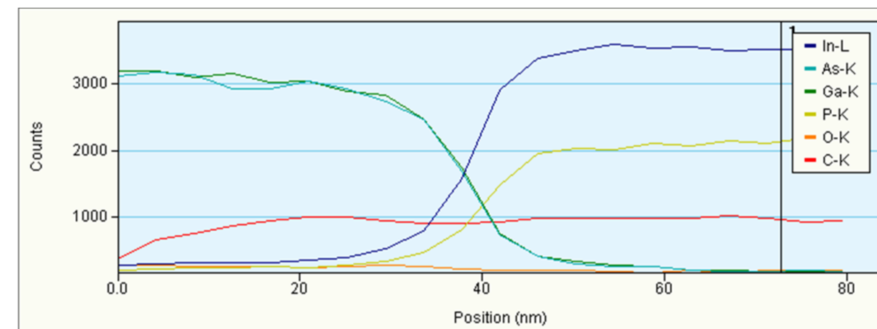
ComBond® Process Results

GaAs / InP wafer bonding









Oxide-free Interface!

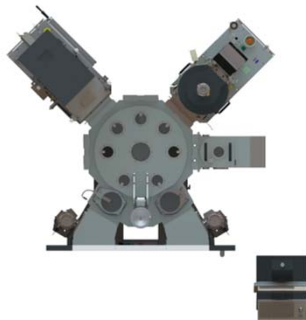
Equipment Soultions

EVG580® ComBond®

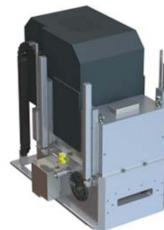
EVG®580 ComBond® Equipment

- Requirements
  - Surface activation (oxide removal, avoid roughness increase)
  - High vacuum (retain oxide-free surface)
  - Low (room) temperature bonding process (retain crystal structures, minimize amorphous layer growth, avoid stresses due to CTE mismatch)
- Solutions

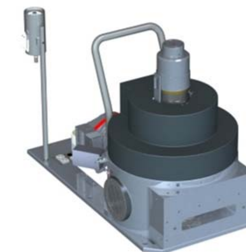
High Vacuum System



CAM (ComBond Activation Module)

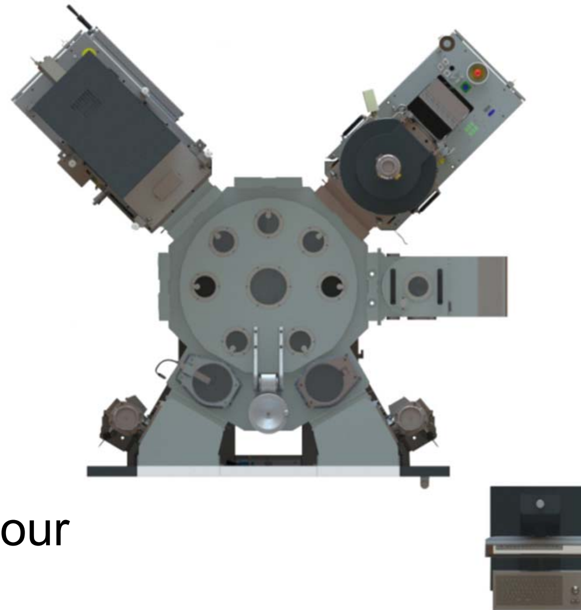


Bond Module



EVG®580 ComBond® Equipment

- Fully automated high vacuum system
- Modular design
- Flexible configuration
- Cassettes or EFEM
- Wafers up to 200 mm
- Throughput: 20 units / hour



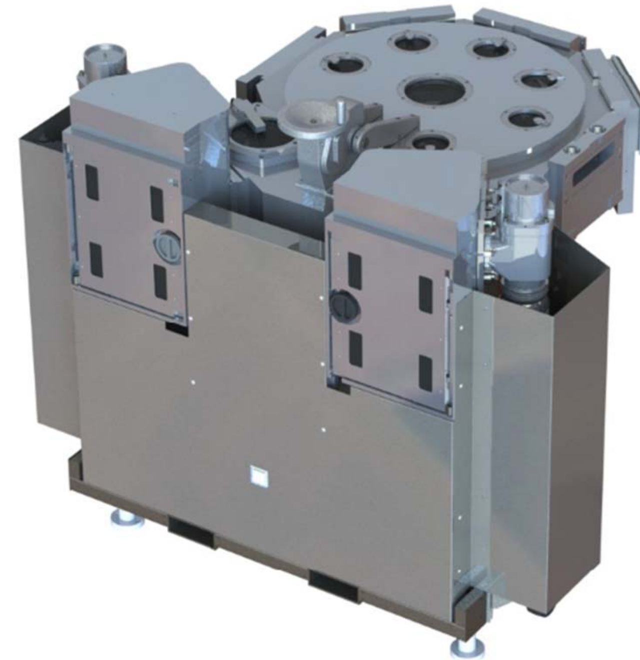
BASIC FUNCTIONS
Vacuum bake
Optical pre-aligner
Robot unit with end-effector(s) and controllers
Vacuum system with gauge, turbomolecular and roughing pump
View ports
Wafer flipping

VACUUM CAPABILITY	Pressure [mbar]
Handling system	$< 7*10^{-8}$
Cassette load lock	$<1*10^{-6}$
CAM module	$< 9*10^{-8}$
Bond module	$< 9*10^{-8}$

CONFIGURATIONS	3 Process Modules	5 Process Modules	6 Process Modules
Wafer size	up to 200 mm	up to 200 mm	up to 200 mm
Load lock	1 cassette station or 1 manual load port	2 cassette stations or EFEM with up to 4 cassettes	2 cassette stations or EFEM with up to 4cassettes
CAM module	1	2	2
Bond chamber	1	1	1
Free ports		1	2
Robot	Single arm	Dual arm	Dual arm

EVG®580 High Vacuum Cluster

- Operated at base pressures < 7×10^{-8} mbar
- Maintains the fully automated wafer transport and handling
- Maximum six process modules
- Maximum wafer stack height 4 mm
- Buffer station for up to two wafers
- Single or dual arm robot
- Integrated bake out
- Optical prealigner
- Automatic wafer centering sensor
- Optical sensor for wafer detection
- Load lock
  - Manual, cassette, EFEM loading
  - Double pitch cassette for up to twelve wafer
  - Pressure recovery 3 minutes to ≤ 6×10^{-5} mbar
  - High speed vent (vacuum to atm) ~ 1 min

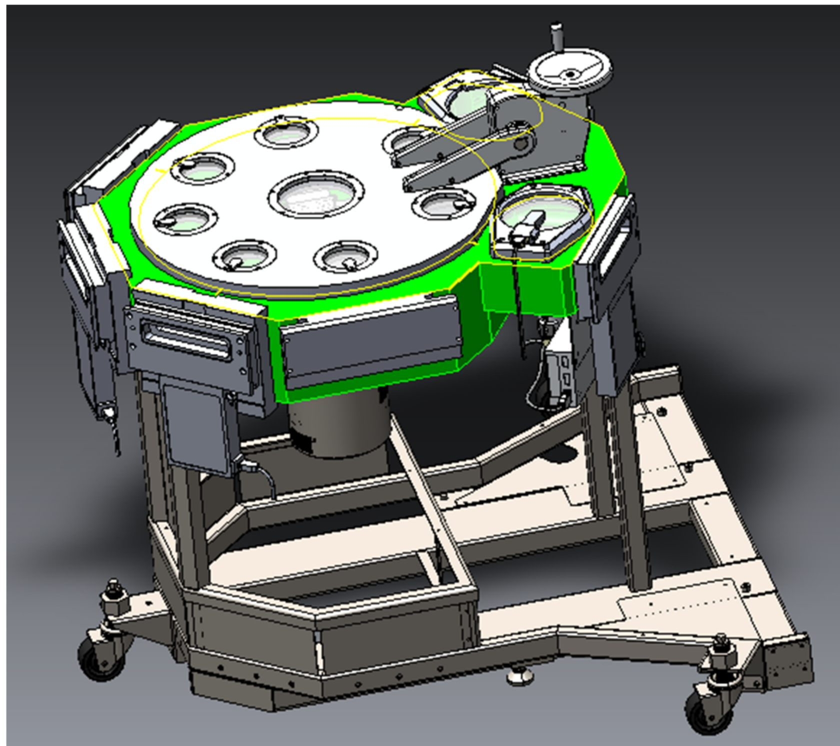


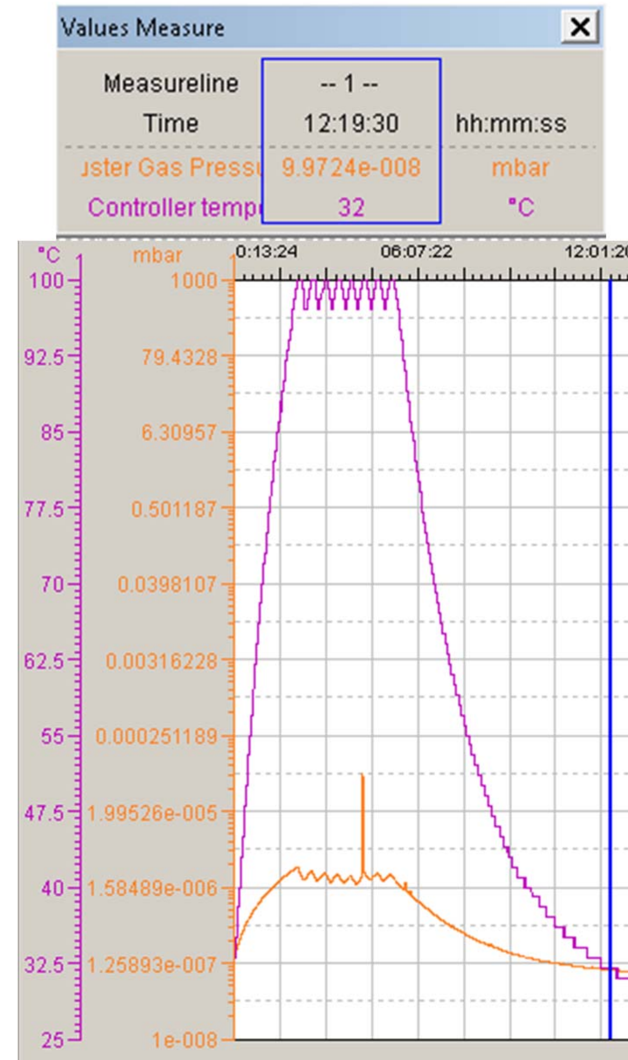
High Vacuum Handling System Transport Chamber

- Bake out of chamber wall
- Base pressure (with bake < 24h)

  < 1 x 10^{-7} mbar Turbo pump

  < 7 x 10^{-8} mbar Cryo pump (optional)

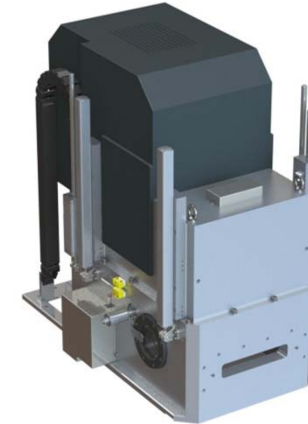




EVG®580 ComBond® Activation Module (CAM)

- ComBond® Activation Module (CAM)

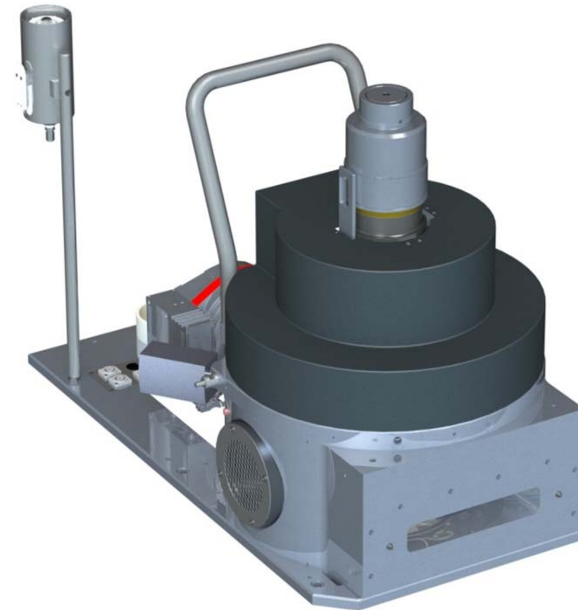
  Surface modification treatment to allow covalent bonding at or near room temperature.
- The CAM surface treatment technology achieves
  - Oxide-free and particle-free surfaces
  - Low surface roughness
  - Uniform oxide removal and surface activation
  - High throughput
- Process chamber pressure
  - Base pressure < 9×10^{-8} mbar
  - Process pressure ~1×10^{-5} mbar



CAM Specifications	
Roughness increase	< 0.1 nm
Cleanliness	< 1×10^{10} metal ions / cm^2 < 5 particles (> 0.2 µm) added per wafer
Oxide removal (Si)	up to 15 nm / min

EVG®580 Bond Module

- Electrostatic chucks
- Heated and not heated version
- Enhanced vacuum level of
  $< 9 \times 10^{-8}$ mbar
- Open space between heaters of
  25 mm for enhanced outgassing
- Active water cooling of top and bottom heaters



EVG 580 Bond Module	Technical Data
Piston force	Up to 100 kN
Maximum temperature	400 °C
Heating rate	45 °C / min
Wafer stack height	< 4 mm
Purge gas lines	1

EVG®580 ComBond® Configurations

	1	2	3	4	5
Configuration					
Process Modules	3	5	5	6	6
Cassette Station	1 (12 slot cassette) optional single substrate loading (up to 2 substrates)	2 (12 slot cassette)	up to 4 (25 slot cassette)	2 (12 slot cassette)	up to 4 (25 slot cassette)
*Estimated Throughput [Wafer/h]	~ 8	~ 13	~ 15	~ 16	~ 20

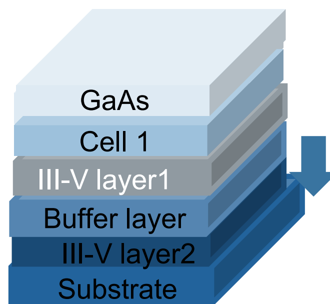
*calculated with current BKM Recipe and max. amount of process modules

Applications

Heterogenous integration, layer transfer, MEMS,..

Applications - Examples

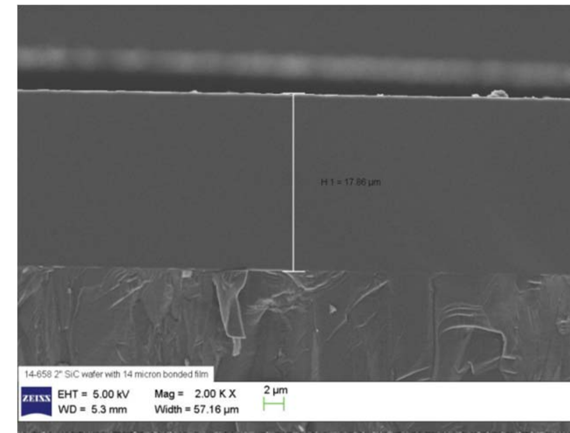
- Multi-junction solar cells based on III-V semiconductors



- Bond forms cell 2

- Bonding of solar cell stacks to bottom cells
- Bonding of III-V layers to form a cell structure with certain wavelength sensitivity
- Any combination possible (CS on CS or Si, Ge,.)
- Certain buffer layers not required
- Room temperature bonding process
- Electrically conductive bond interface

- Power Devices



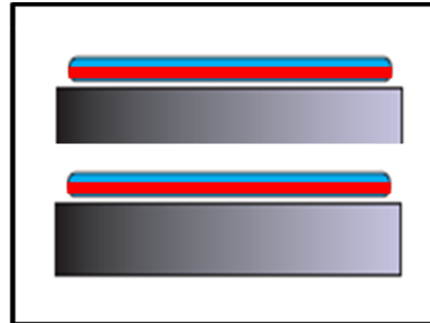
Crystalline SiC on polycrystalline SiC*

- Vertical Power Devices need conducting interface
- Oxides can act as trap states increasing resistance and reducing device performance
- Engineered substrates as growth templates can save costs

*ComBond Result, Courtesy of GT Advanced Technology

EVG

- **Improved Vacuum Encapsulation**
- Wafers are baked out prior to aligning and clamping.
  - Will be open faced



  - Much larger spacing then when clamped
    - Typical clamp thickness is 100-200µm
    - Stacked bakeout module will can have spacing of 10-20mm
  - This increased spacing improves the desorption of water molecules from the surface of the wafer by increasing the probability that the desorbed water molecule will 'escape'

Summary

- Surface activation is needed to achieve superior bonding quality at low temperatures through formation of covalent bonds

- Advanced applications need advanced surface activation methods to
  - Encapsulate high vacuum (MEMS)
  - Remove surface oxides
  - Eliminate the need for thermal annealing

- EVG®580 ComBond® represents a solution to such advanced application demands

- **Proven facts**: EVG®580 ComBond® and its CAM are capable to
  - Maintain **high vacuum levels** at ~ 10^{-8} mbar
  - Perform with **highest cleanliness**
  - Effectively **remove surface oxides** on various wafer materials
  - Retain or **even improve** surface roughness after activation
  - Produce **real room temperature** Si-Si wafer bonds with **maximum bond strength**

Thank you!

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