

**[Chemnitzer Seminar 23th June, 2015]
A 3D stacked CMOS image sensor with
16Mpixel global-shutter mode using
4 million interconnections**

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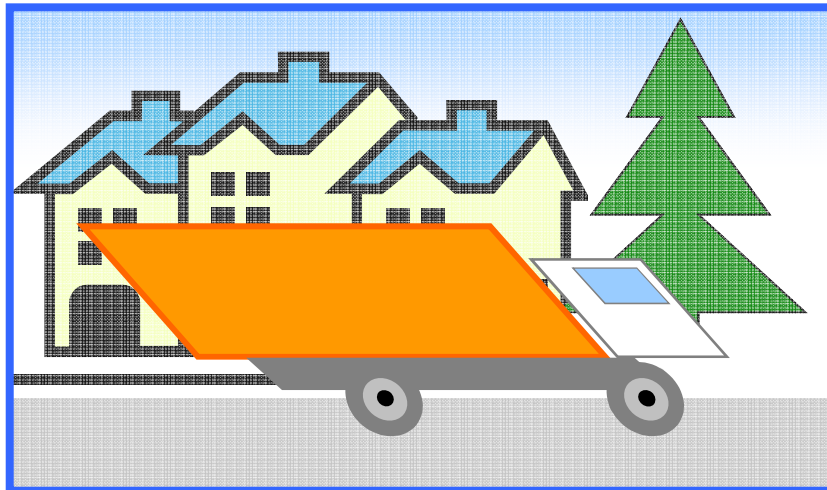
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Conventional Image Sensor

Rolling shutter (RS) operation

- ▶ To prevent “rolling shutter distortion”,
mechanical shutter is necessity.

Rolling shutter image sensor : line by line exposure
=> It has the distortion when captured moving target



Background (Motivation)

Global shutter (GS) CMOS image sensor (CIS) ideal for digital cameras

- ▶ **No rolling shutter distortion/no mechanical shutter**

- High speed continuous shooting

- Seamless shooting between still mode and movie mode

- No black-out period for electronic view finder



Our Targets

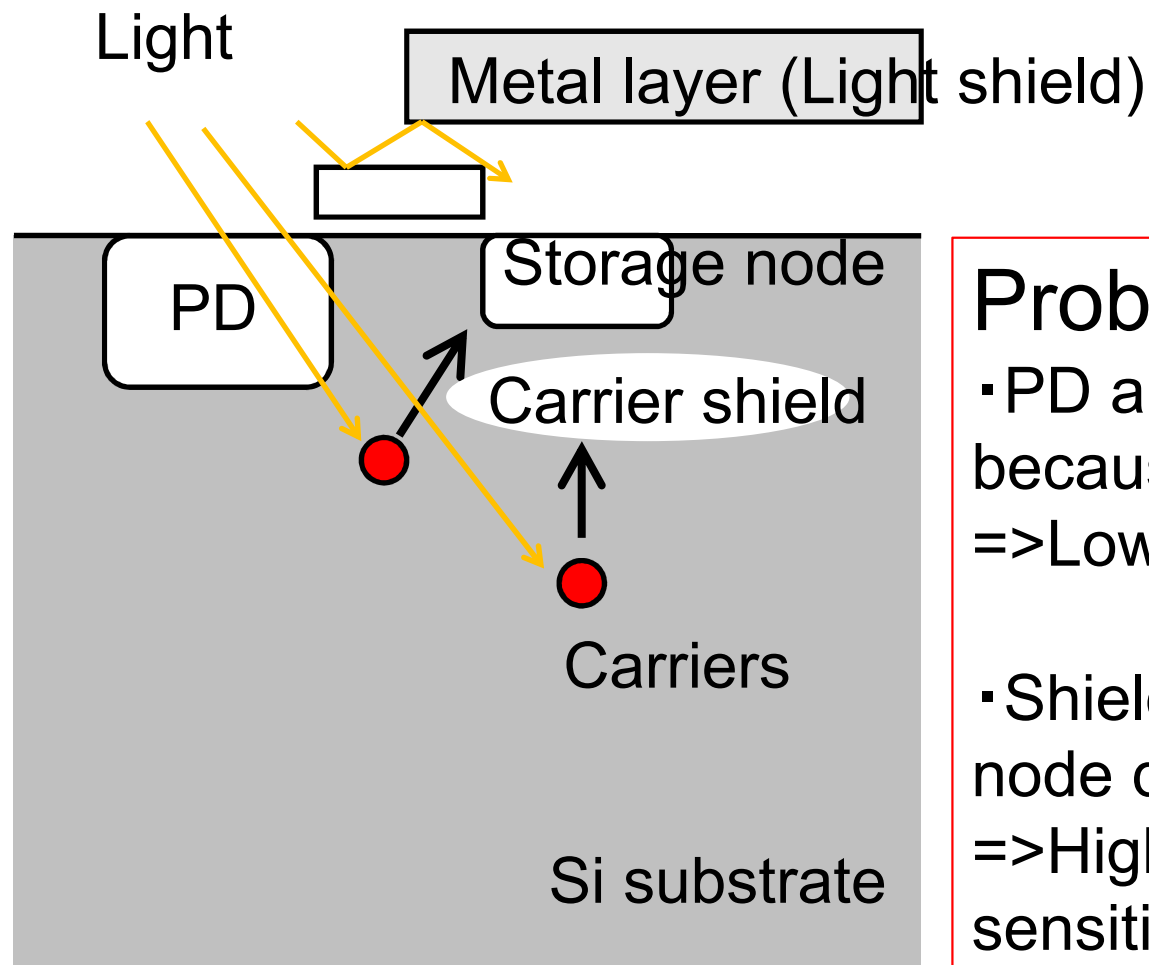
To develop a GS image sensor for digital cameras with:

- ▶ **High resolution: 16M pixels**
- ▶ **High image quality: 3.8-um BSI pixel**
- ▶ **No artifacts: small parasitic light sensitivity**



General Problems of Global Shutter CIS

Storage node in same substrate as Photo Diode (PD)
Storage node beside PD

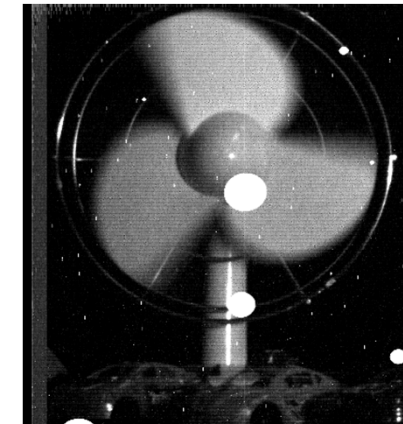
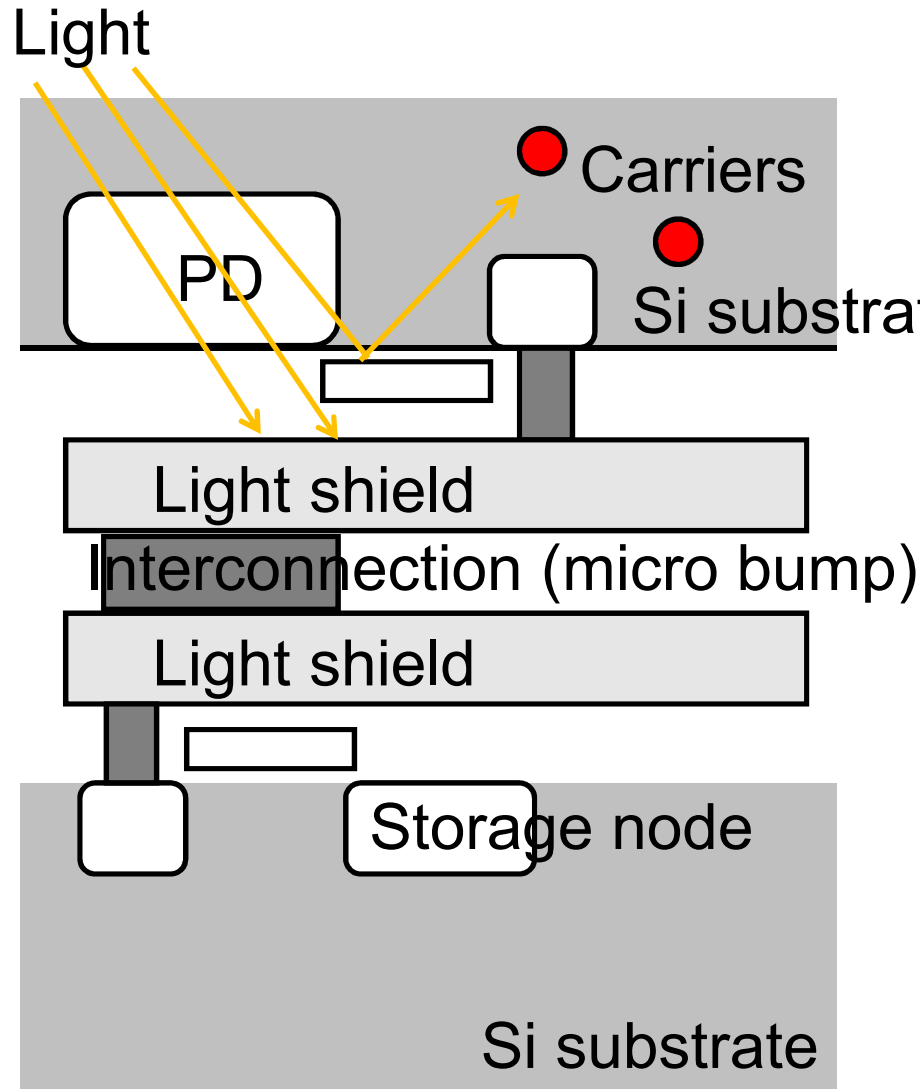


Problems

- PD area decreased because of storage node => Low full well capacity
- Shielding light to storage node difficult => High parasitic light sensitivity

Our Previous Work (ISSCC2013)

3D stacking technology with micro bumps



| | |
|-----------------------------------|-------------------|
| Chip size | 6.5 × 6.5 mm |
| Effective pixels | 704 (H) × 512 (V) |
| Pixel size | 4.3 × 4.3 μm |
| Number of interconnections | 90,112 |
| Minimum pitch of interconnection | 8.6 μm |
| Parasitic light sensitivity (PLS) | -160 dB |

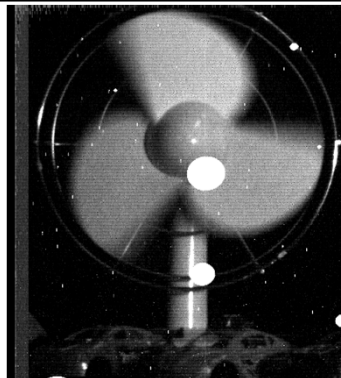
FSI, BSI, 3D stacked image sensor

| | FSI | BSI | 3D stacked |
|-----------|--|--|---|
| Structure | <p>Light</p> <p>Si</p> <p>PD</p> <p>Metal</p> | <p>Light</p> <p>Si</p> <p>PD</p> <p>Metal</p> <p>Support wafer</p> | <p>Light</p> <p>Si</p> <p>PD</p> <p>Metal</p> <p>Circuit wafer</p> |
| Feature | <ul style="list-style-type: none"> • Easy to fabricate | <ul style="list-style-type: none"> • PD can receive much more light • Pixel metal layout is easier | <ul style="list-style-type: none"> • Higher functionality • Higher performance |
| Process | <ul style="list-style-type: none"> • Normal CIS process | <ul style="list-style-type: none"> • Wafer bonding • Wafer thinning | <ul style="list-style-type: none"> • Wafer bonding • Inter connection • Wafer thinning |

Our New Work

ISSCC2013

| | |
|-----------------------------------|-------------------|
| Chip size | 6.5 × 6.5 mm |
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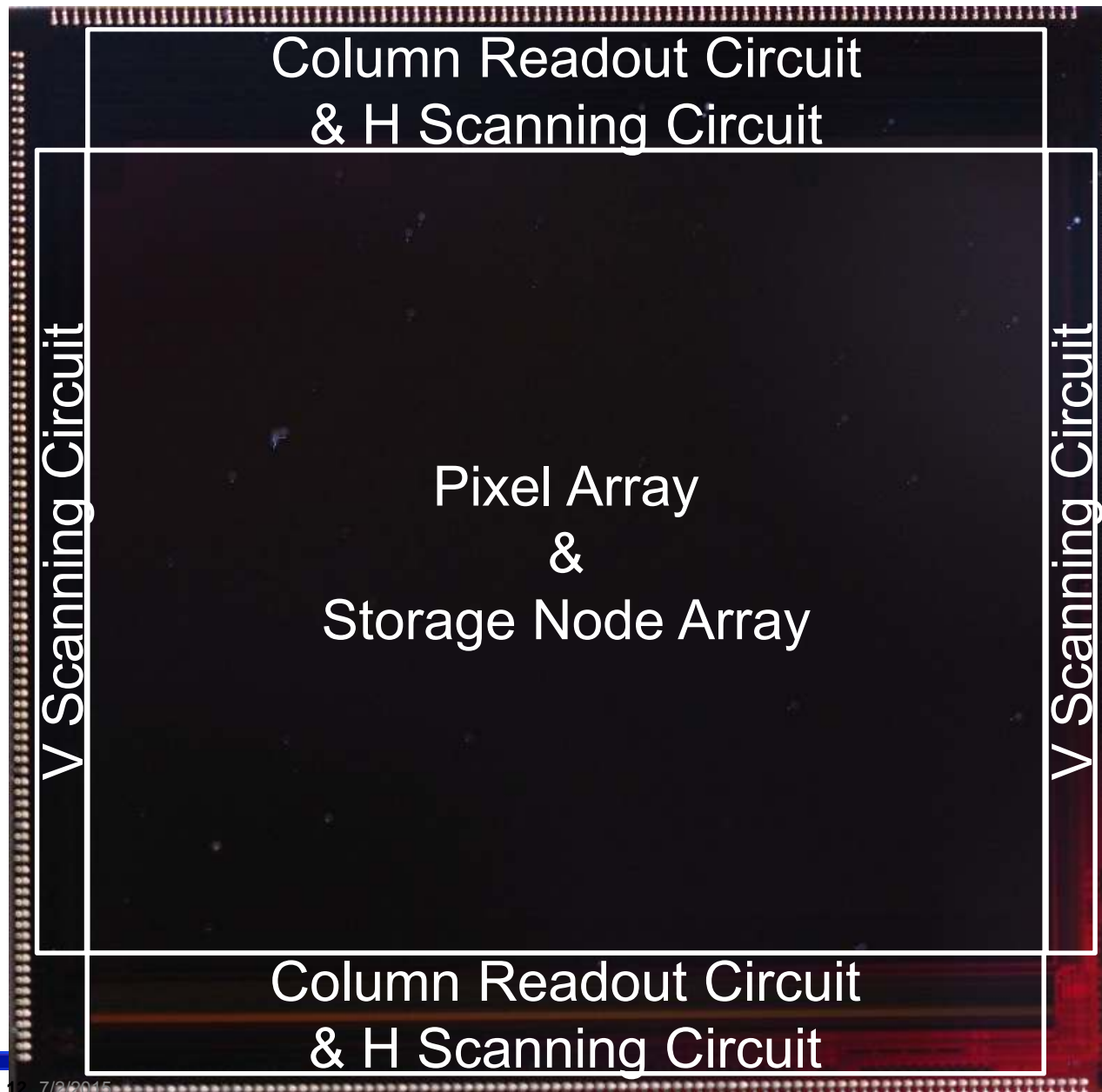
New Target

- Bigger chip size
- Higher resolution
- Smaller pixel size
- Higher number
- Smaller pitch
- Keep high performance
- Better image quality

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Appearance of Die



Chip Size

20.1 × 19.7 (mm)

Pixel Area

17.5 × 13.2 (mm)

Effective Pixels

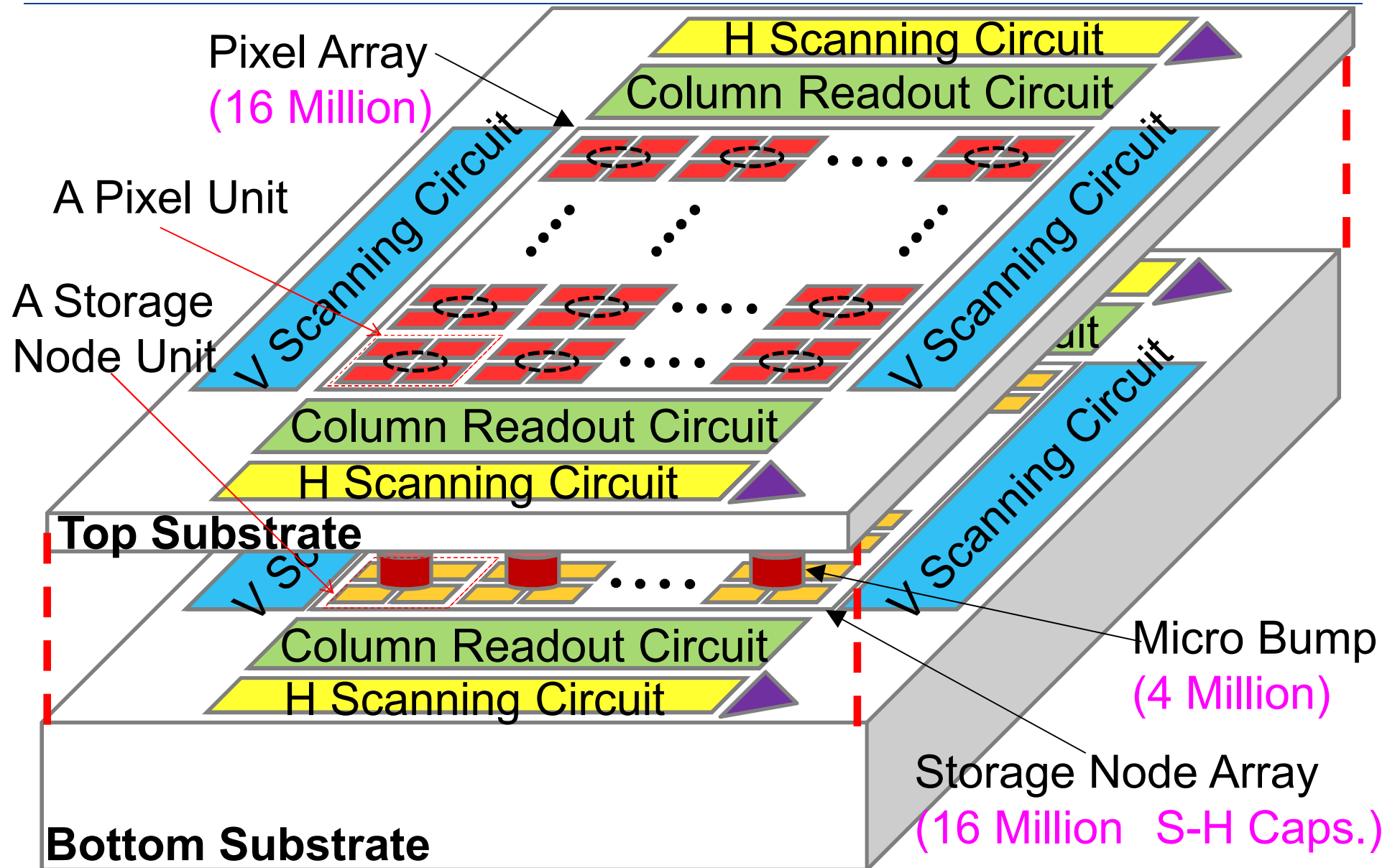
4608 × 3480

Pixel Size

3.8 × 3.8 (μm)

OL20150702-1 **OLYMPUS**

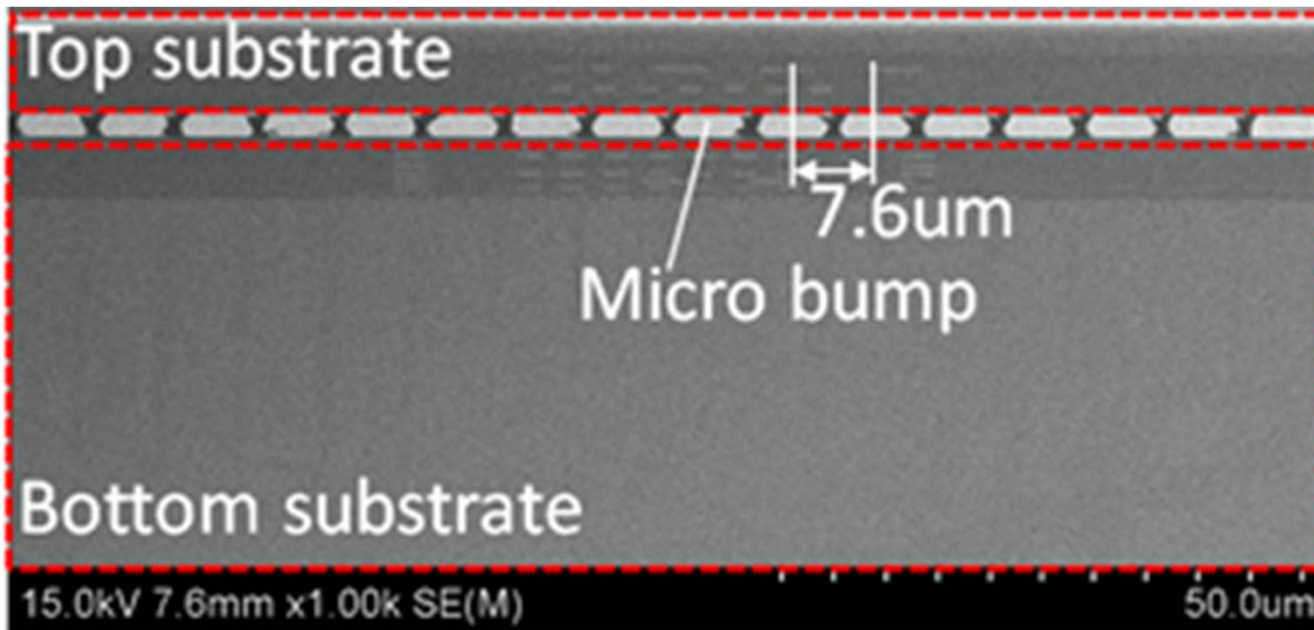
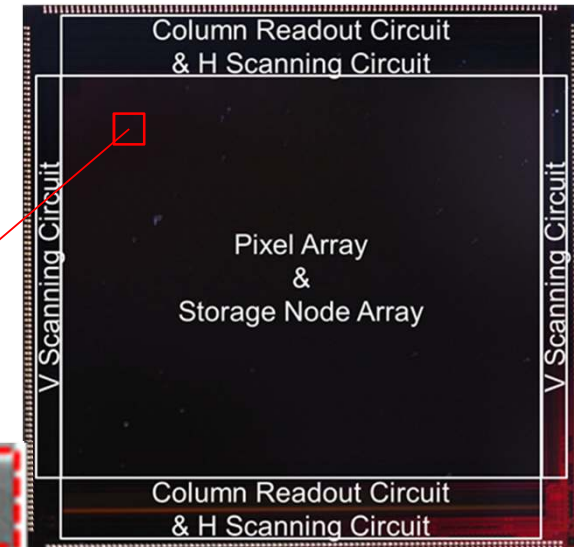
Block Diagram (Whole Chip)



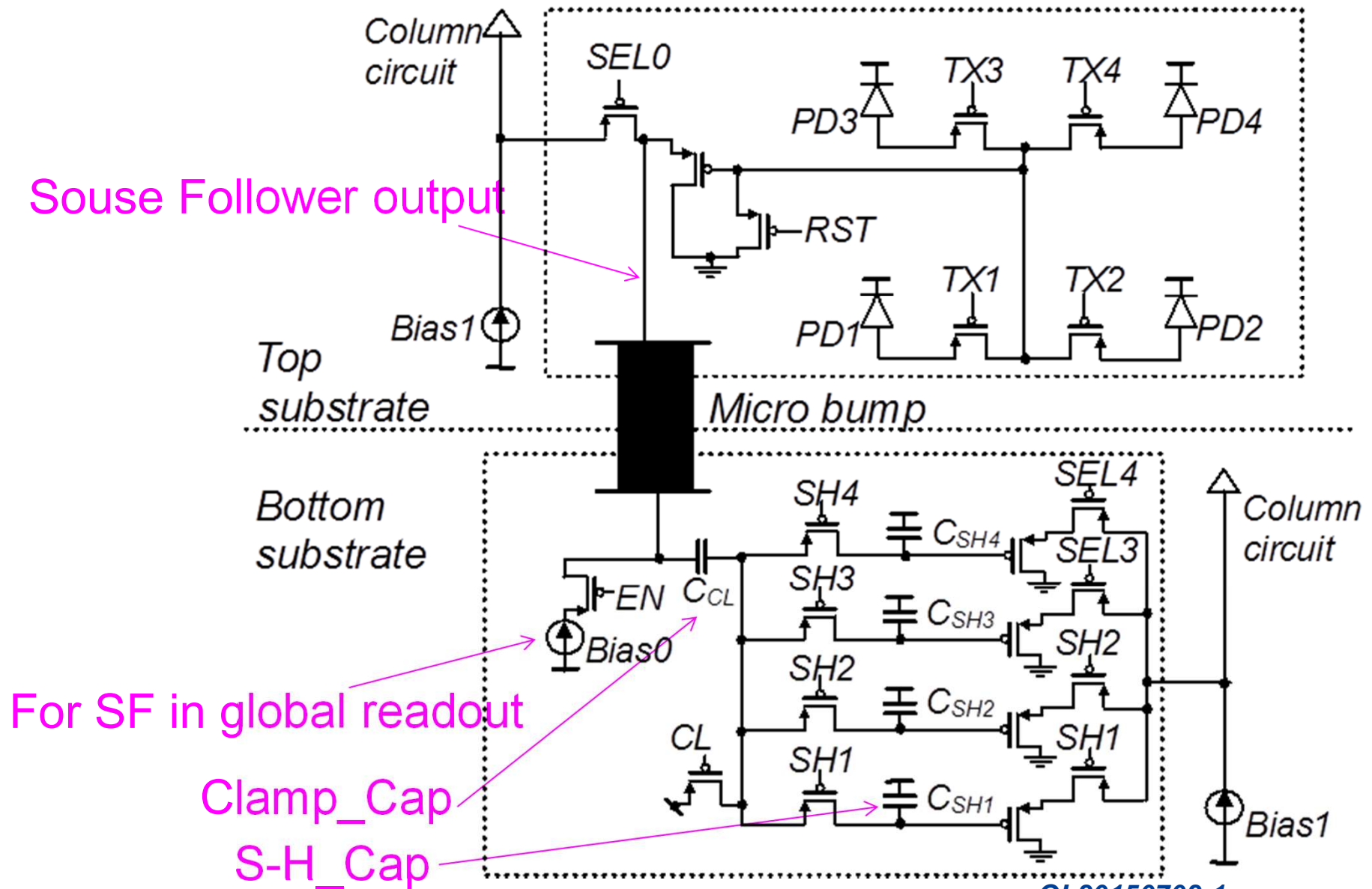
Device Structure

7.6- μm micro bump pitch

Cross Section



Schematic of a pixel unit circuit

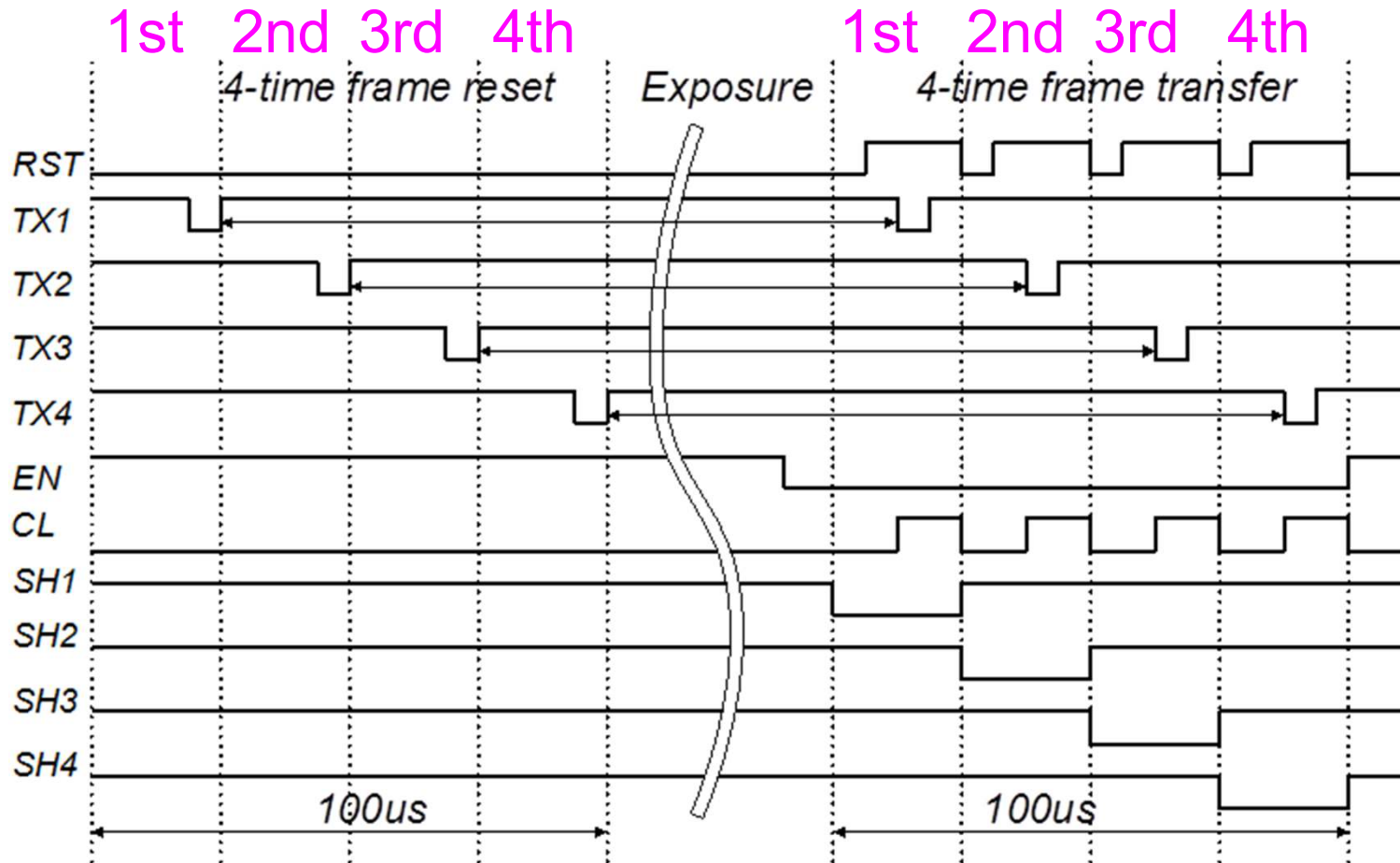


Timing Diagram of Image Sensor

Timing from PD to storage node in GS mode

=> 4-time frame reset & transfer

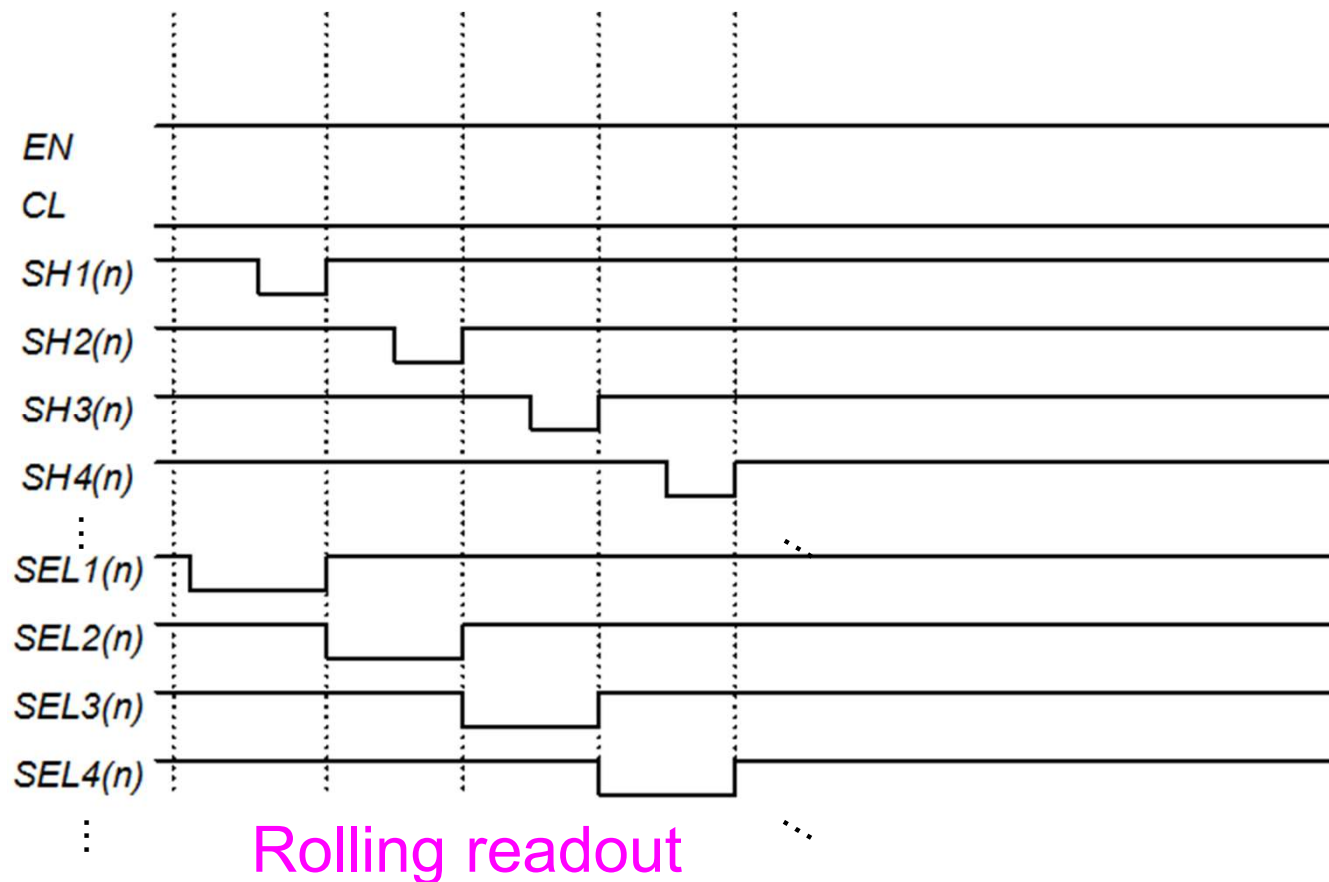
Reset and signal levels are readout for pixel CDS.



Timing Diagram of Image Sensor

Timing from storage node to column circuit in GS mode
=> Rolling readout at 5 fps

Ref. and signal levels are readout for column CDS.



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Captured Image : Color sample

16Mpixel high resolution image with On-chip color filter



Captured Image : B/W sample

Scene: A target (a fan) moving very fast
Tint: 125us



Captured in RS 60-fps mode
with a commercially available
camera



Captured in GS mode
with our image sensor

Specifications

| | This work | Previous work |
|--|--------------------------------|--------------------------------|
| Fabrication process of top substrate | 0.18- μm 1P6M | 0.18- μm 1P6M |
| Fabrication process of bottom substrate | 0.13- μm 1P6M | 0.18- μm 1P6M |
| Chip size | 20.1 \times 19.66 mm | 6.5 \times 6.5 mm |
| Pixel area size | 17.51 \times 13.22 mm | 3.03 \times 2.20 mm |
| Effective pixels | 4608 (H) \times 3480 (V) | 704 (H) \times 512 (V) |
| Pixel size | 3.8 \times 3.8 μm | 4.3 \times 4.3 μm |
| Read out rate | 5 fps | 30 fps |
| Supply voltage | 3.3 V | 3.3 V |
| Number of interconnections in pixel array area | 4,008,960 | 90,112 |
| Minimum pitch of interconnection | 7.6 μm | 8.6 μm |

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Bigger

Higher

Finer

Higher

Finer

Measurement Results

| | This work (Pixel Size: $3.8 \times 3.8 \mu\text{m}$) | Previous work (Pixel Size: $4.3 \times 4.3 \mu\text{m}$) |
|---|---|---|
| Conversion gain | 35 $\mu\text{V}/\text{h}^+$ | 26 $\mu\text{V}/\text{h}^+$ |
| Full well capacity | 35,000 h^+ | 30,000 h^+ |
| Sensitivity with 3200-K light source (B/W sample) | 35,000 h^+/lxs | 60,000 h^+/lxs |
| Dark current at 60° | 50 h^+/s | 1000 h^+/s |
| Parasitic light sensitivity (PLS) | -180 dB | -160 dB |

Photodiode process and pixel layout were optimized

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Conclusion

◆ Key technology

- ▶ **Wafer on wafer bonding**
- ▶ **Interconnection at 7.6- μm pitch**
- ▶ **4 million interconnections in pixel area**

◆ Achievements

- ▶ **16Mpixel global-shutter function with -180-dB PLS**
- ▶ **High image quality**

Future Work

◆ Technology

- **Finer pitch interconnection**
- **Improvement sensor specs for global shutter (frame rate, random noise)**

◆ Applications

- **Advanced image sensor using pixel level interconnection (minimum chip size, in-pixel ADC, WDR)**
- **3D stacked image sensor with other chips (DSP, memory)**

OLYMPUS
