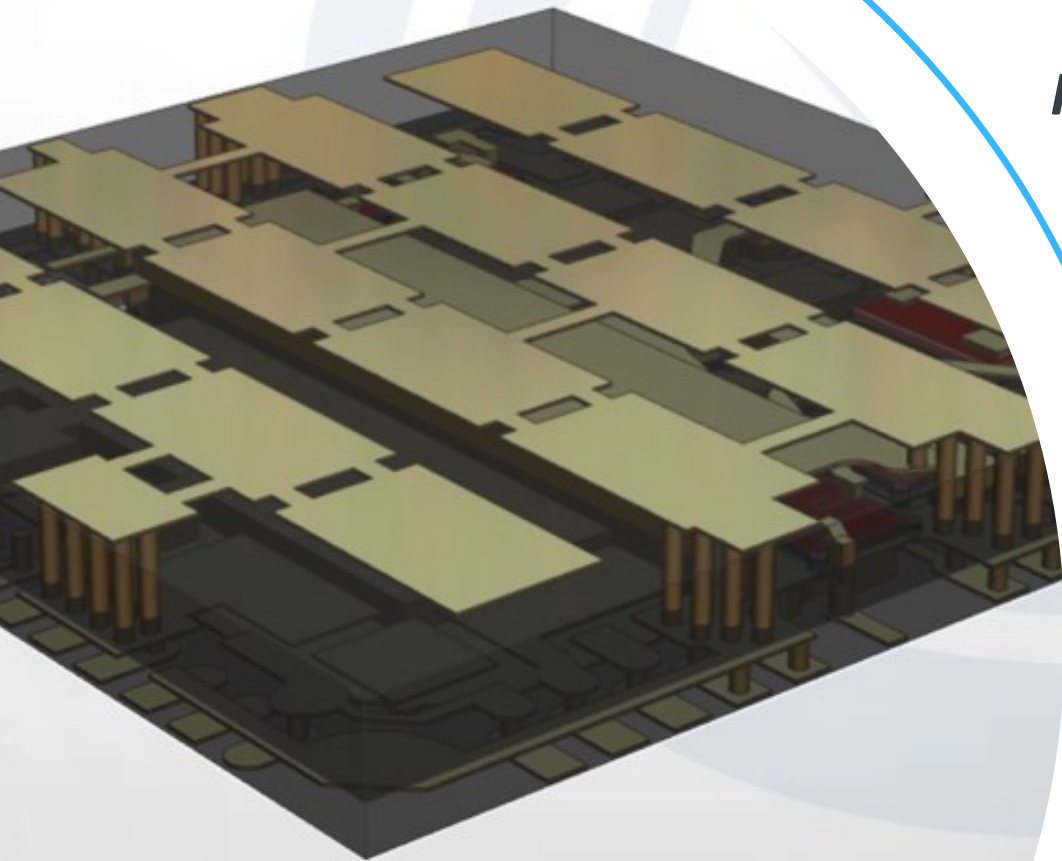


Breakthrough in the packaging industry to unleash innovation

Heterogeneous integration & 3D packaging technology

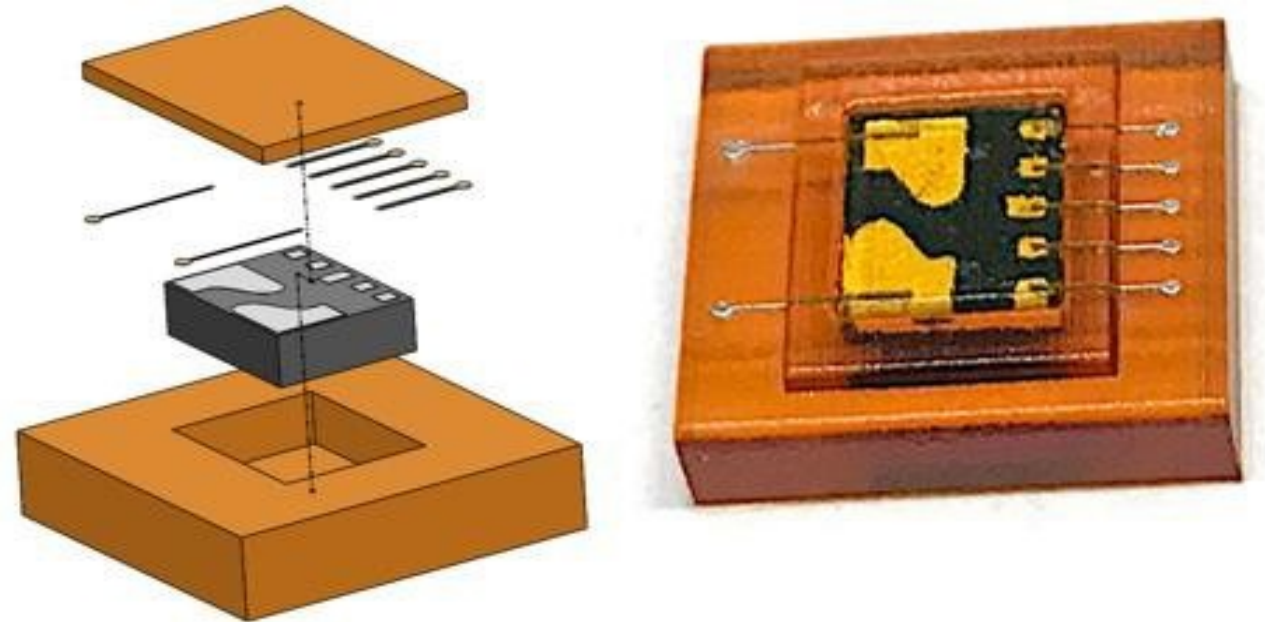
MIRKO SIDOTI

June 2023



Agenda

- Nano Dimension introduction
- Why AME? Motivation
- AME Packaging History & Process Evolution
- AME Technology Basics and opportunities
- System in Package (SiP) Development Flow
- RF SiP Case Study
- Power Transistor AME Packaging Case Study
- Summary



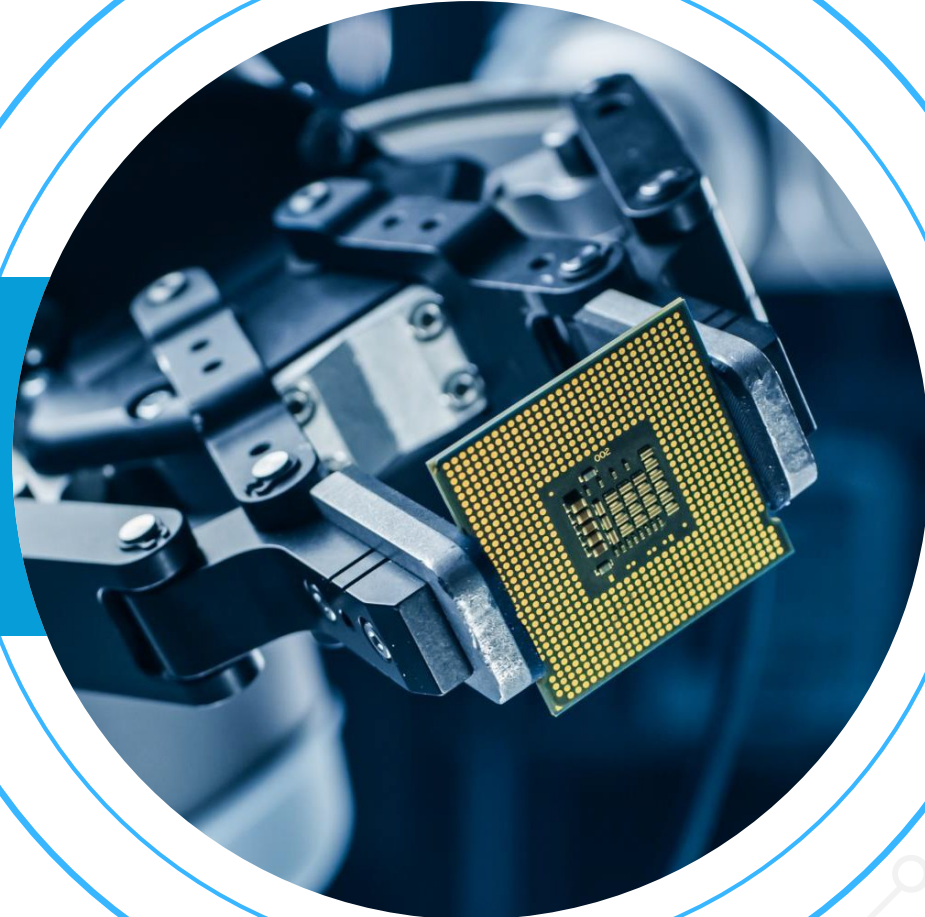
Acronyms:

AM = Additive Manufacturing

AME = Additively Manufactured Electronics

SiP = System in Package

Who is Nano Dimension?

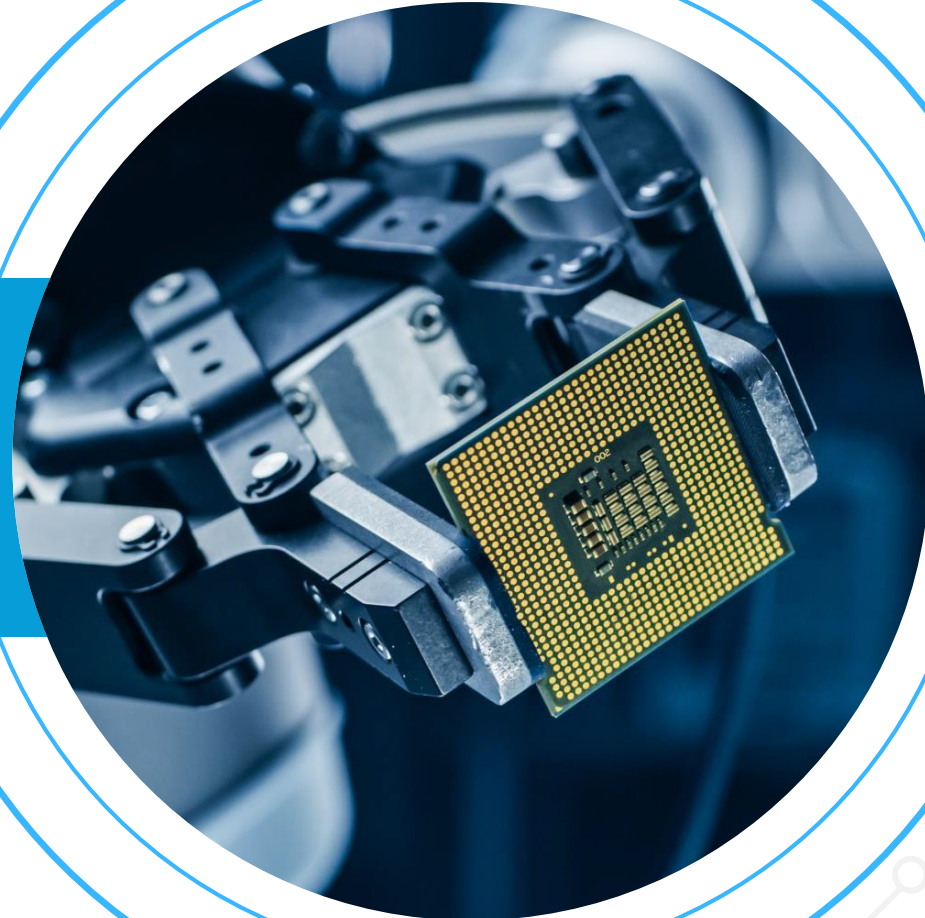


We make...

...all of these
**advanced deep learning-AI led
manufacturing solutions**
that are used by
industrial-level organizations
to 3D print and assemble
**High Performance Electrical
& Mechanical Applications**



Why AME?

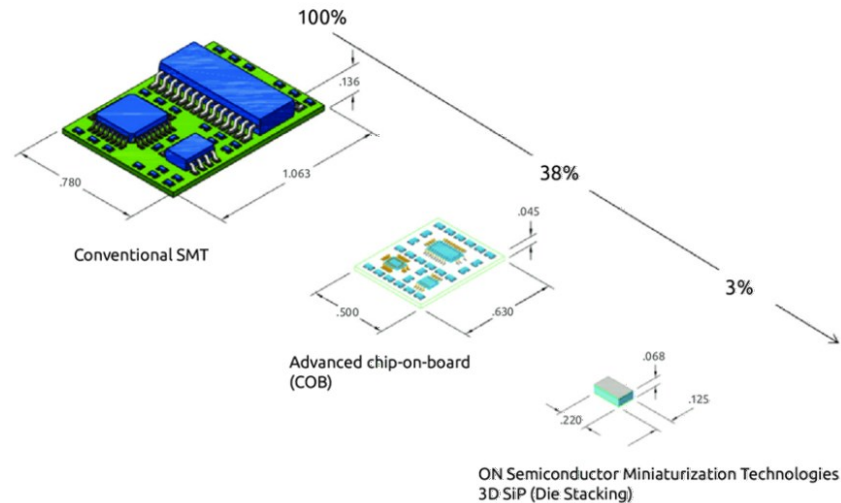


Motivation

CURRENT WORLD OF ELECTRONICS

1. Technical Limitations:

preventing improvement of performance and reduction of other factors such as weight and size



Weight and size over 90% down

2. Supply chains:

hurting most in the high variety small mix and when prototyping (long R&D cycles)

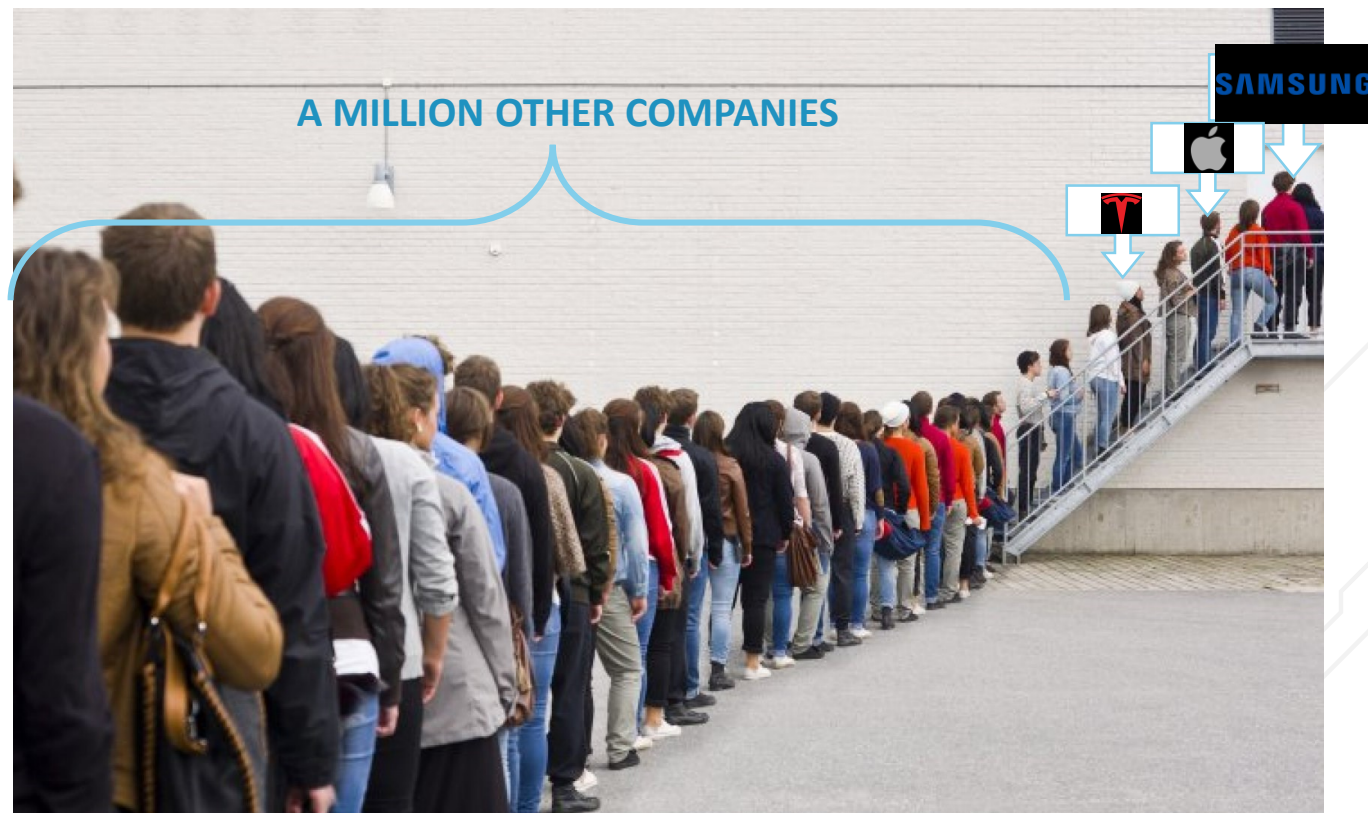


Motivation (cont.)

LONG LINES FOR PACKAGING AND PROTOTYPING

Very long lead time for small & medium-sized enterprises and very long R&D-cycles

- To produce a prototype, 4 R&D cycles are required
- each cycle has a 3-4 months lead time until supplied from the global packages & electronics manufacturer



Motivation (cont.)

TRADITIONAL MANUFACTURING VS. SUSTAINABLE AM SOLUTIONS

3. Sustainability

A holistic approach towards functional electronics with net zero carbon emissions



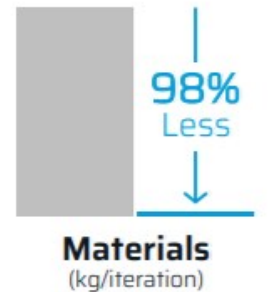
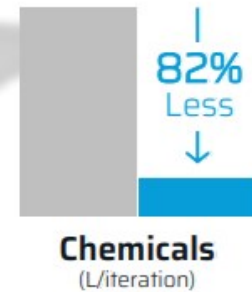
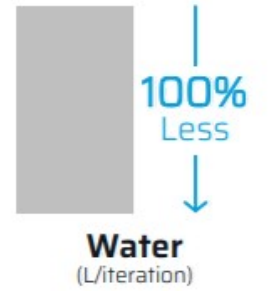
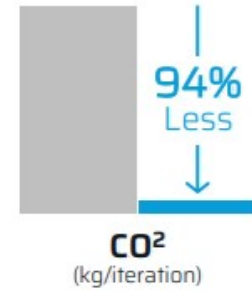
Motivation (cont.)

TRADITIONAL MANUFACTURING VS. SUSTAINABLE AM SOLUTIONS

Before



After



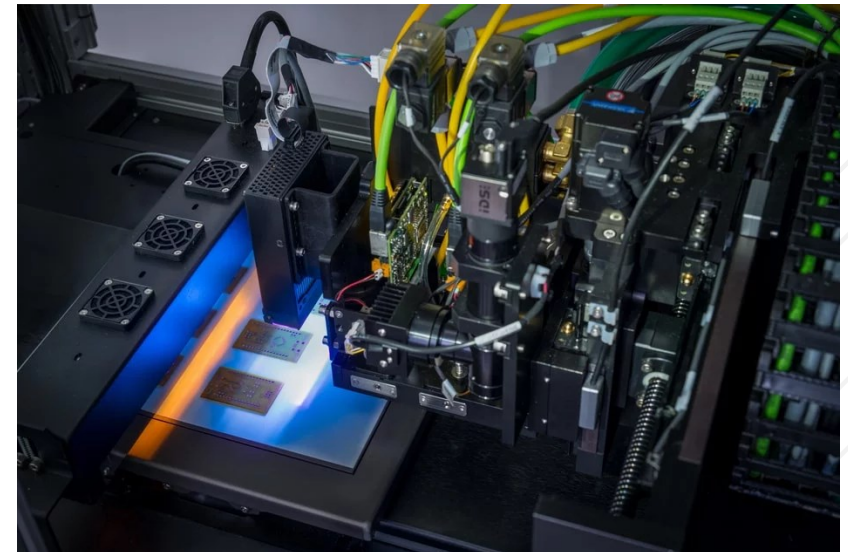
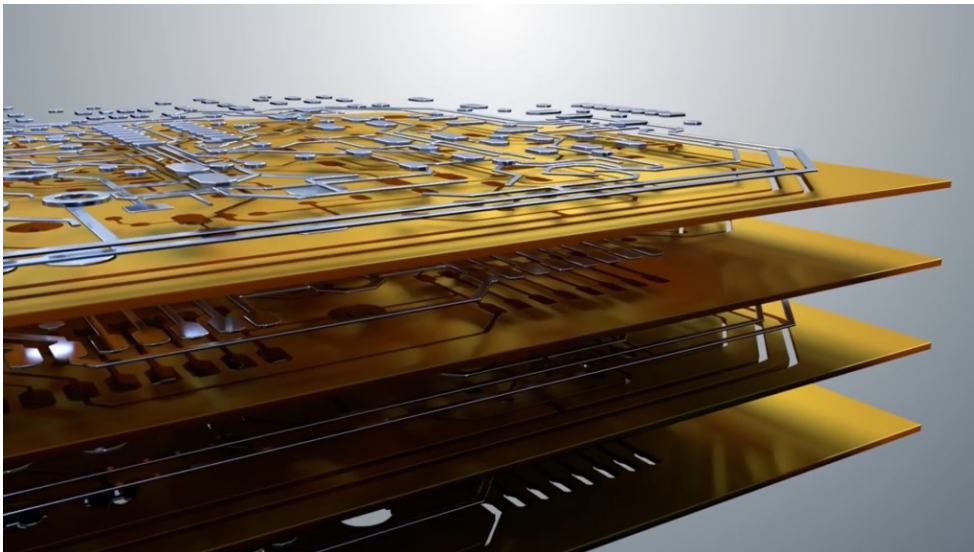
¹ Based on a 2021 study by HSSMI, a UK based sustainability consultant

But how it works?

ADDITIVE MANUFACTURING ELECTRONICS (AME) - PROCESS DESCRIPTION

- Inkjet technology that combines UV-cured dielectric material (acrylic monomers) with silver nanoparticles (Ag NP) that undergo sintering upon IR radiation.

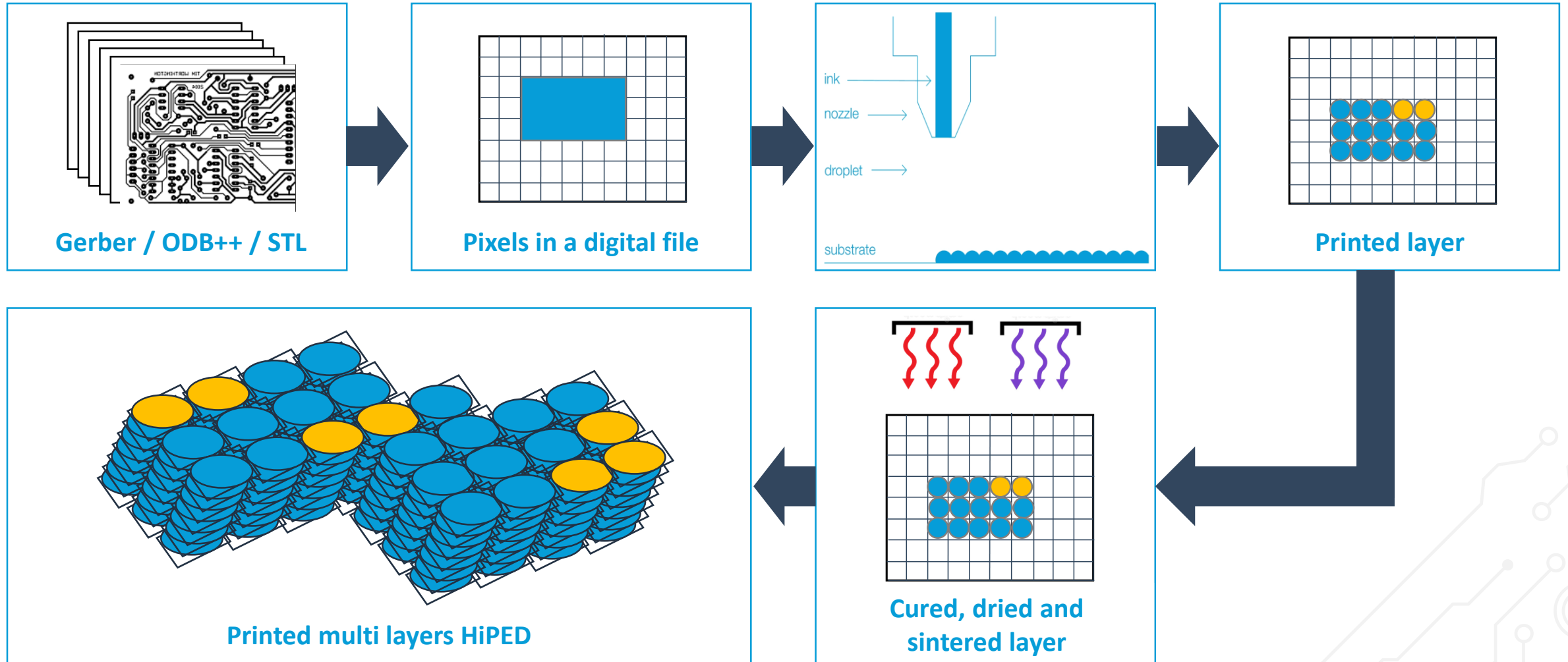
Result in solid objects with highly conductive patterns in shapes unachievable through traditional processes



Additive Manufacturing Electronics (AME) - DragonFly



From a Digital design file to a Printed Hi-PED

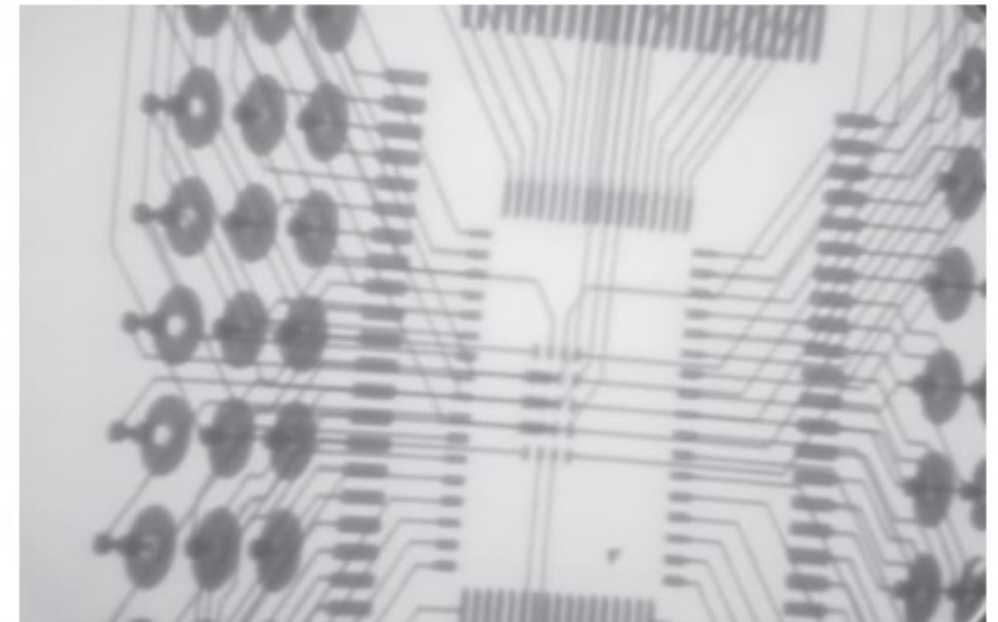
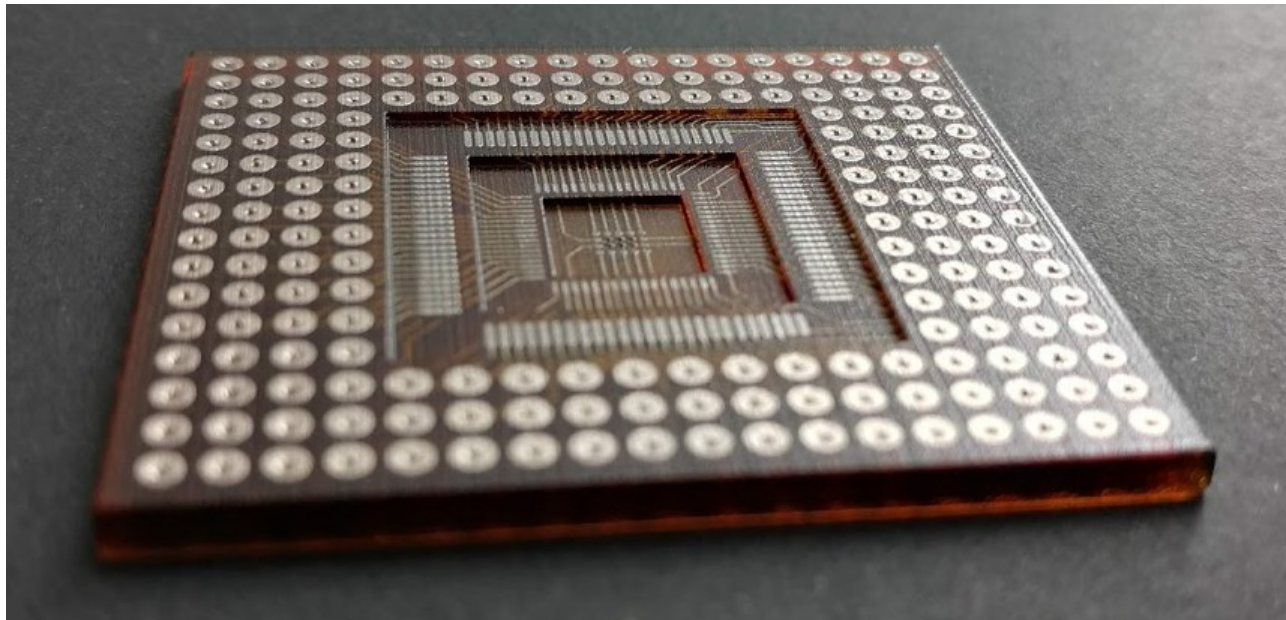
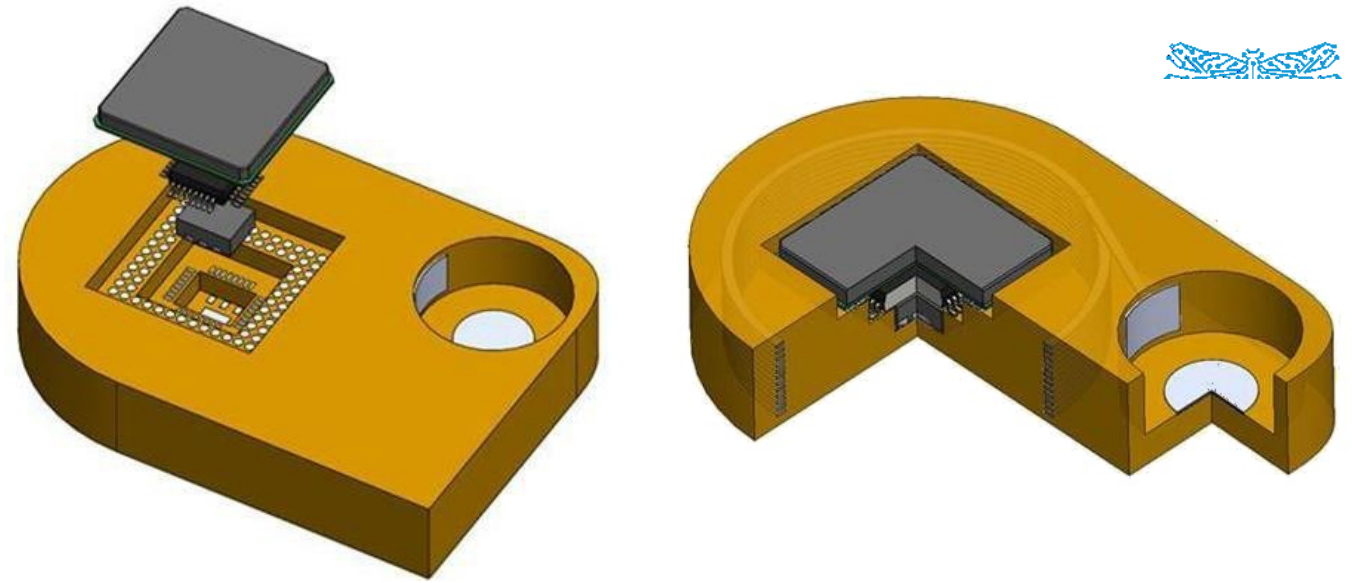




History

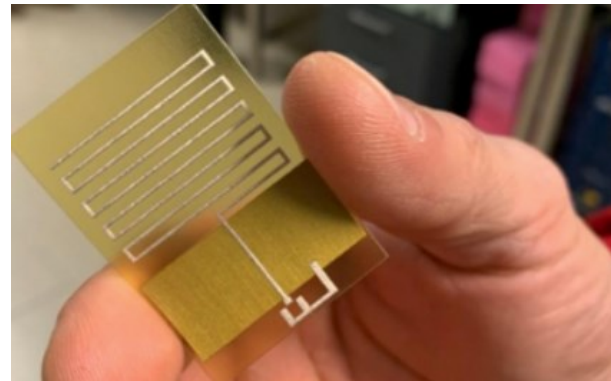
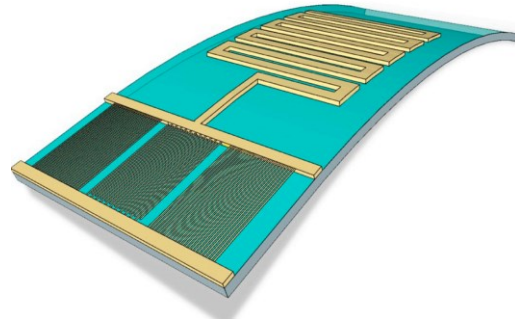
AME SOCKETS & INTERPOSERS

- Very first encapsulation concept: Stacking of packaged ICs and interposers



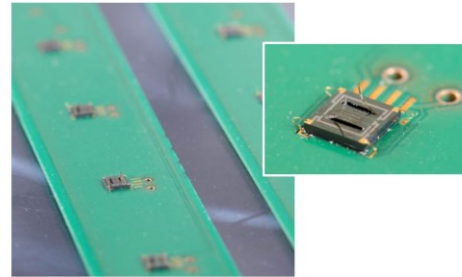
History (cont.)

AME SENSOR APPLICATIONS

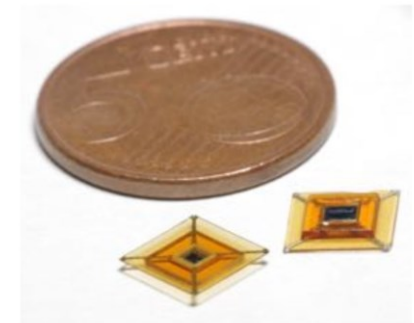


Compact and flexible meander antenna for Surface Acoustic Wave sensors

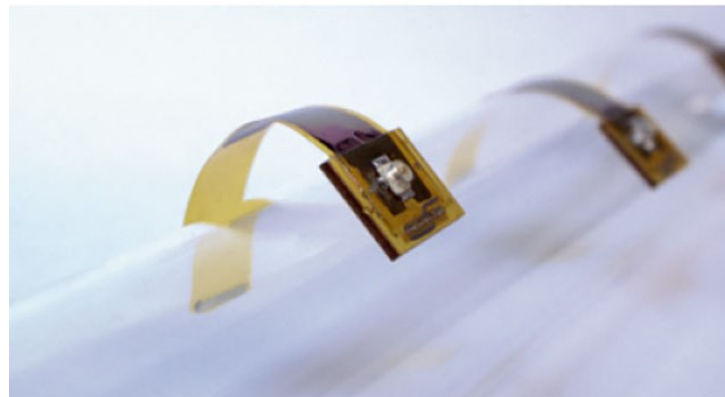
Artificial Hair Cells for Flow Sensing



EMBEDDING FLOW SENSORS IN SEALED PACKAGE



Sensor direct print packaging (3D printed wirebonding)



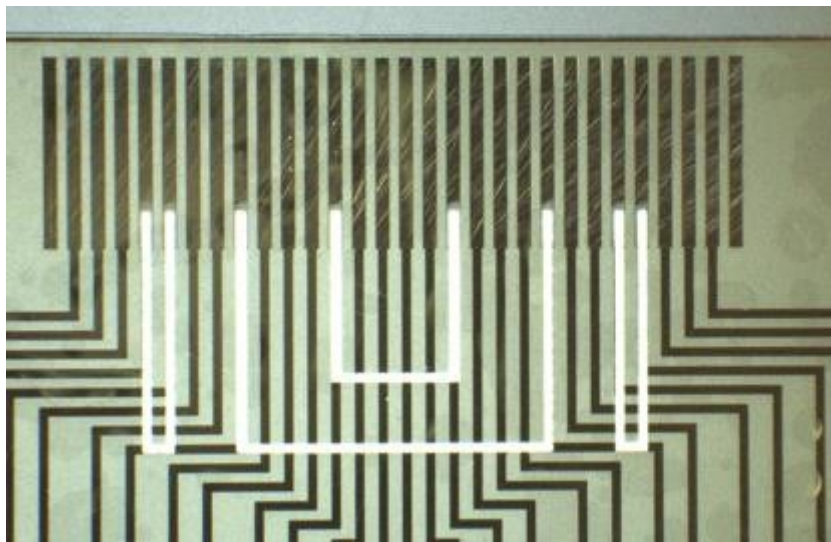
3D embedded sensor in electrical packaging



Optoelectronic Neural Surface

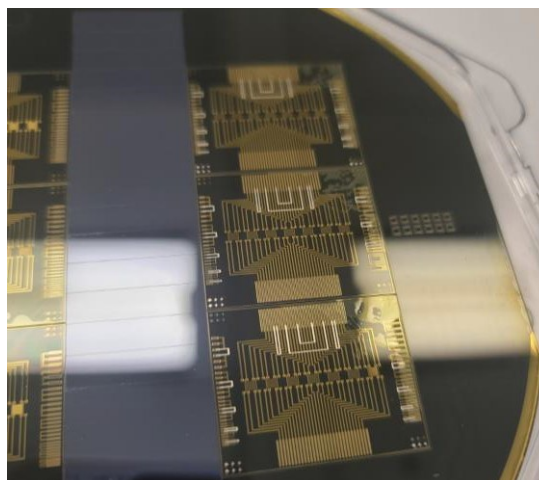
History (cont.)

TESTPATCH AGCITE® BONDING



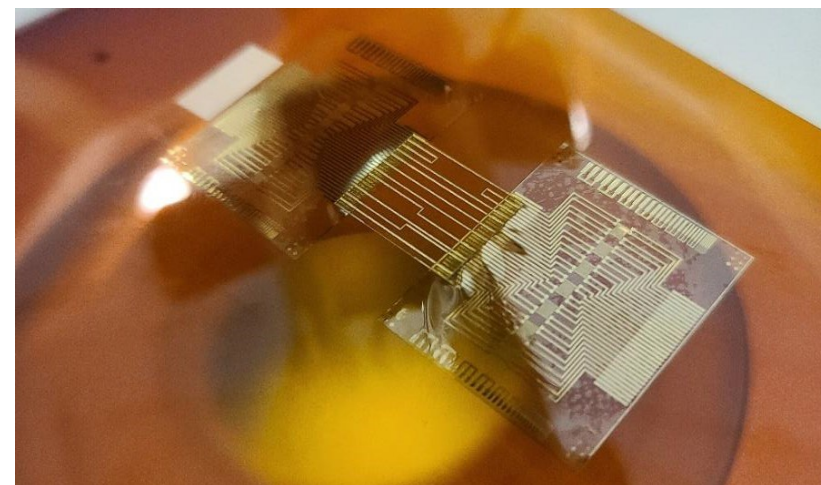
Print on foil

success



Print on wafer

success



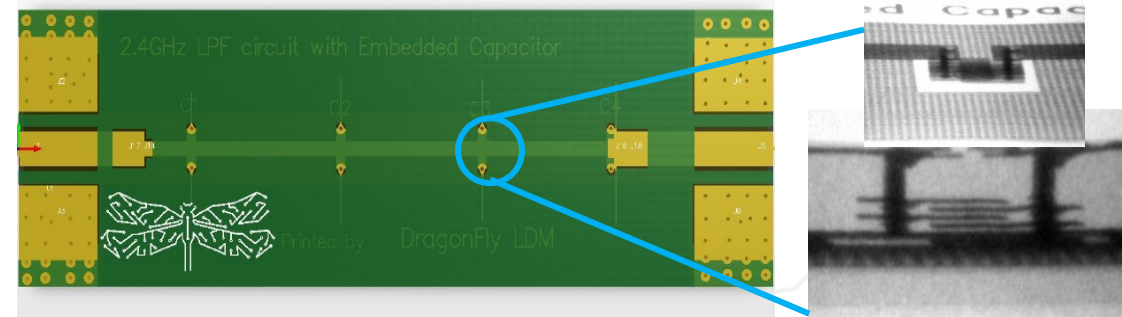
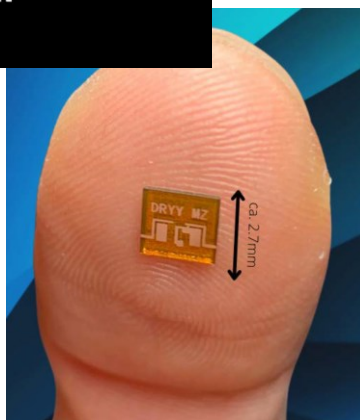
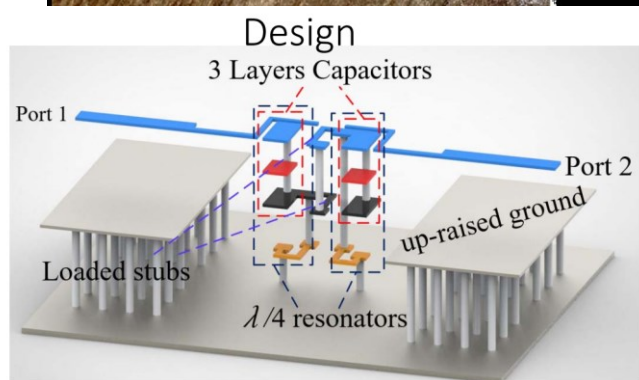
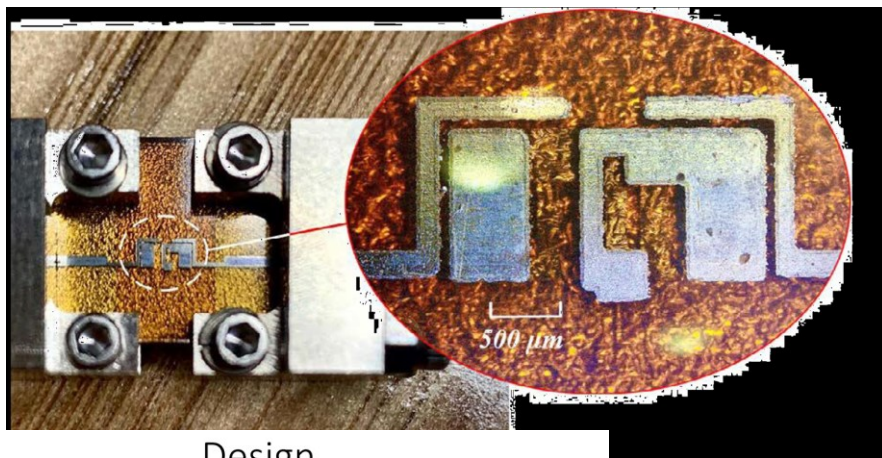
Connect two foil on flex substrate

success

RF Examples

HIGH FREQUENCY FILTERS

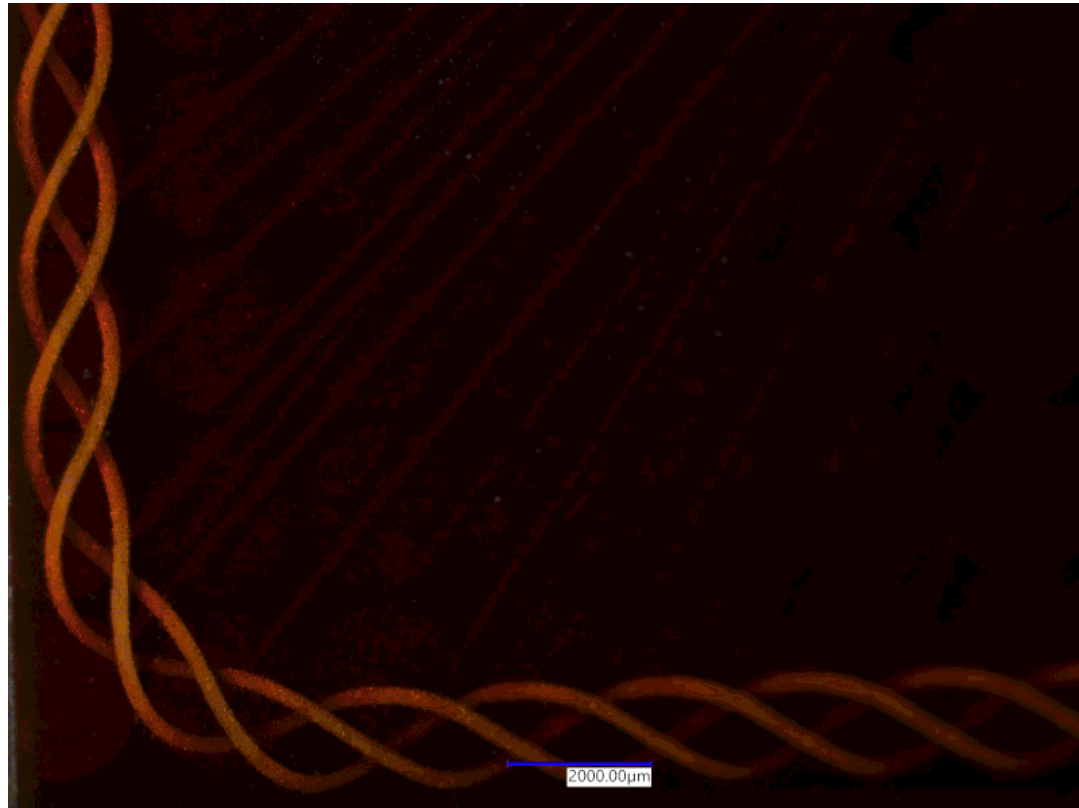
- Complex tuning iterations and extra laser trimming process is replaced by an overnight print



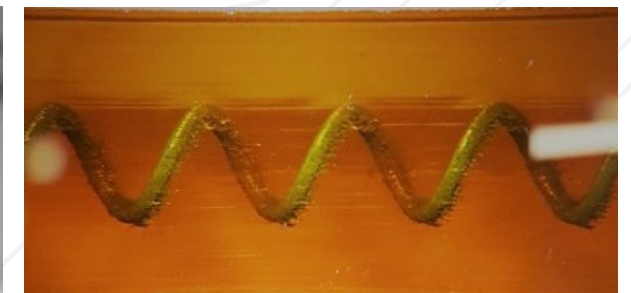
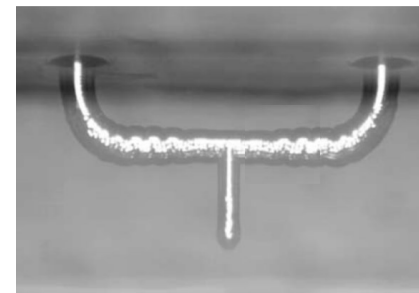
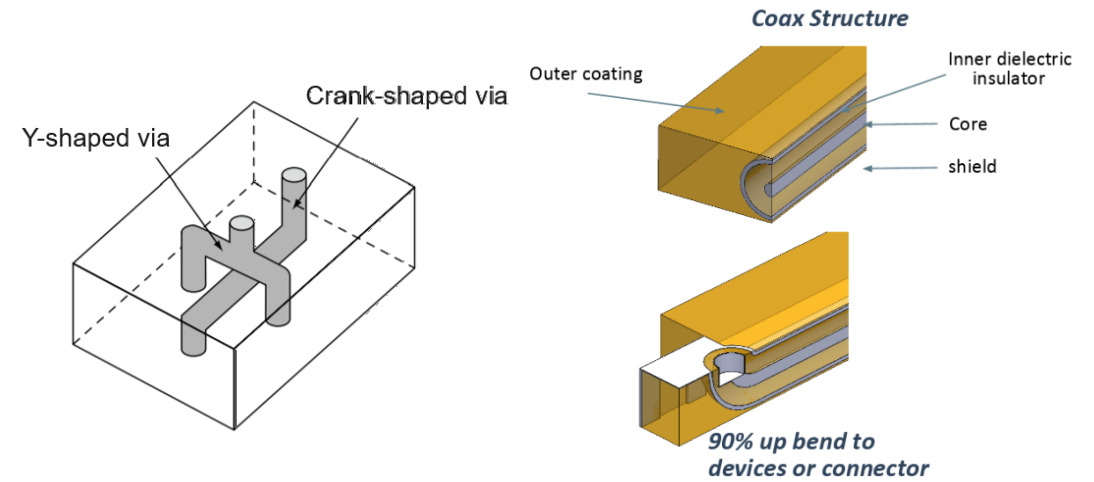
New Design Thinking

NON PLANAR TRANSMISSION LINES

- Coaxials, twisted pairs, waveguides. Freedom of via intercon



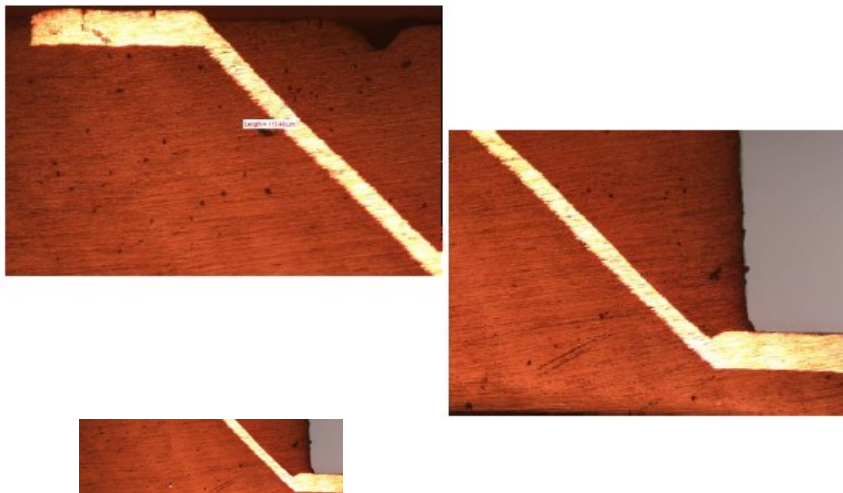
Source: J.A.M.E.S



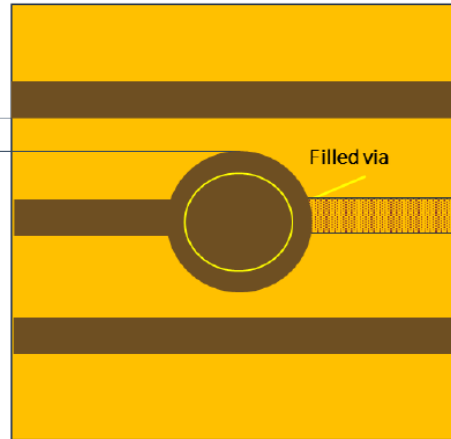
New Design Thinking

HIGHER DENSITY ROUTING

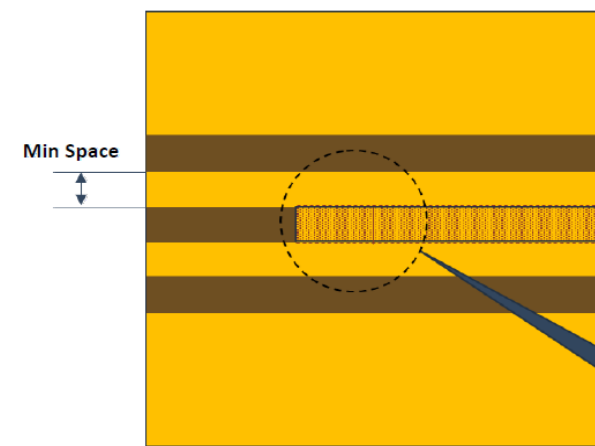
- Homogeneous Z-axis structures allow to 45 degrees vias with increased performance and space reduction



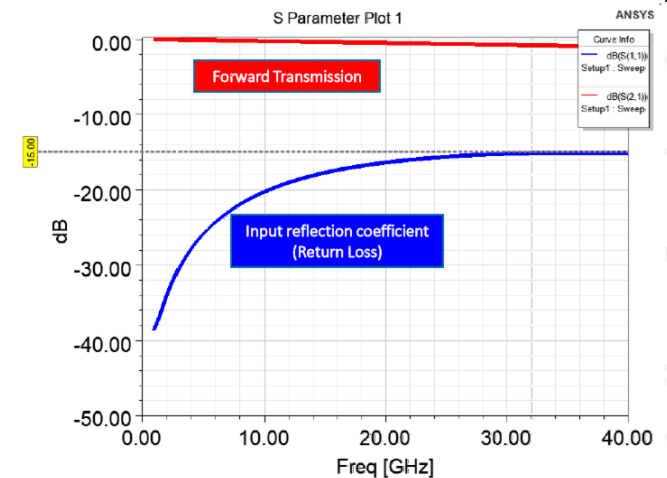
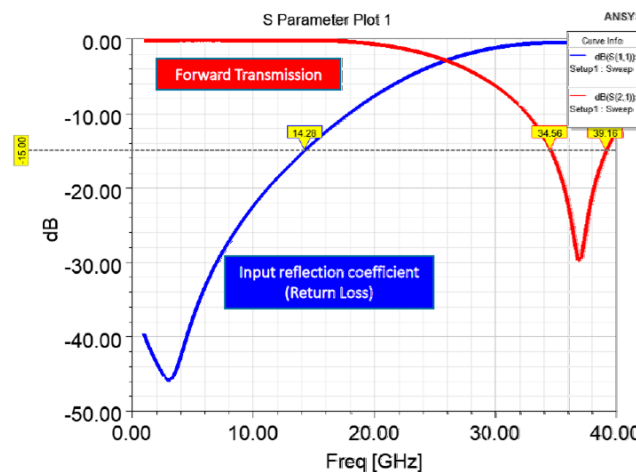
Traditional PCB Process



3D AME Process



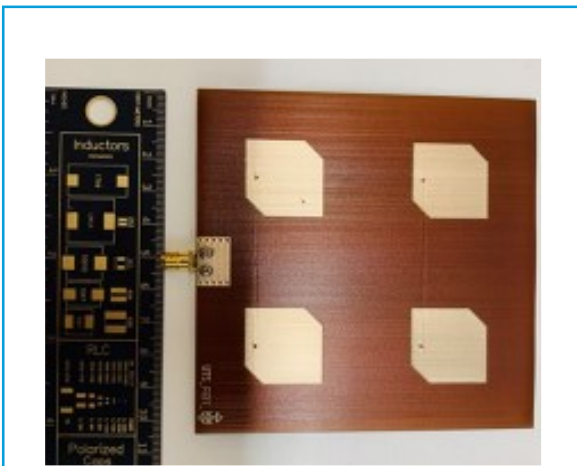
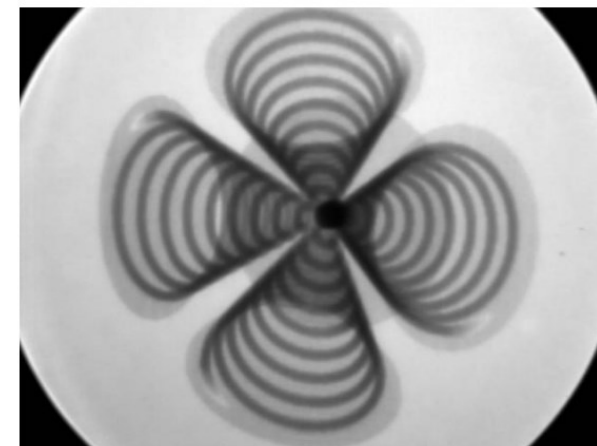
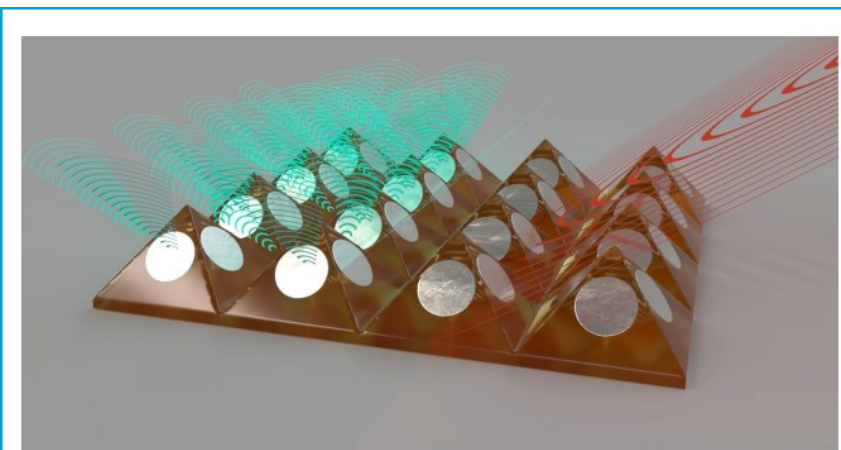
Traditional VIA and pad location



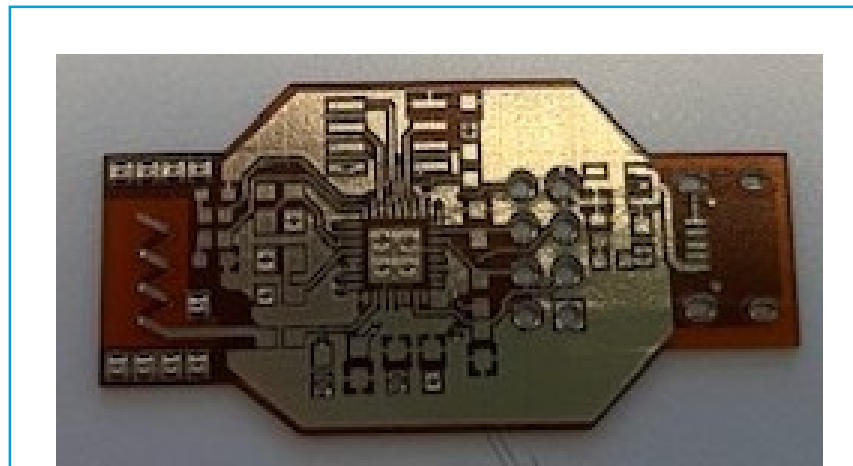
New Design Thinking

3D-PRINTED ANTENNAS AND RESONATORS

- AME technology is an enabler for new designs of antennas
- Design freedom in the 3D space enables unique antennas such as: Omni directional antennas, coils antennas, special shaped phased-array antennas, etc.



Multilayer Array of Stacked Patches

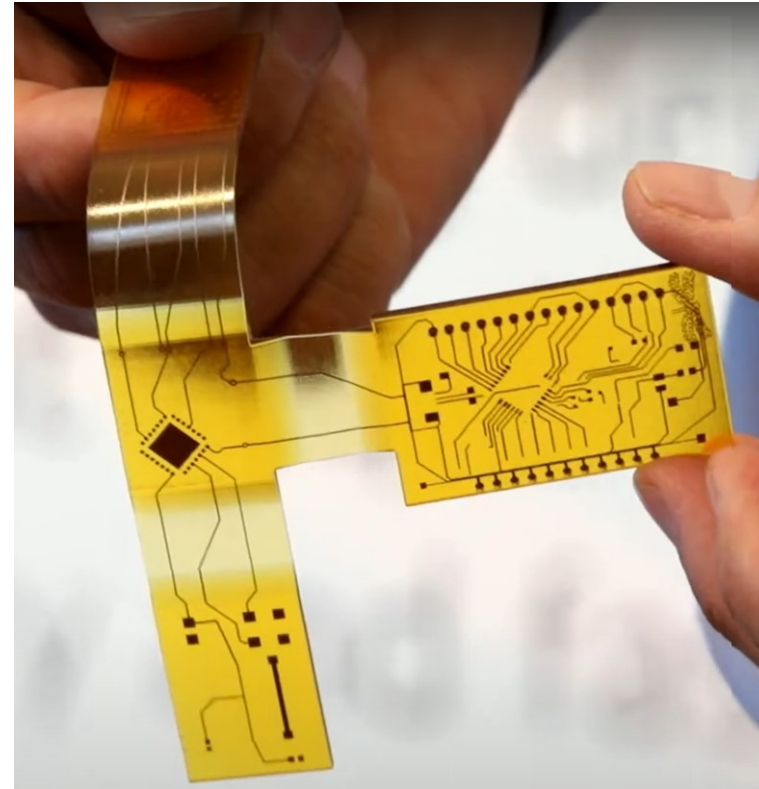


Metamaterial Antenna

New Design Thinking

FLEXIBLE AND FLEX-RIGID STRUCTURES

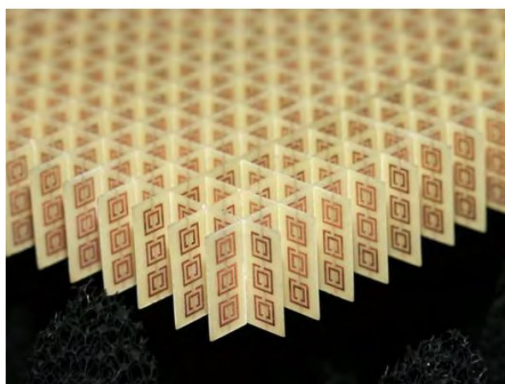
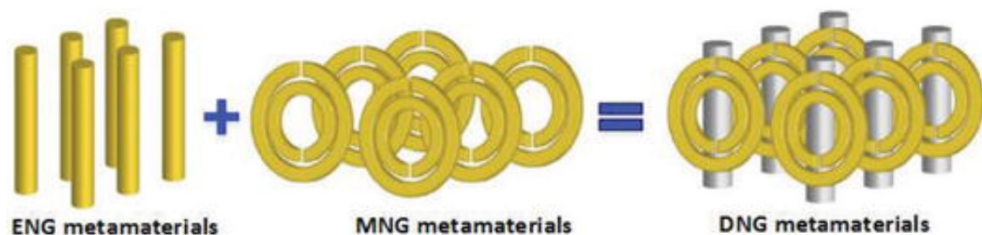
- Flexible structures
- Flex-rigid assemblies
- MID (Molded Interconnect Devices)



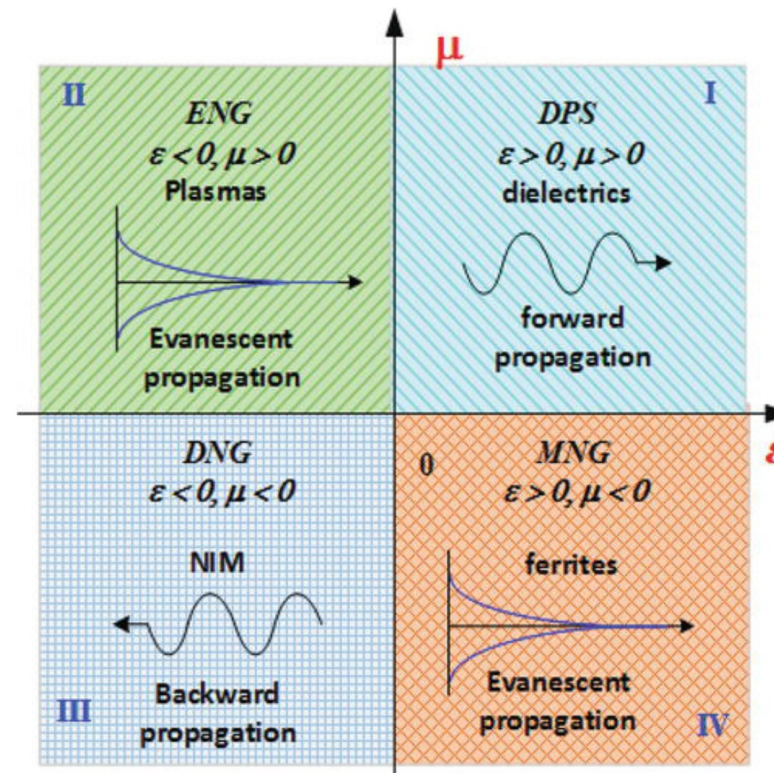
New Design Thinking

3D-PRINTED METAMATERIALS

- Conventional technologies rely on time consuming precise assembly
- AME is an enabling technology for agile design of 3D metamaterials with isotropic or quasi-isotropic behavior



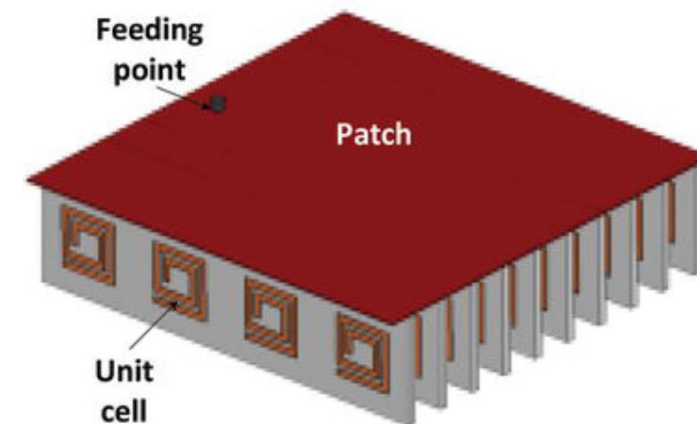
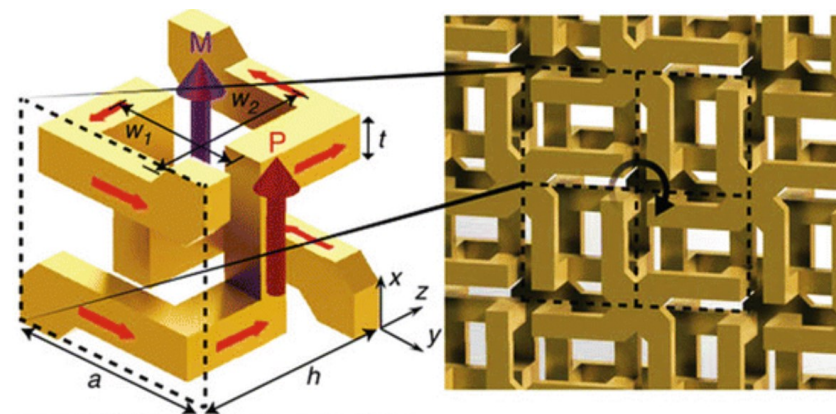
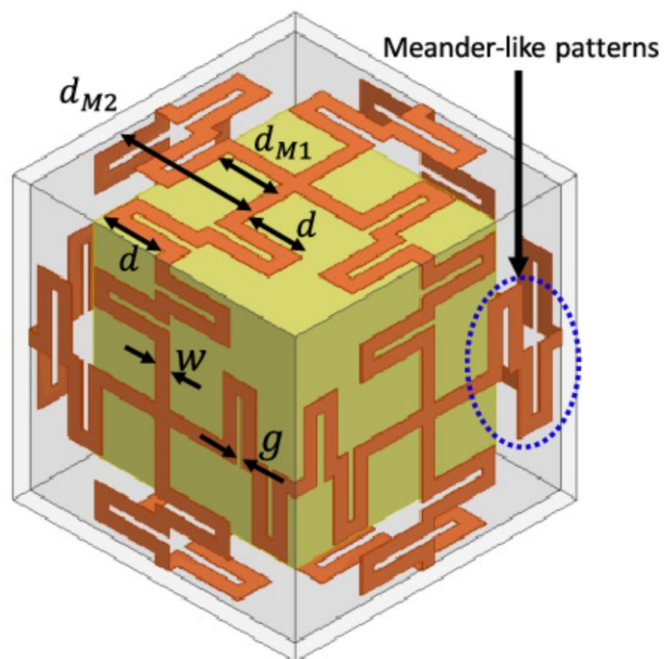
Conventional technologies



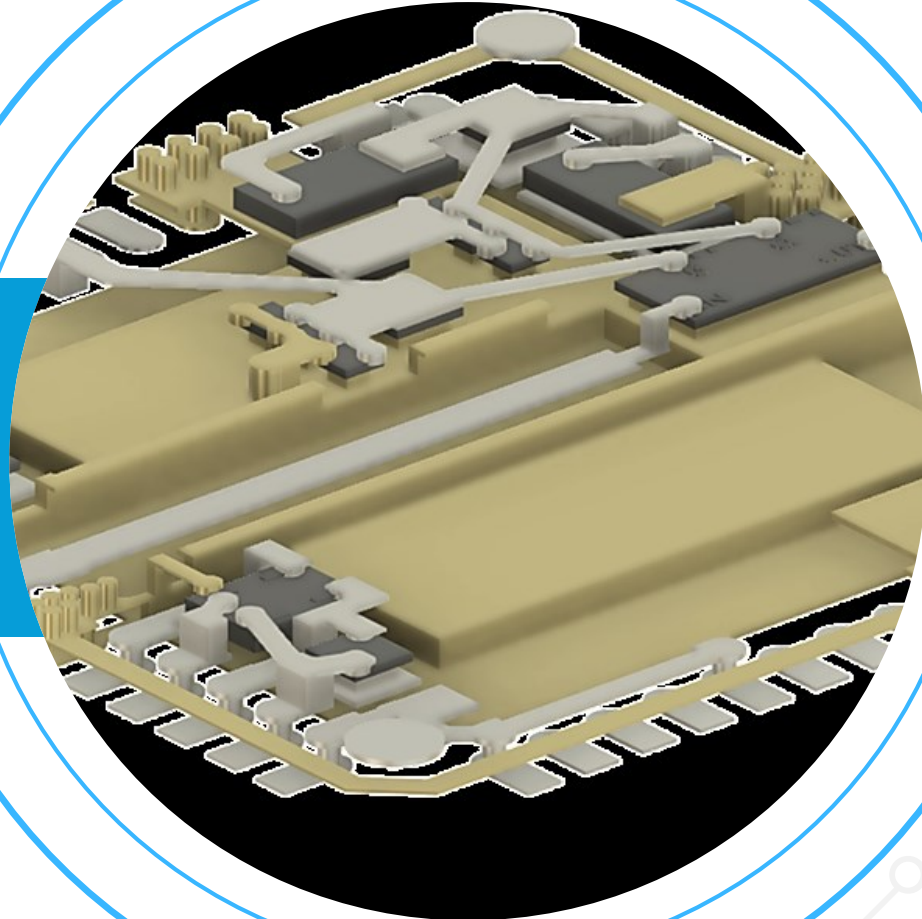
New Design Thinking

3D-PRINTED METAMATERIALS

- 3D Metamaterial cells and structures possible with AME:



SiP development flow

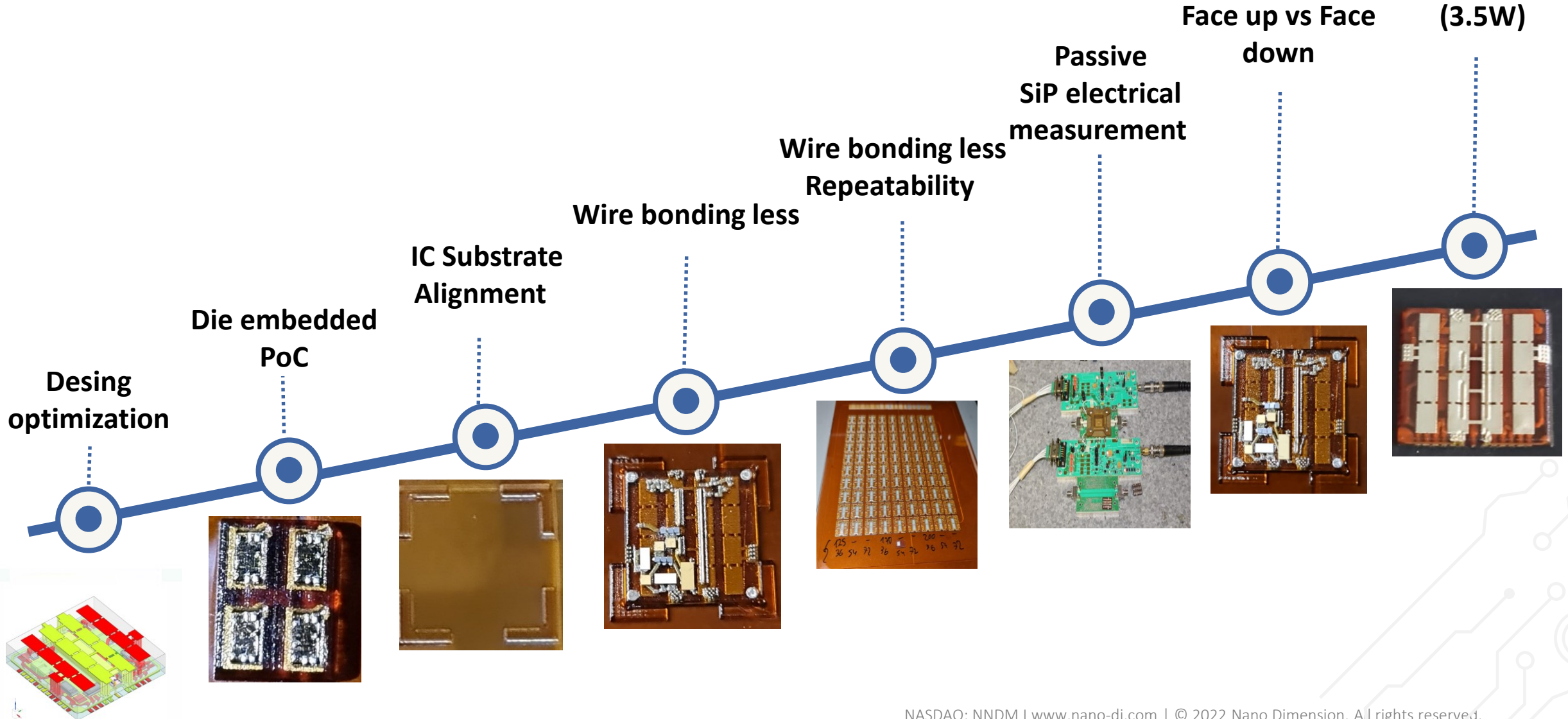


Process Evolution

PROCESS PLANNING, SYSTEM DESIGN AND DIE IMPLEMENTATION

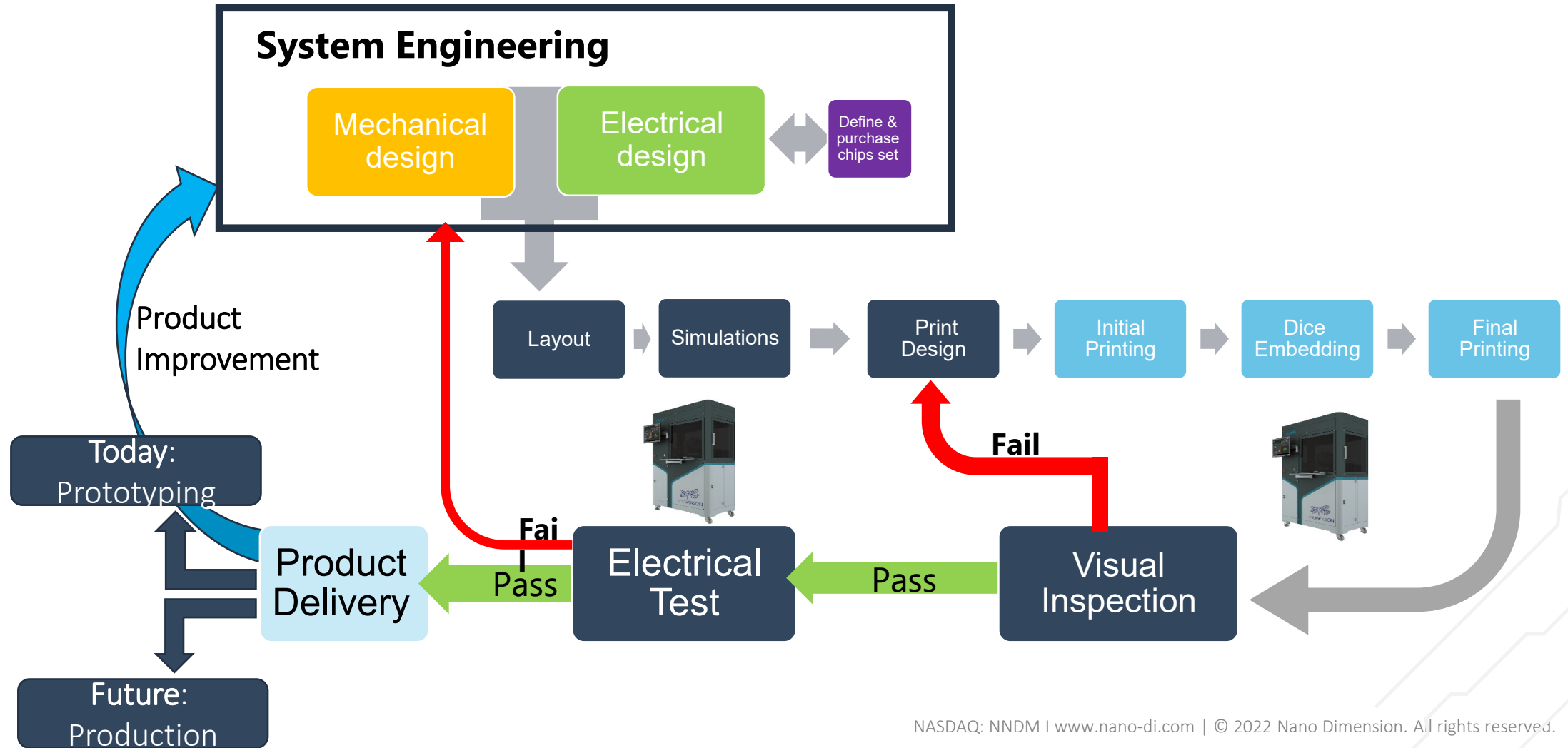


Functional SiP
(3.5W)



System in Package (SiP) development flow

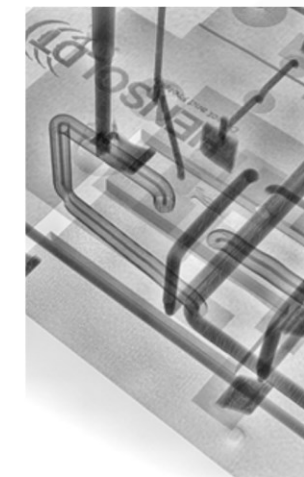
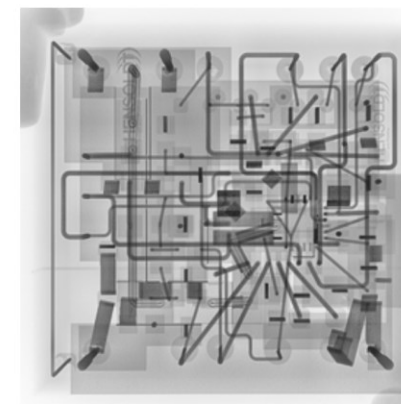
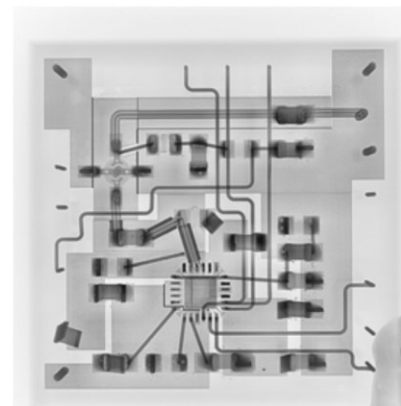
PROCESS PLANNING, SYSTEM DESIGN AND DIE IMPLEMENTATION



New Design Thinking

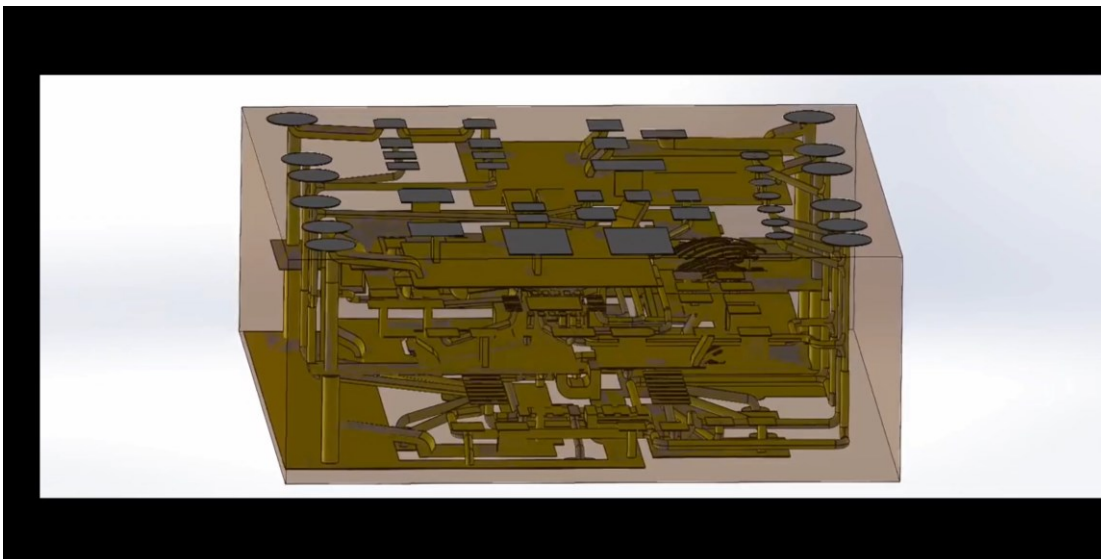
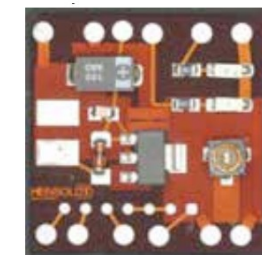
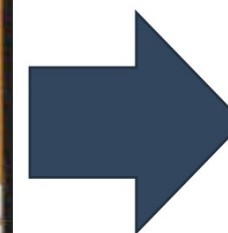
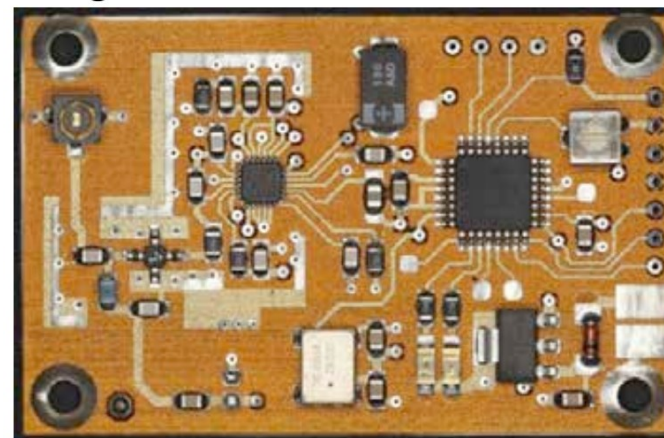
RF SYNTHESIZER

- 3D Heterogeneous Integration
- Includes DC, digital signals and also RF
- Shielded coaxial lines to keep signal integrity/Impedance controlled interface
- Printed passive components (coils, capacitors)
- Miniaturization



High Resolution X-ray Views

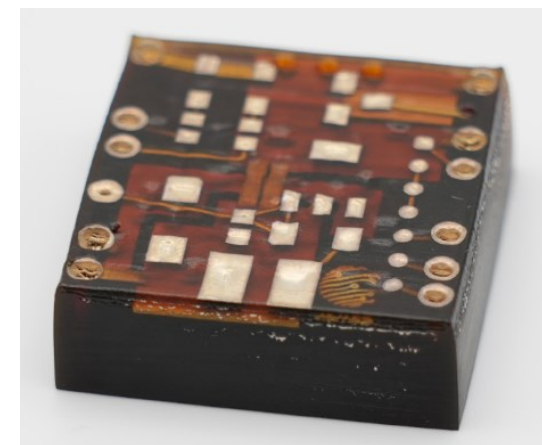
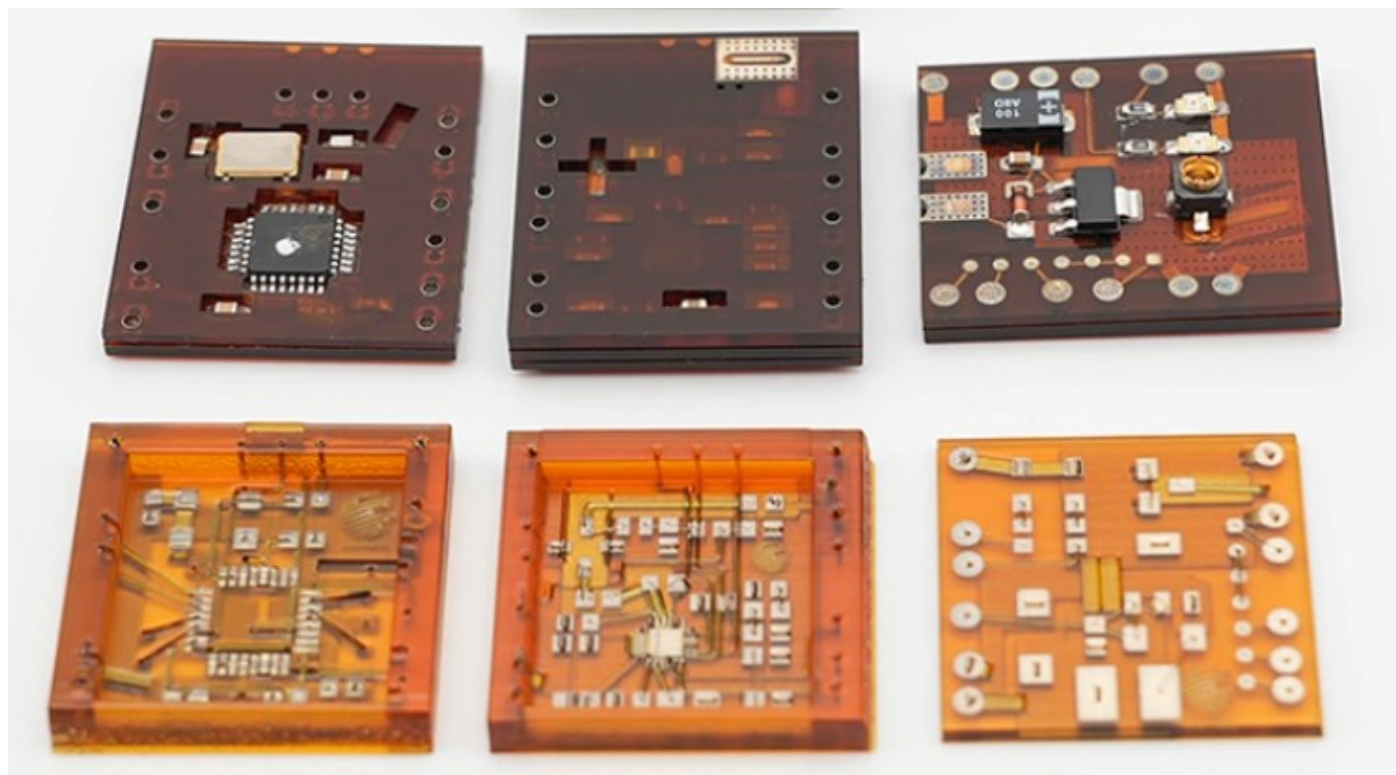
Original PLL board



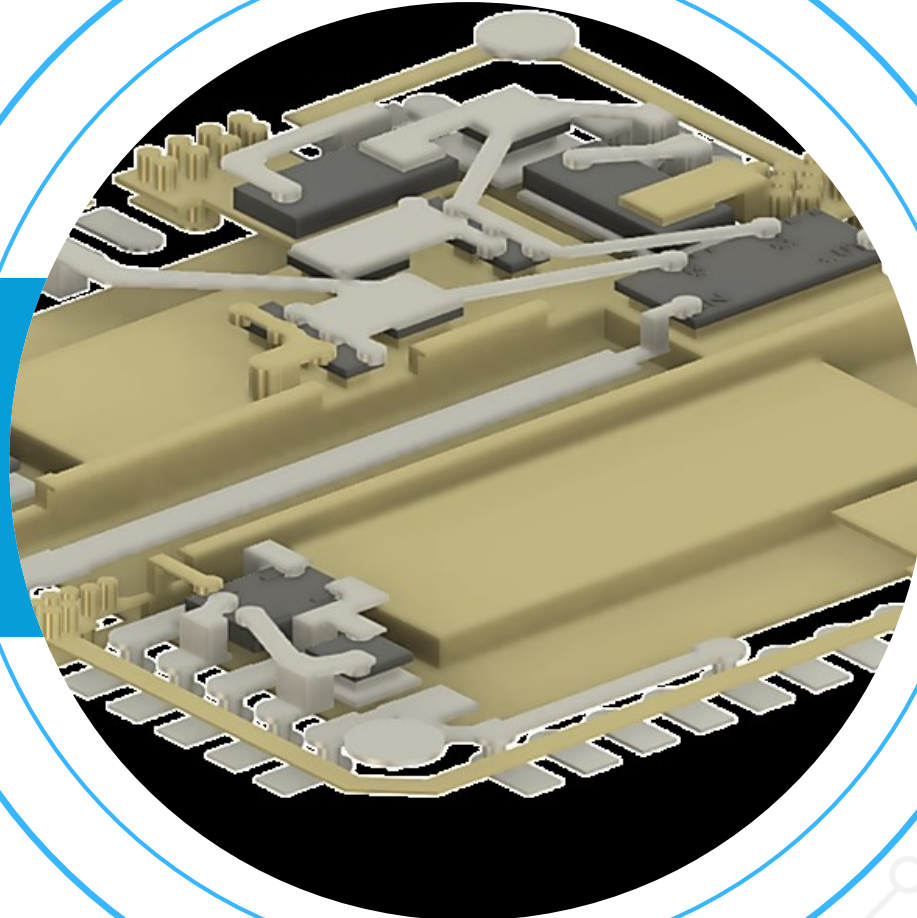
New Design Thinking

RF SYNTHESIZER –CONT’

- 3 steps process

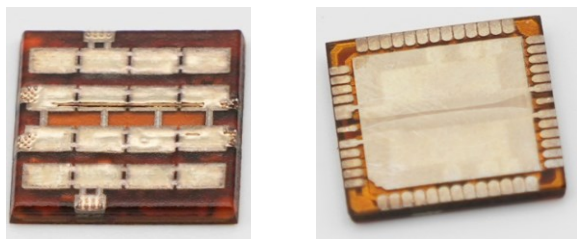


RF SiP

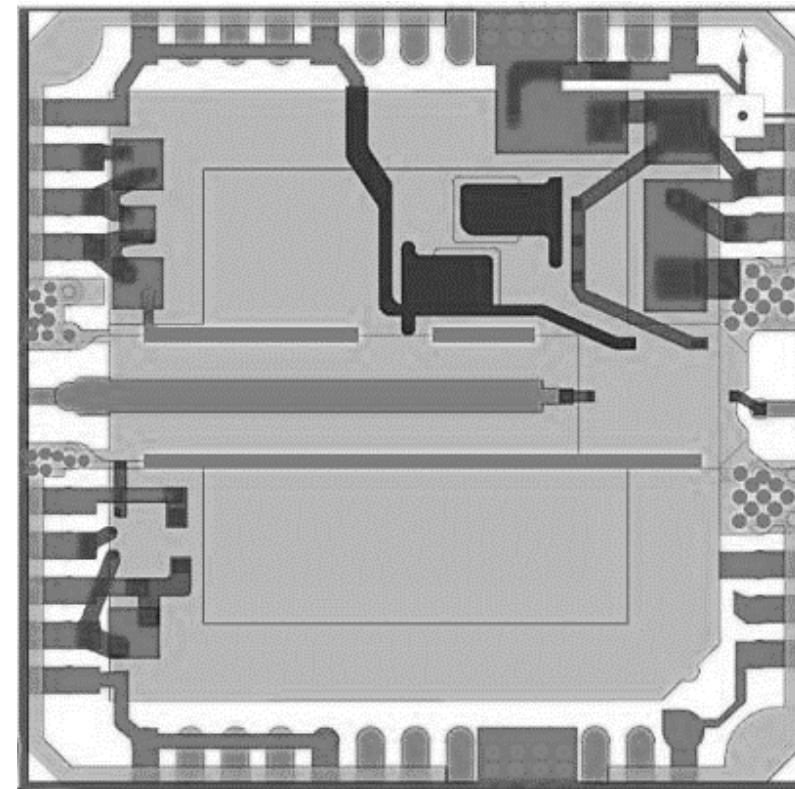
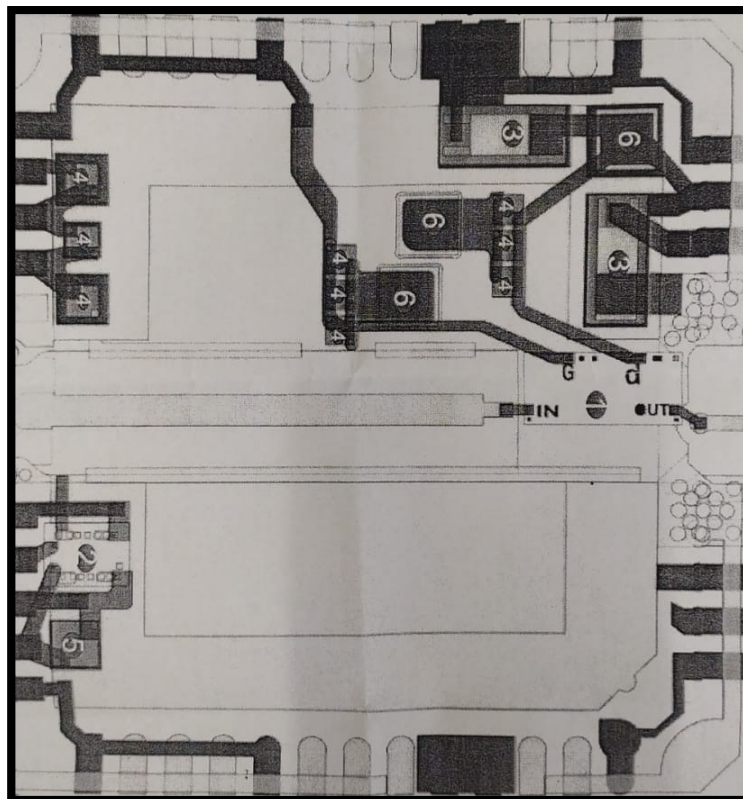


Schematic

- Main component:
 - MMIC 4W X-band die (QPA1022D)
- Other: Resistors (6), capacitors (3) and MOSFET dies.



13.2x13.2x1.5mm



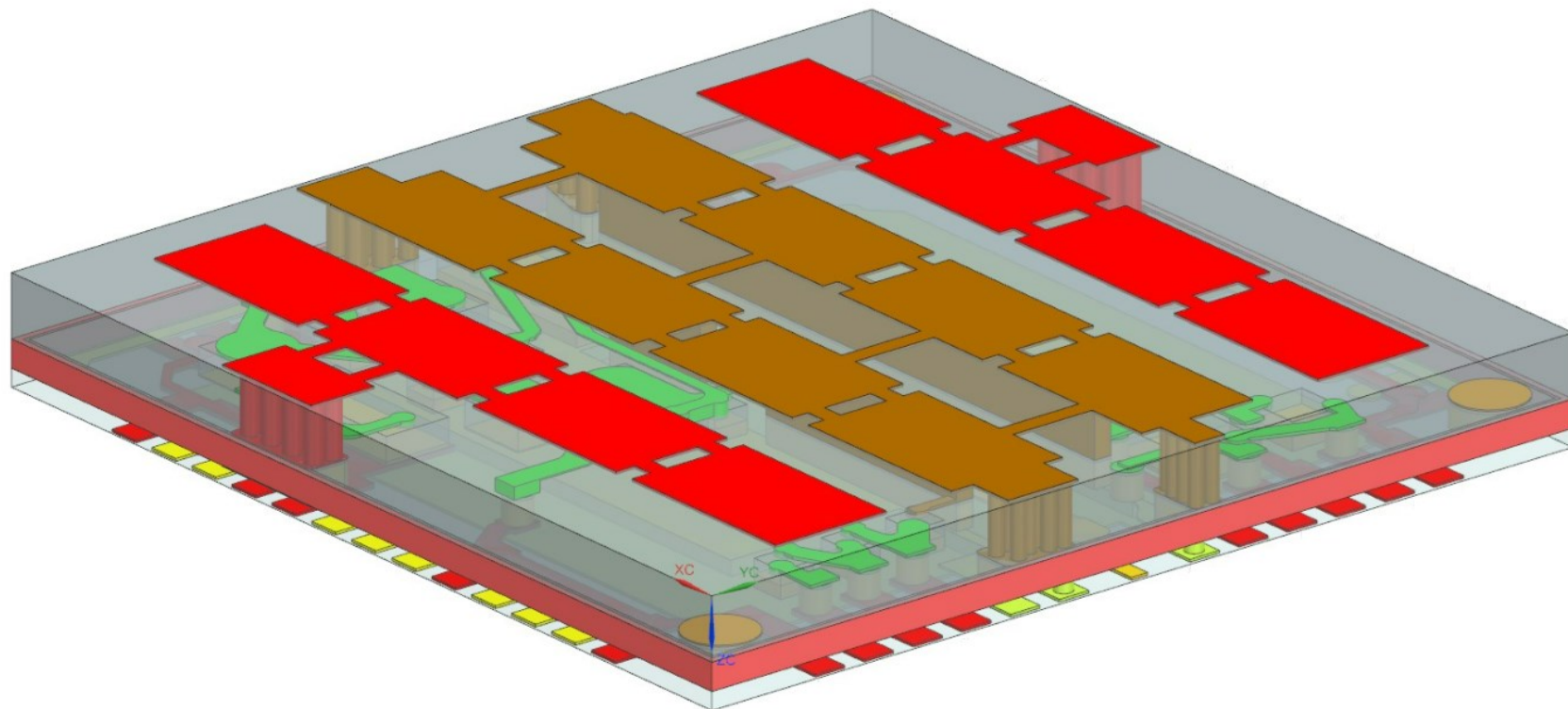
Layout and BOM

- Main component:
 - MMIC 4W X-band die (QPA1022D)
- Other: Resistors (6), capacitors (3) and MOSFET dies.
- Overall physical dimensions
 - 13.2x13.2x1.5mm
- Minimum pad size on die 80um.

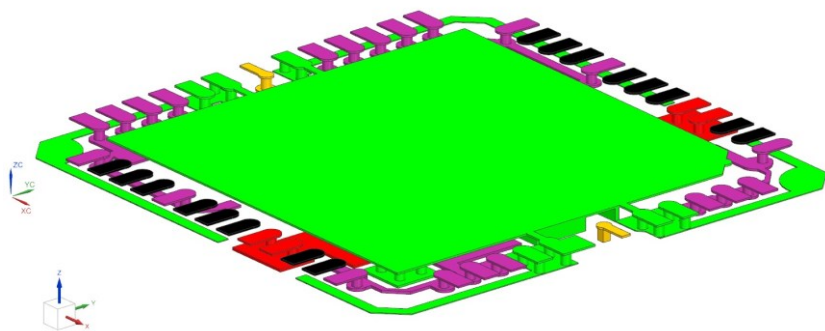
date av
k to upd

1 in NA

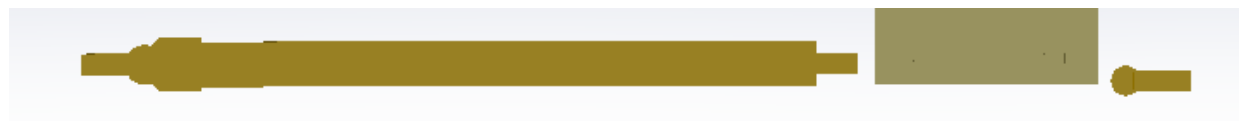
1 in NA



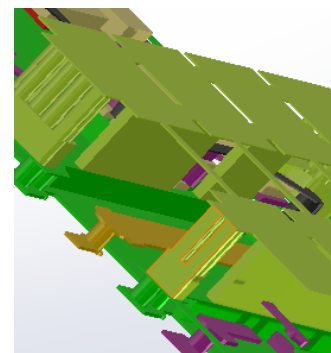
Layout and BOM –cont'



- QFN on bottom side.



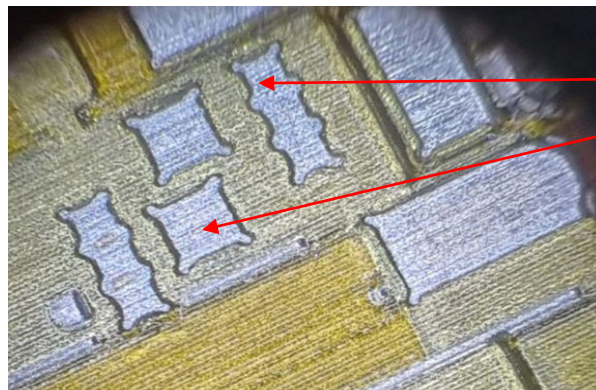
- Main 50-Ohm line



- Shielding for the RF line (walls)

Layout and BOM –cont'

- CAVITIES

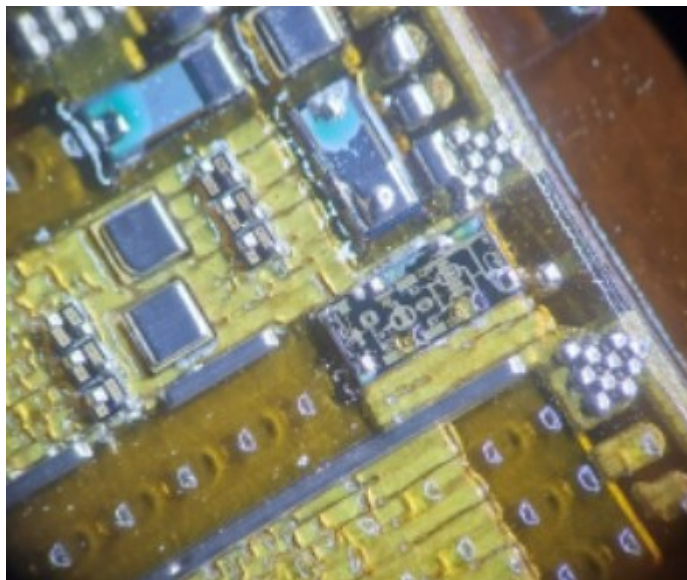


Cavities

- Before components placement

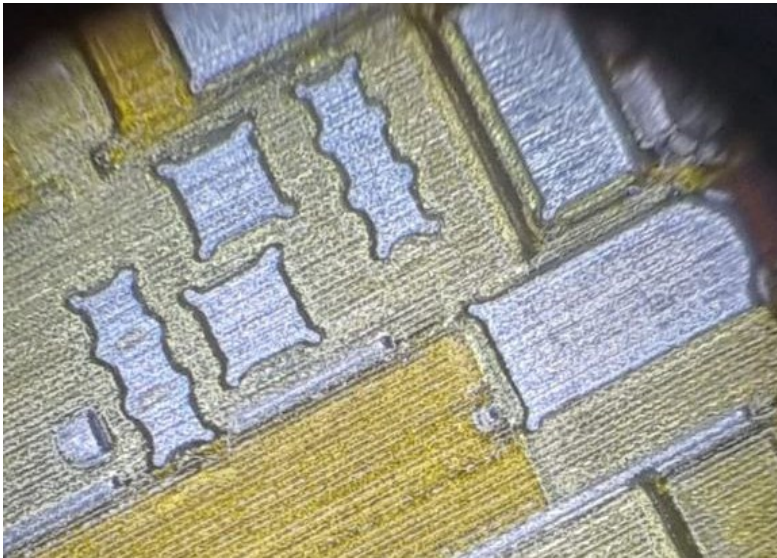
Layout and BOM –cont’

- COMPONENTS PLACEMENT

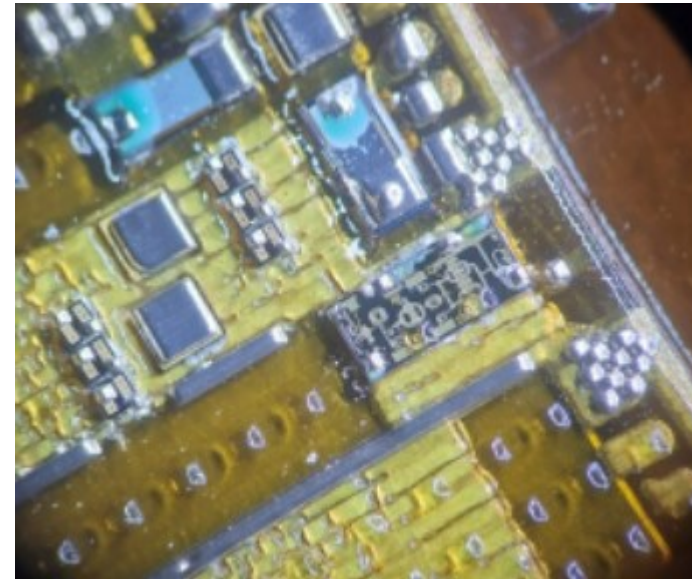


- After components placement

Layout and BOM –cont'



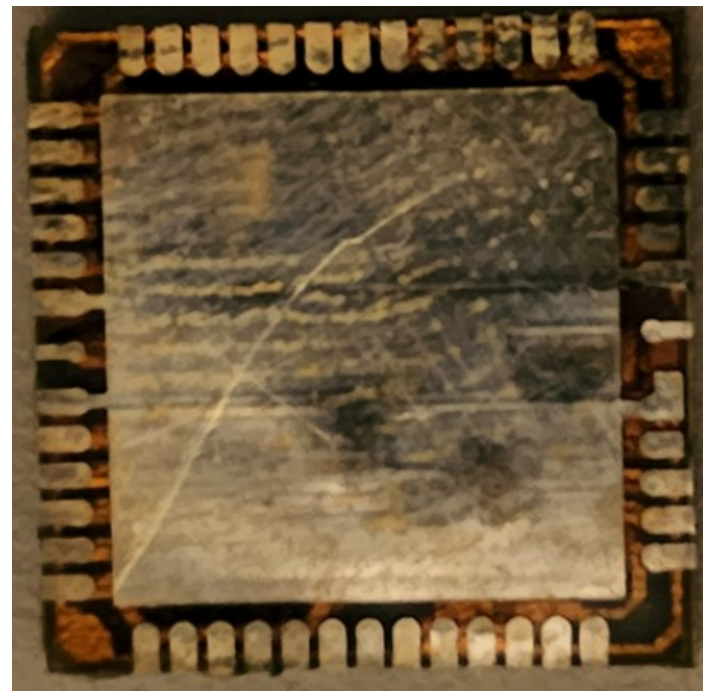
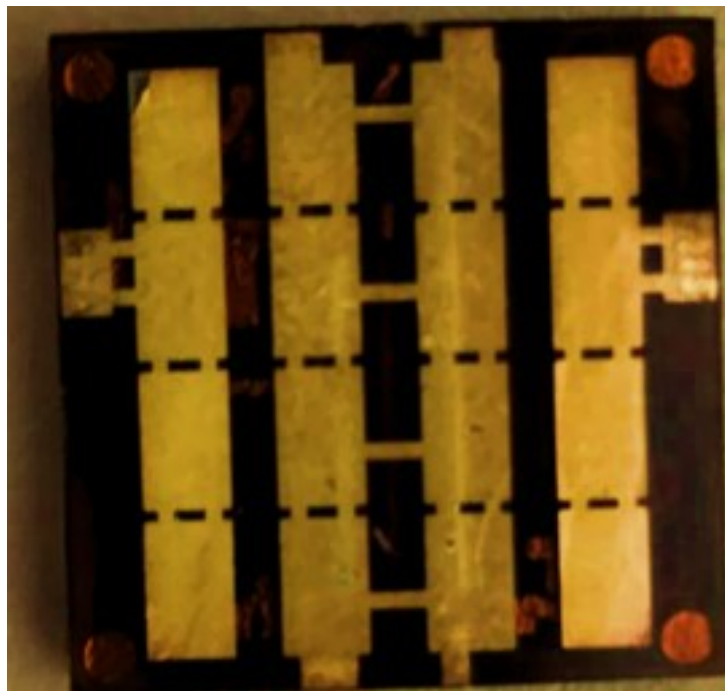
- Before components placement



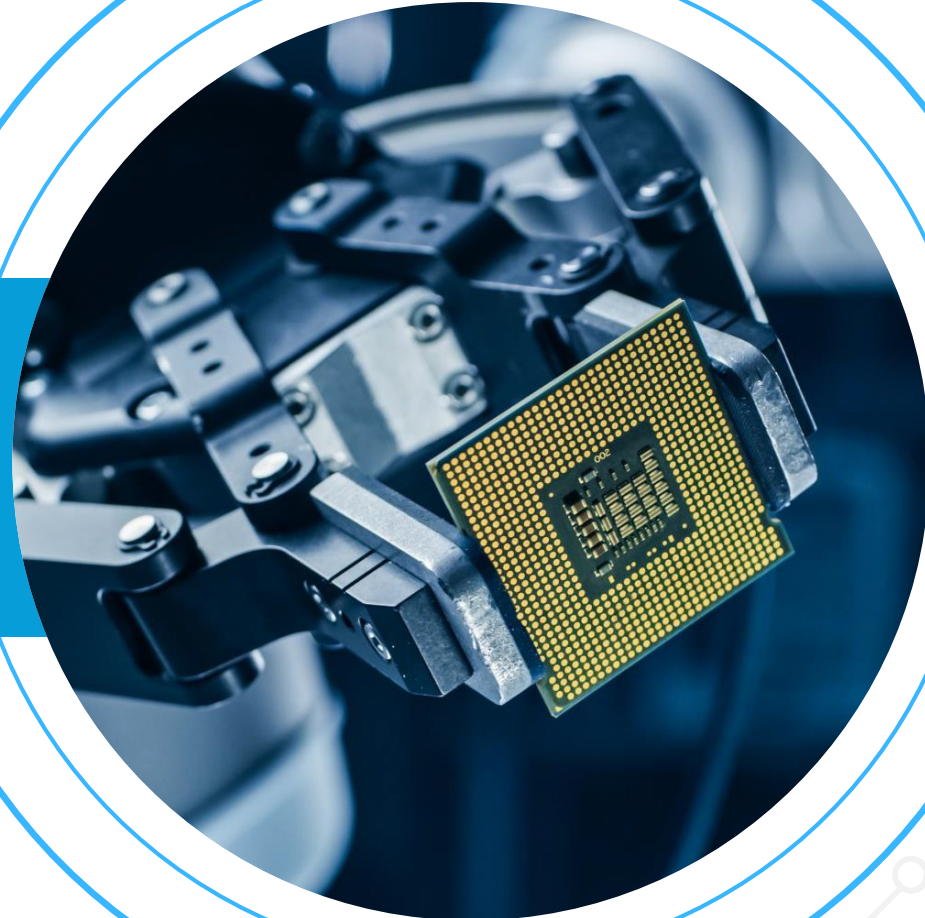
- After components placement.

Layout and BOM –cont’

- FINAL TOP & BOTTOM VIEW



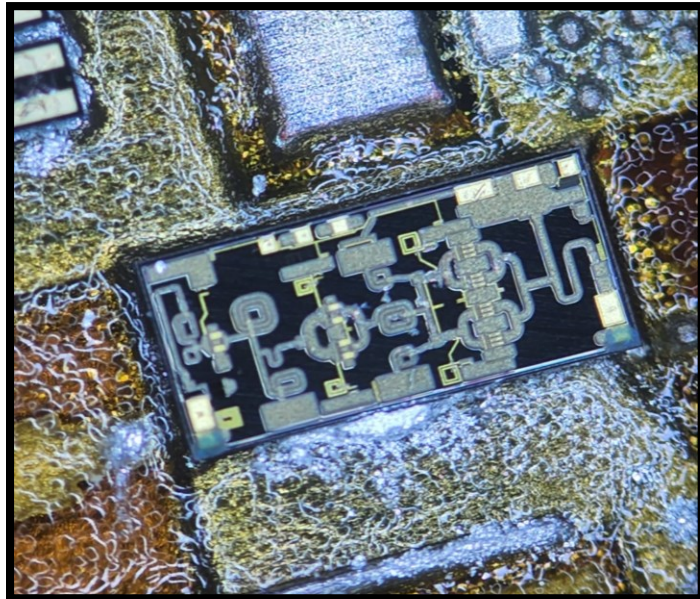
AME Packaging Processes



Top level processes available

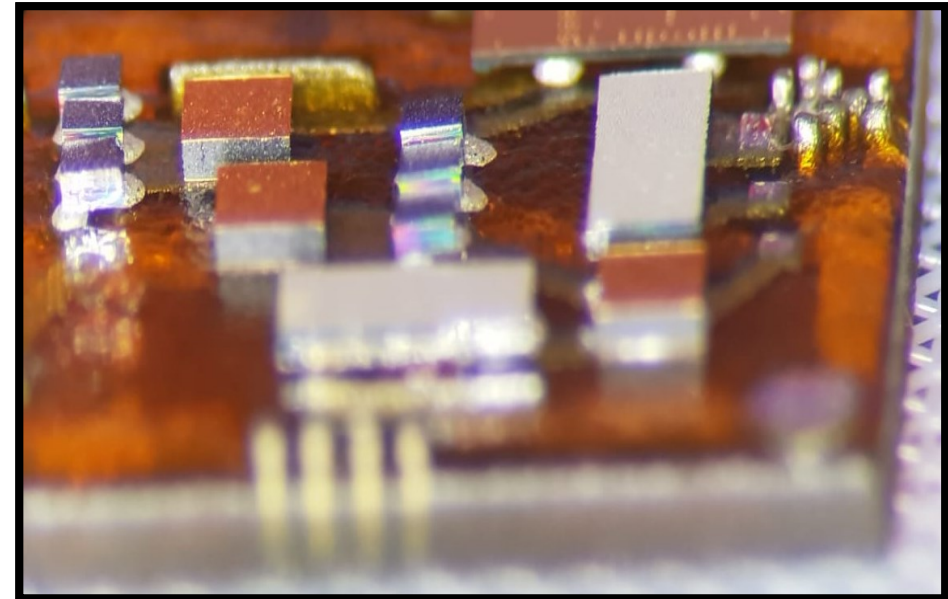
AME PACKAGING PROCESSES

Split Assembly



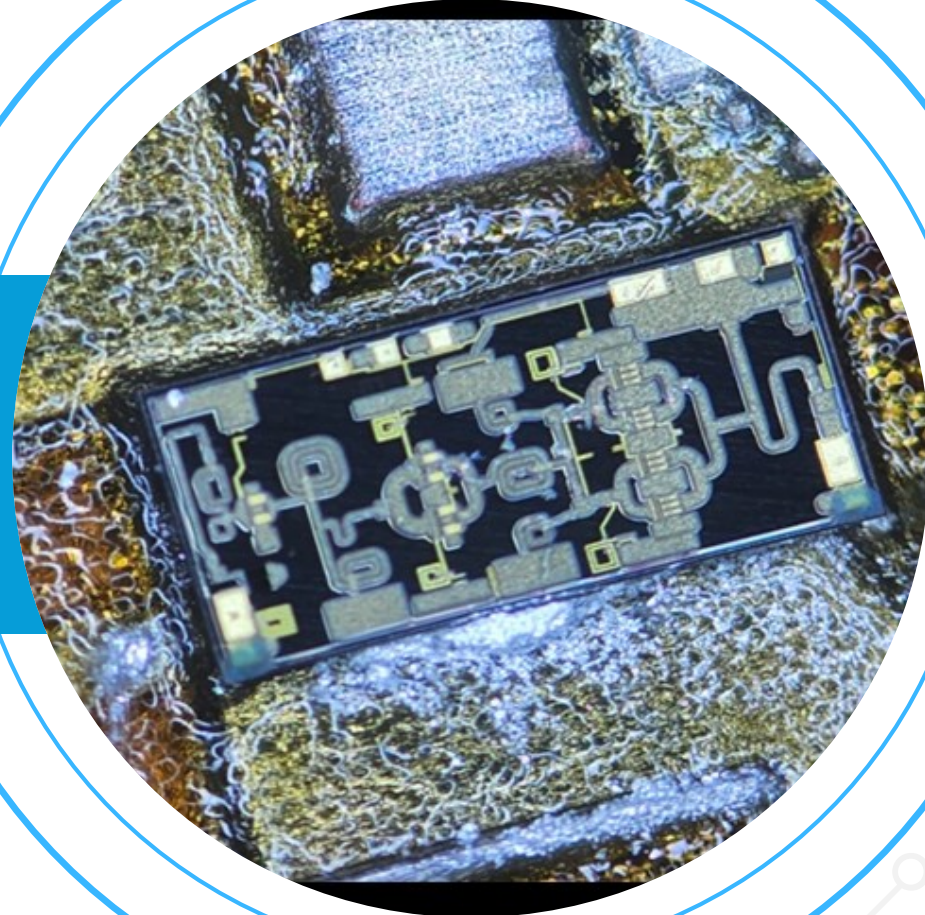
Manual placement of Die is possible

Flip Chip

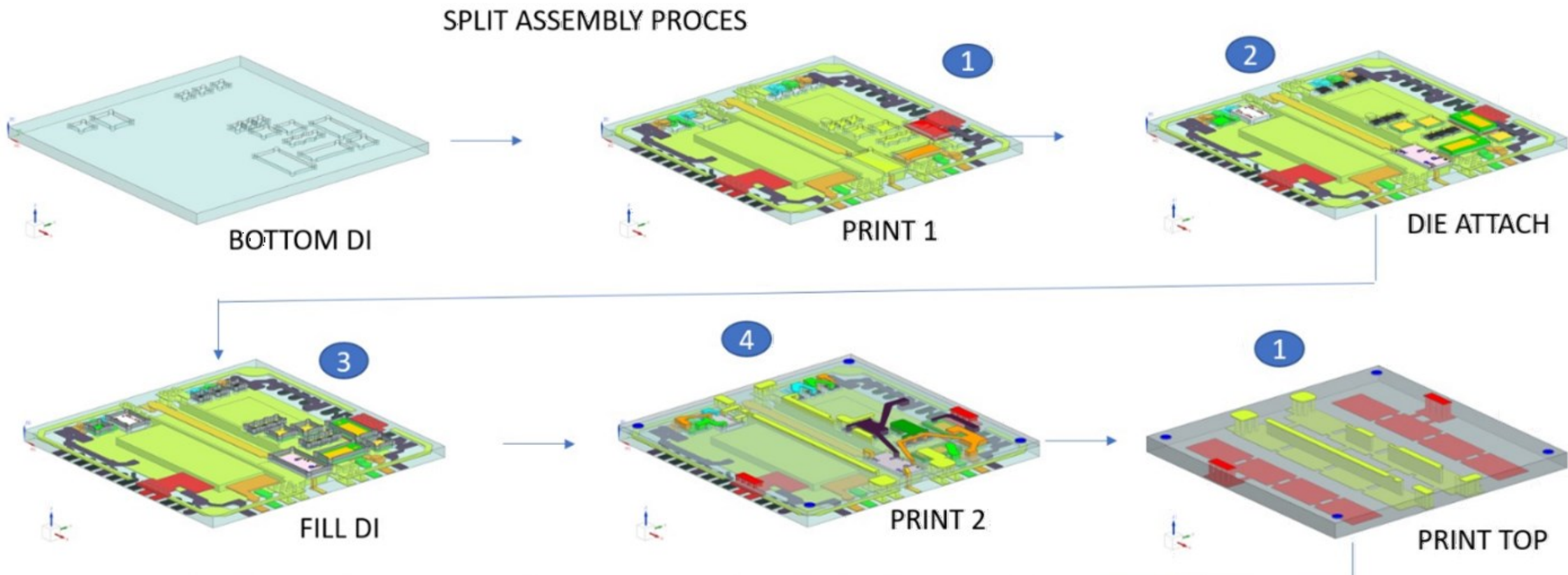


High Accuracy Automatic placement is required

Split Assembly



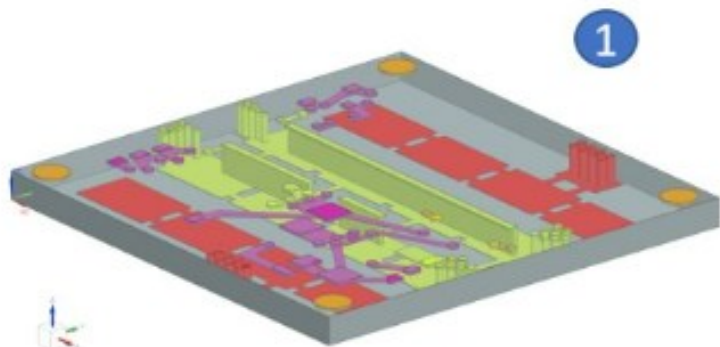
Split assembly process



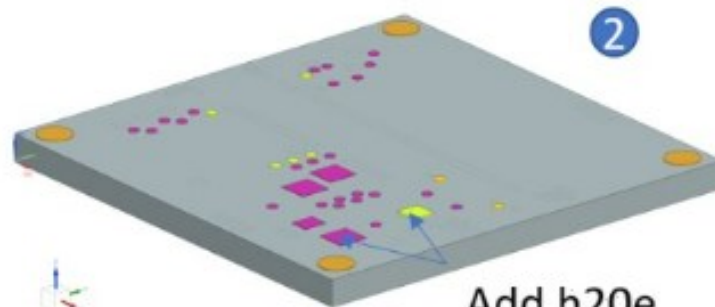
Flip-Chip



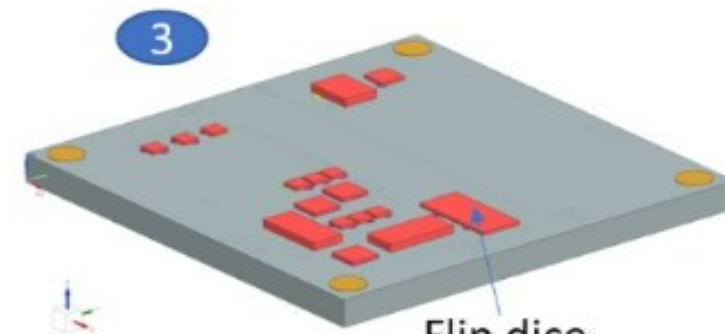
Flip chip assembly process



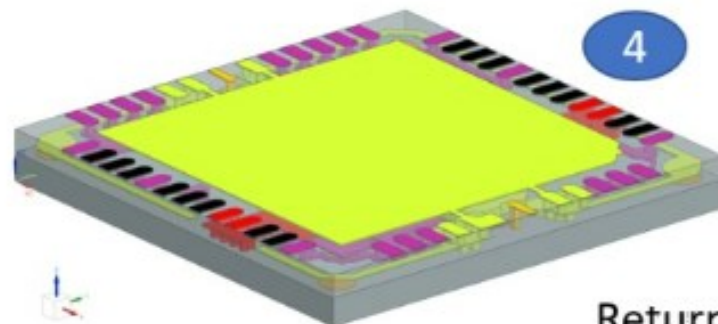
Print bottom



Add h20e

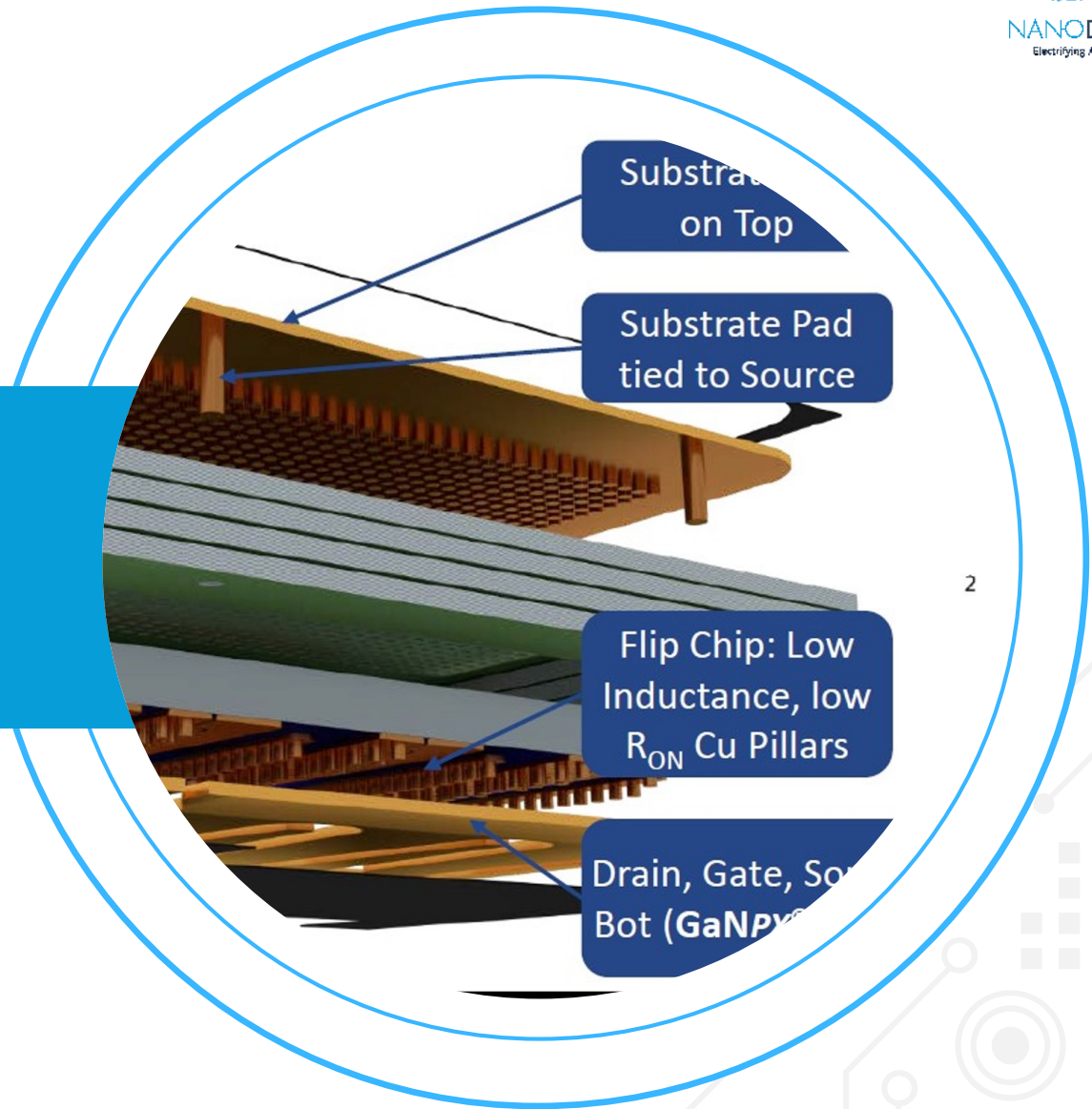


Flip dice



Return to printer
and print top

Power Transistor AME Packaging

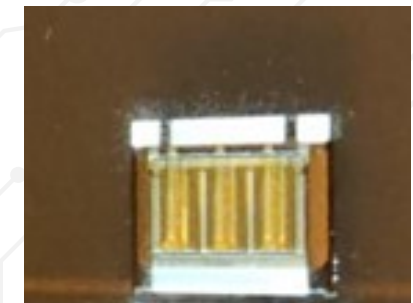
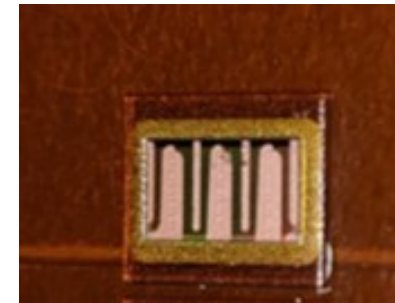
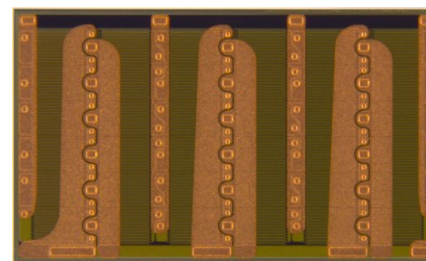
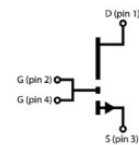
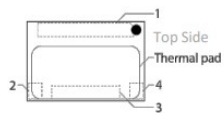
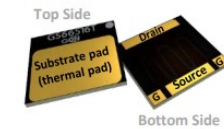
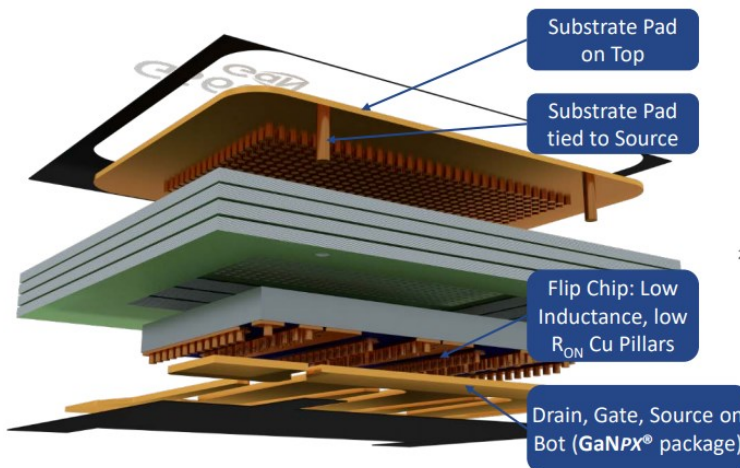
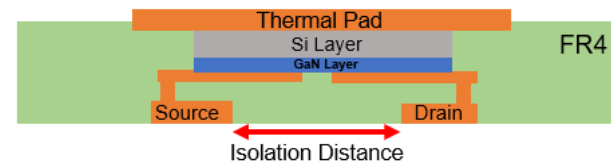
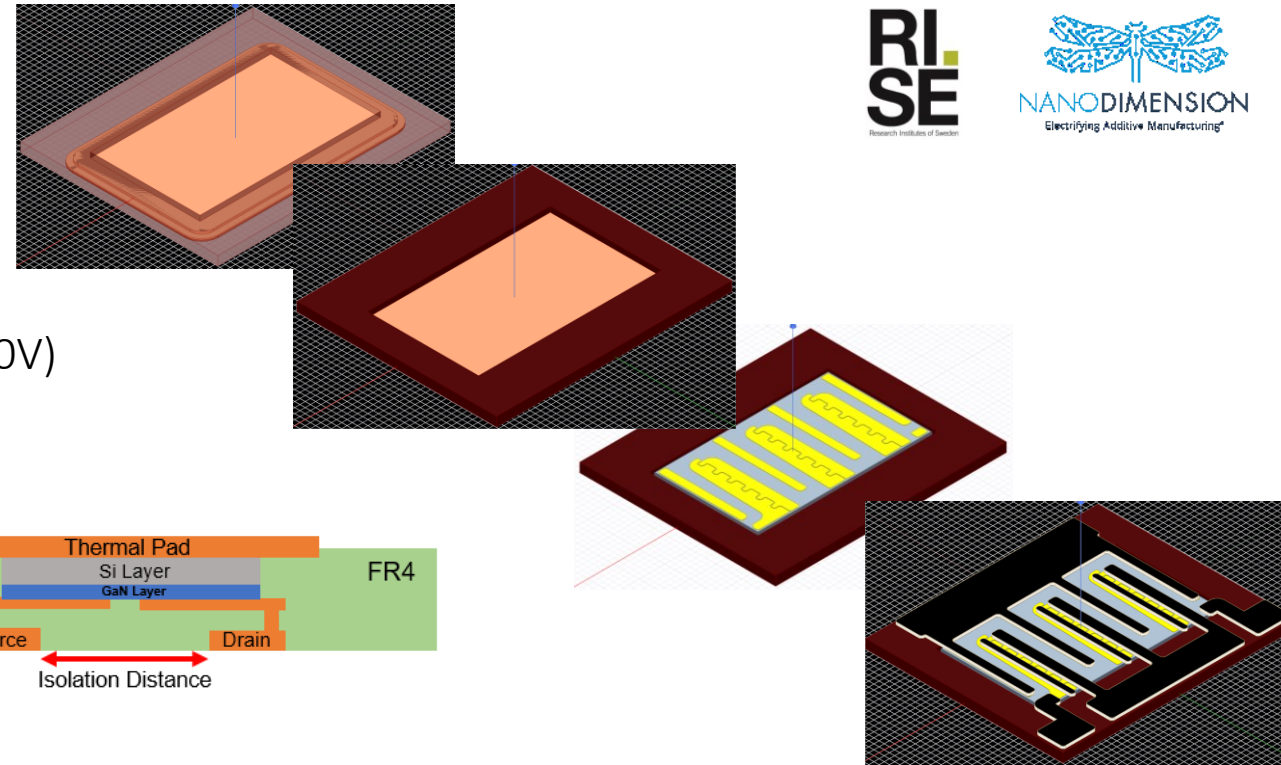


2

Power Transistor SiP

GAN-ON-SILICON

- Enhancement mode GaN-on-silicon power transistor (650V)
- Top-side cooled configuration
- High current $I_{ds(max)} = 60A$
- $R_{ds(on)} = 25m\Omega$
- Very high switching frequency ($> 100MHz$)
- Small 9 X 7.6 mm PCB footprint



Power Transistor SiP

GAN SYSTEMS (GS66516T)

Commercial Package

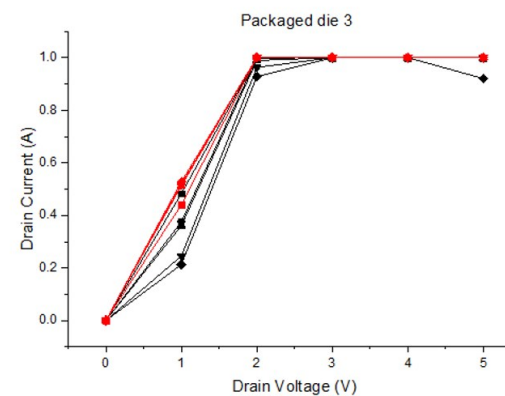
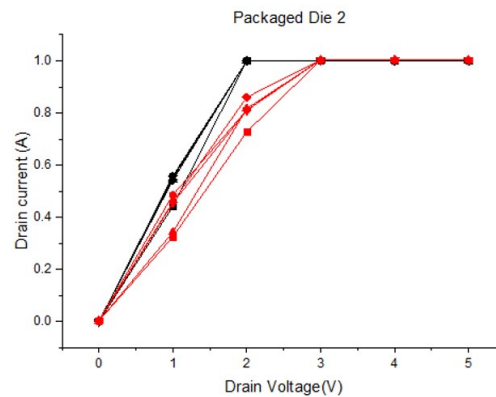
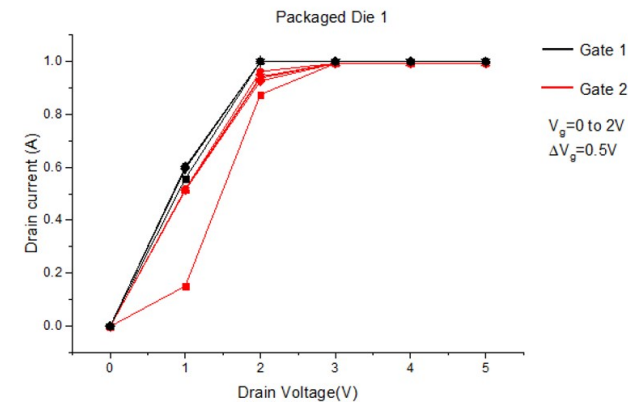
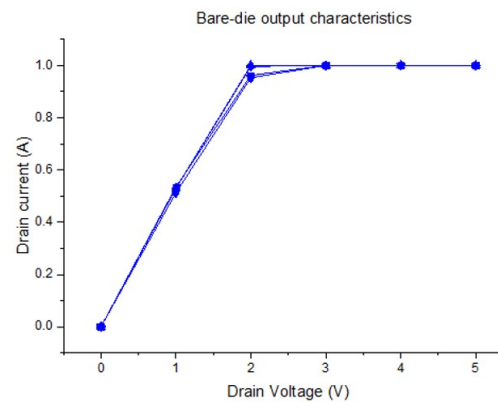
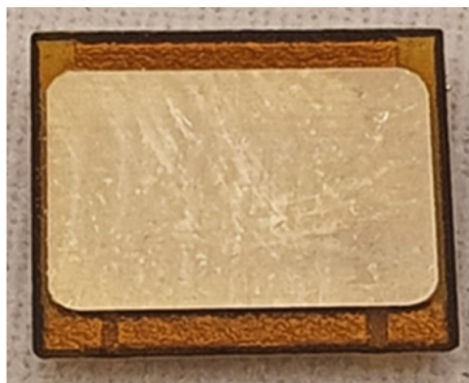


Top Side



Back Side

Printed Package

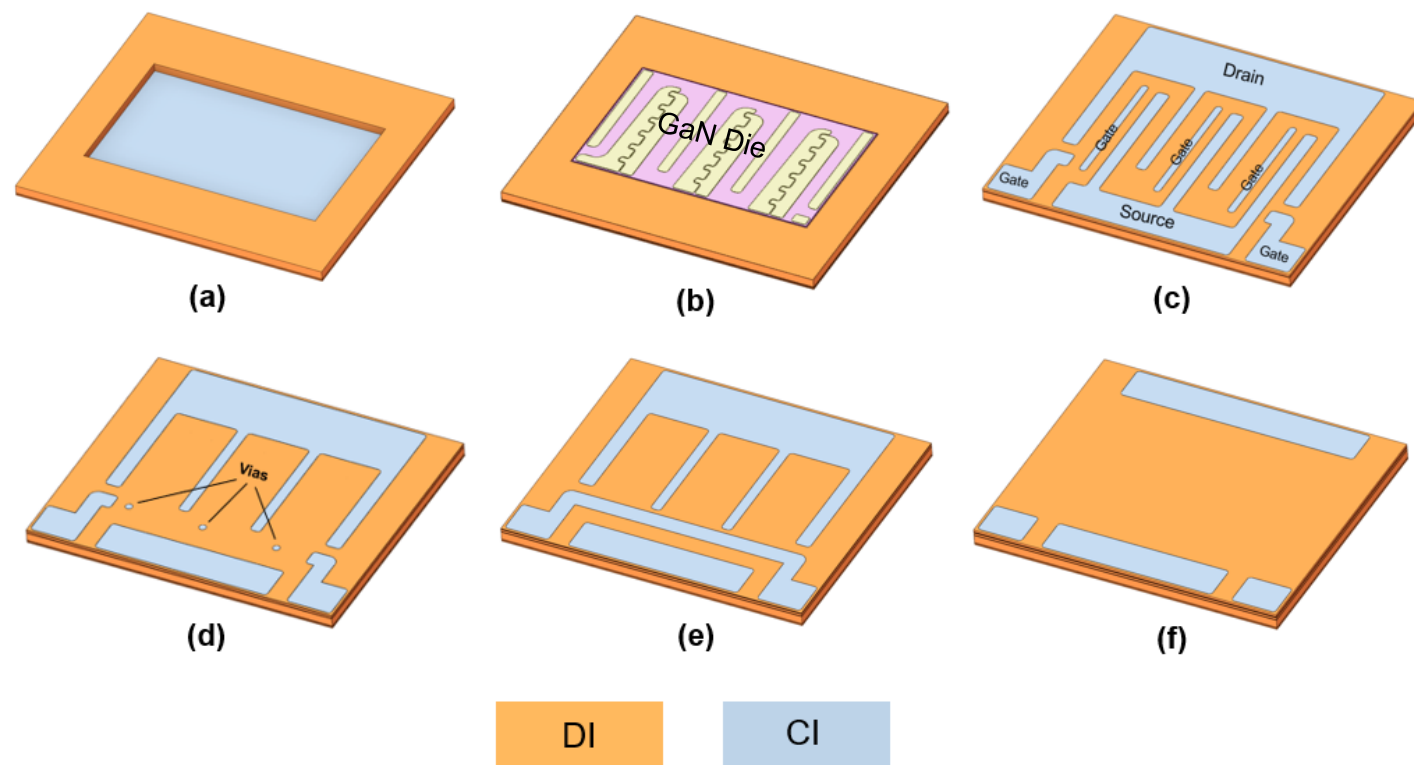


Power Transistor SiP

GAN-ON-SILICON

Process:

- a) Printing dielectric cavities & pause the print (keeping chuck at 100°C)
- b) Placing the silicon dies and adding Epotek conductive glue on the bare pads
- c) Print DI “soldermask alike” and fill gaps
- d) Print CI pads connection
- e) Print interconnecting tracks
- f) Print cover layer



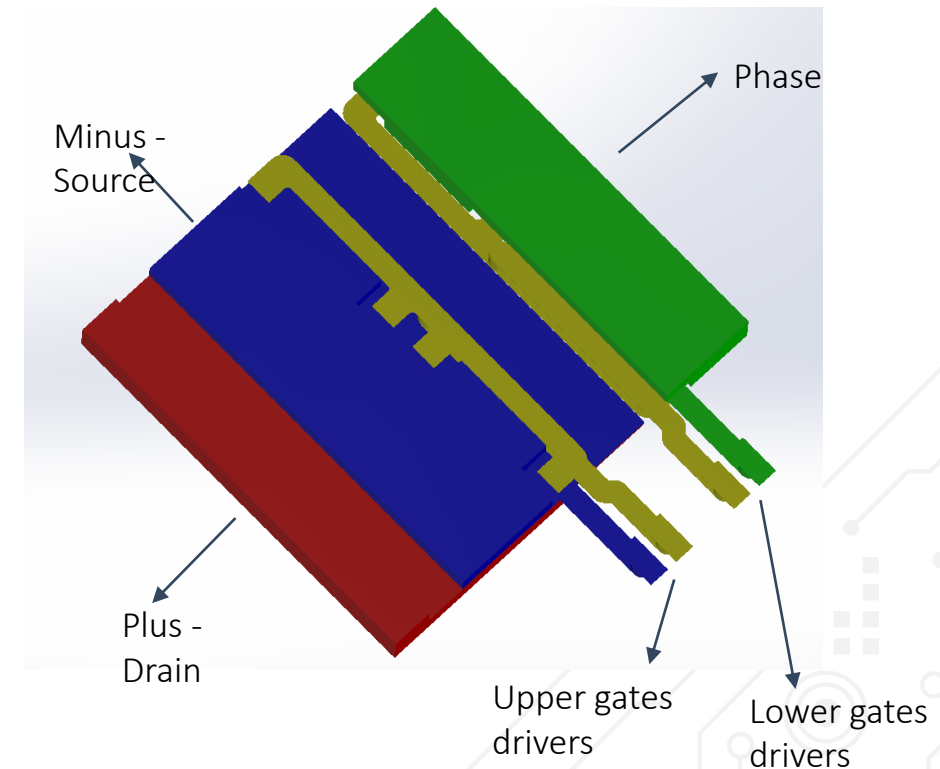
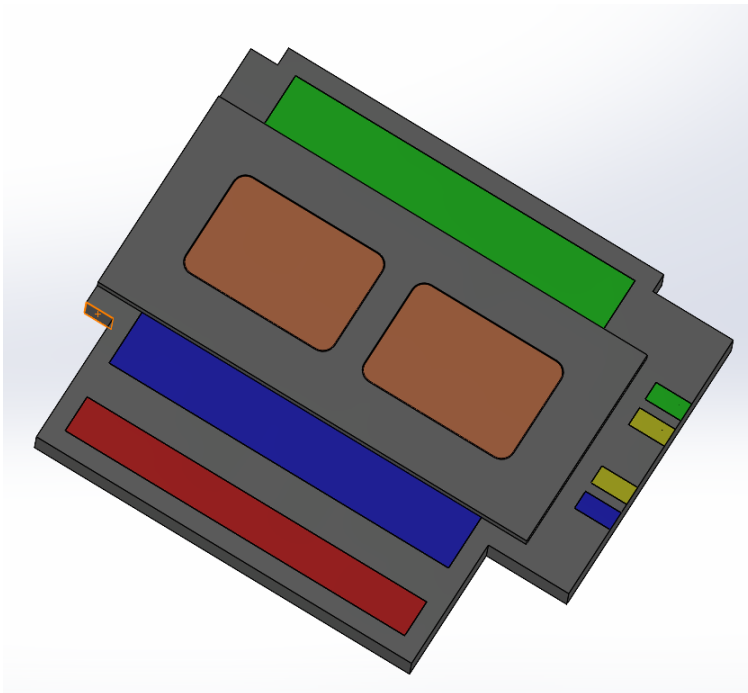
Power Transistor SiP

RI.SE DESIGN FOR AME

- A very compact module with four GaN discretes was designed.

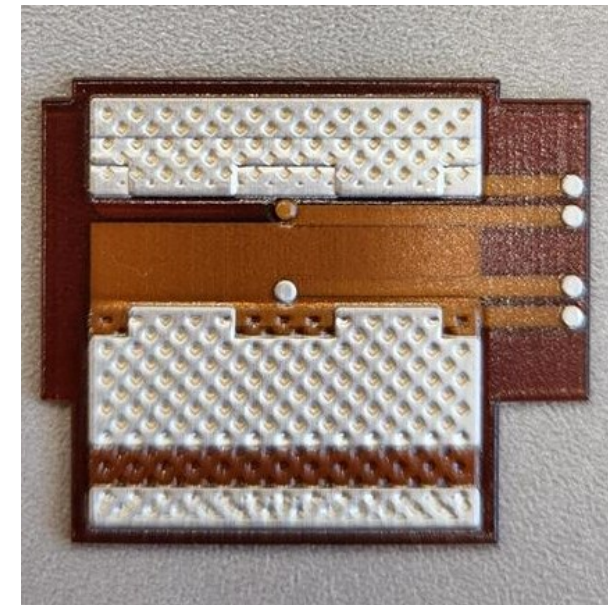
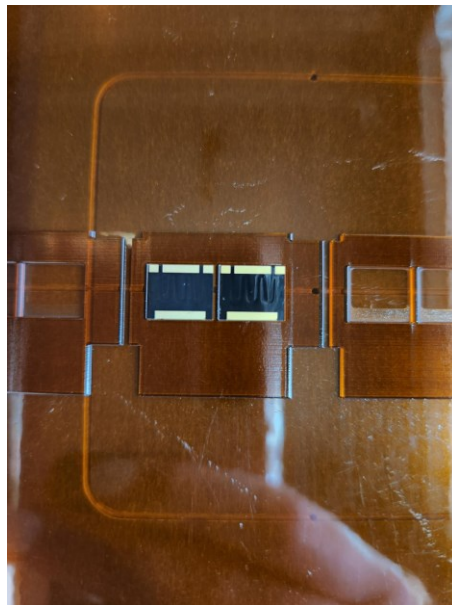
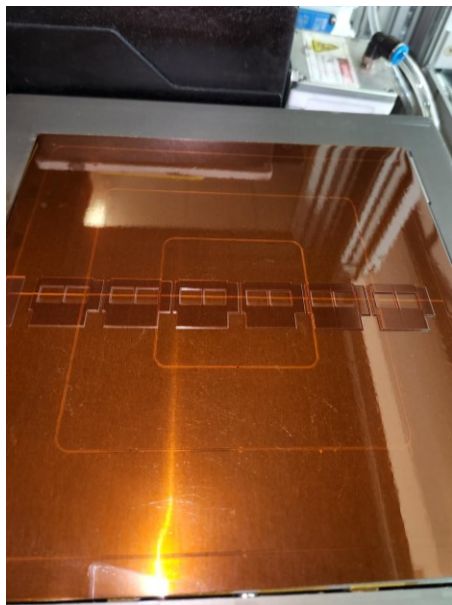
Challenges:

- Meeting the application targets – High voltage, high current
- Effective heat dissipation – High current



Power Transistor SiP

GAN-ON-SILICON



Power Transistor SiP

GAN-ON-SILICON

Module with four GaN HEMTs ($V_{DS} = 650\text{ V}$, $I_{DS} = 60\text{ A}$, $R_{DS(ON)} = 25\text{ m}\Omega$)

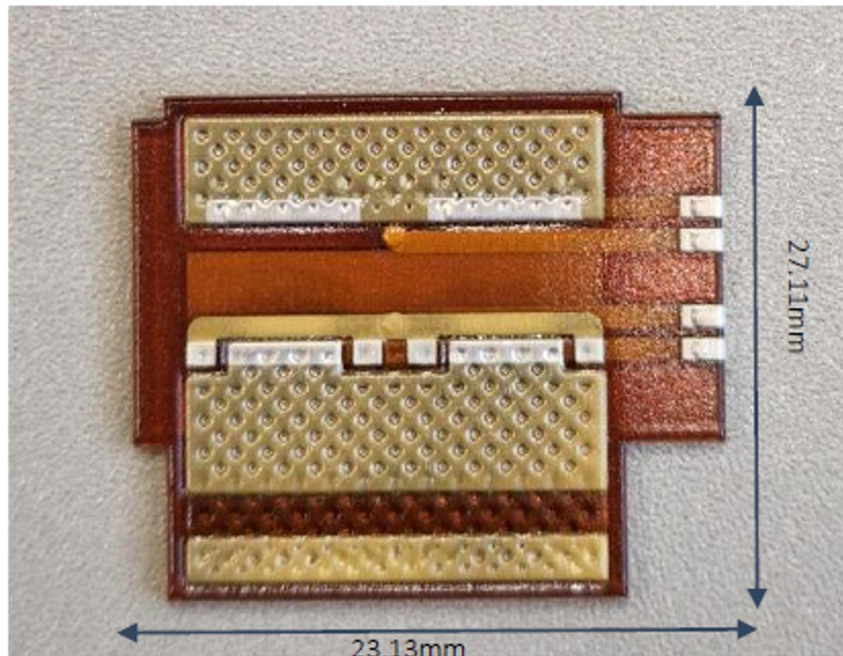
- The AME method have proven to be very time efficient!
 - 2-3 complete packaging iterations within 2-3 months – this normally takes years

The Smallest
High Power Module
of its Kind

Printed with AME technology

“ The device’s mechanical characteristics are approximately 64% smaller than the smallest similar functional devices existing in the market and will create the highest power density for this kind of device.

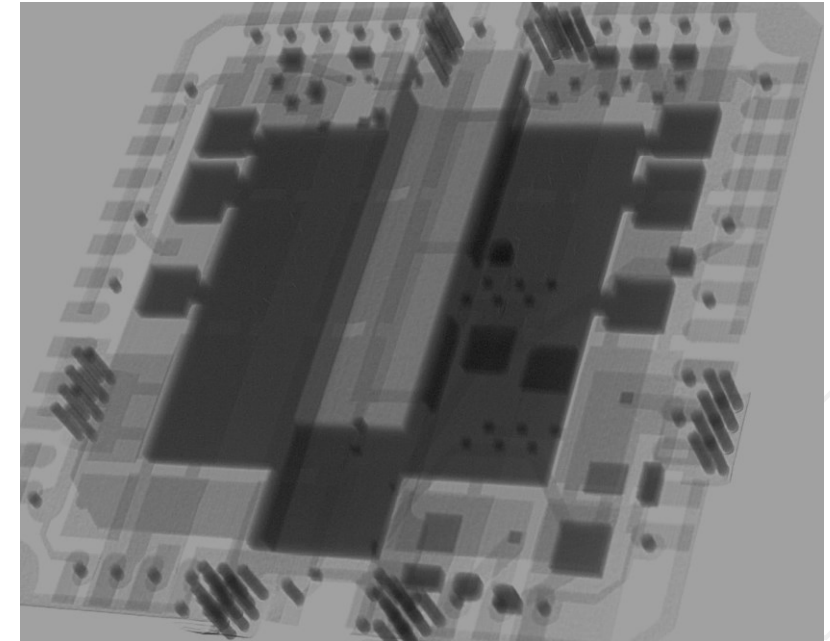
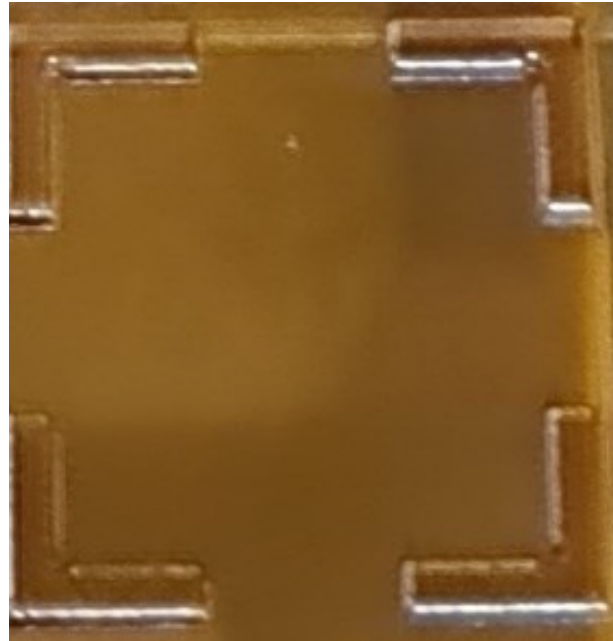
Furthermore, this is the first attempt to use 3D AME technology to reduce size, reduce manufacturing time and improve power density in this kind of circuit.”



Main Process Challenges

- CHALLENGES AND SOLUTIONS

- Registration:
 - Dies placement.
 - Building up the VIAS on top of the dies
 - Removing print for P&P.
- Pushing the current boundaries of design rules and process.





THANK YOU!



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