Wafer level packaging based on wafer bonding and TSVs for advanced MEMS integration

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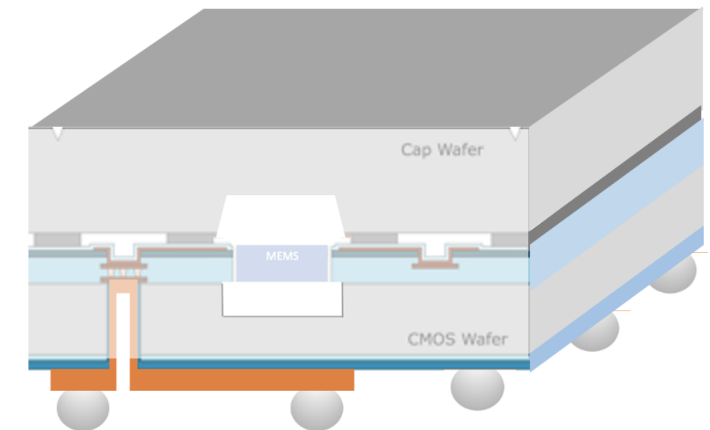
Electronic Packaging and Applications



System in Package vs. System on Chip

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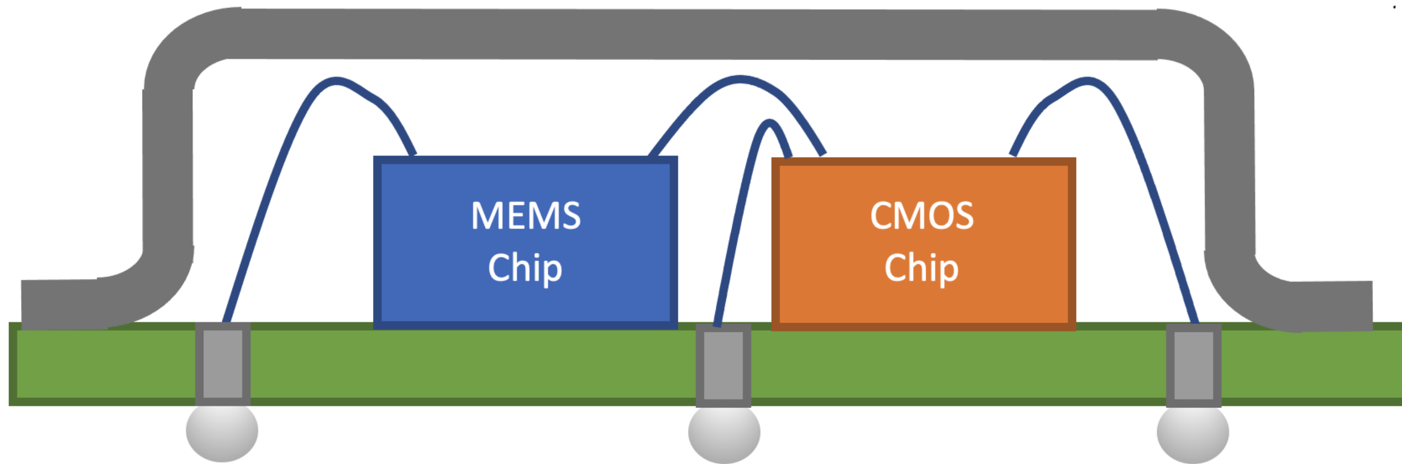
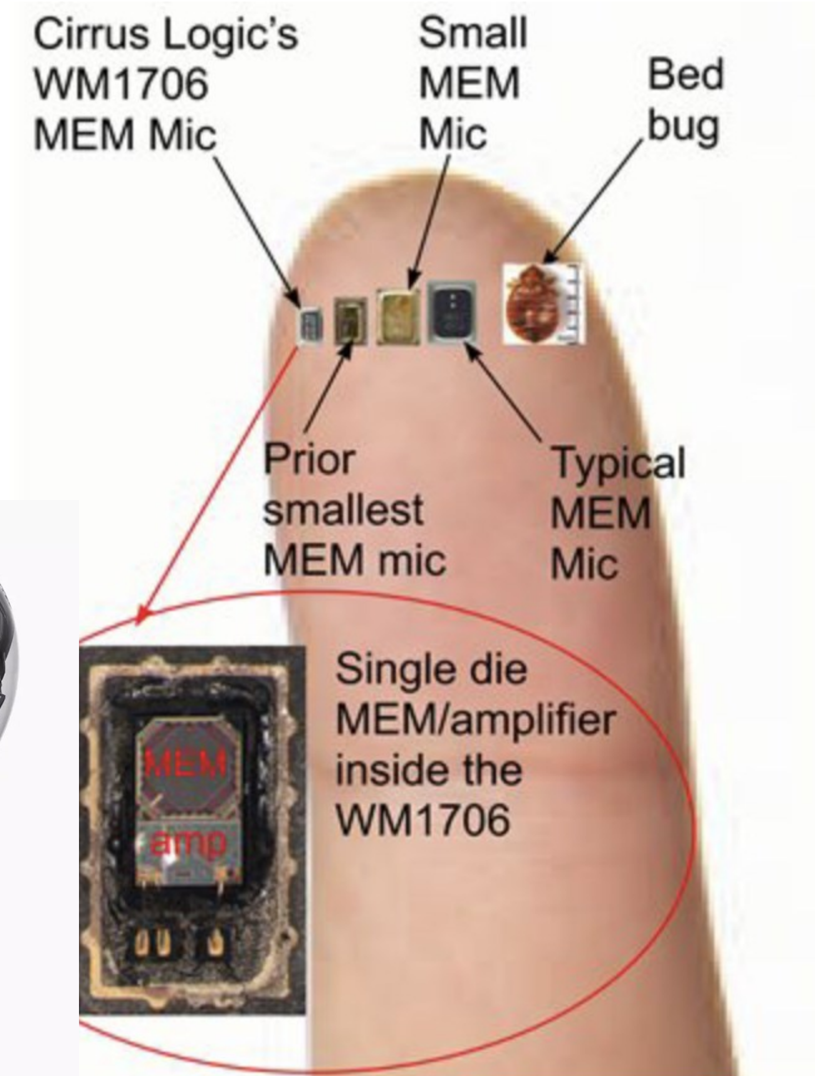


System in Package (SiP) – Package is the integration level widely used – standard, different solutions

+ flexible combination of MEMS and CMOS
- form factor – rather big and bulky
- distributed supply chain (foundry, assembly house)



SoC is focus of the presentation, how to realize proce

Outline

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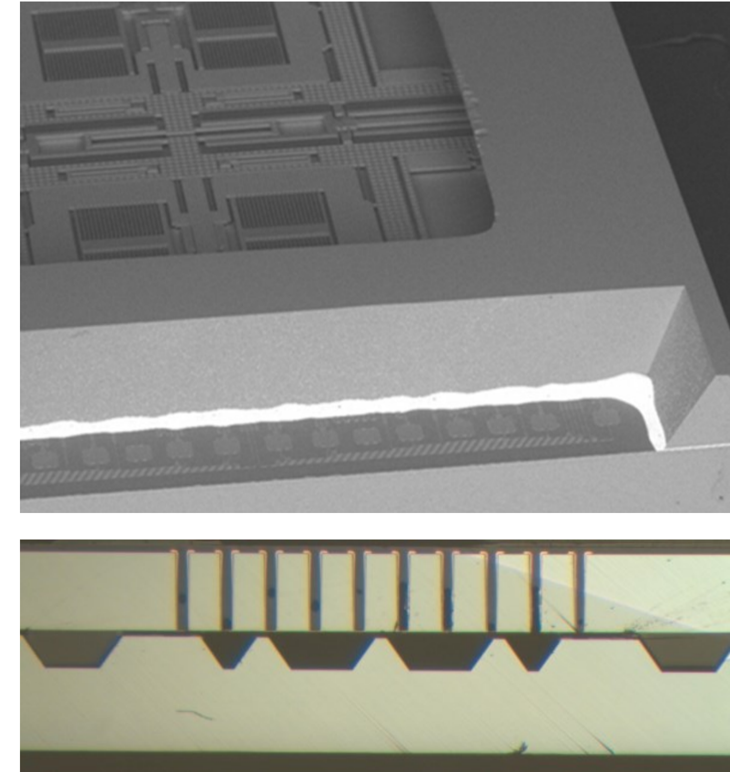
Introduction
- The principle of System on Chip and Wafer Level Packaging
- The Basic Process Integration Scheme

The Basic Process Modules
- Monolithic Integration of MEMS and CMOS
- Wafer Bonding
- Through Silicon Vias
- Finishing after Wafer TSV Process

An Example of a System on Chip – Chip Scale Package Solutions

Application Aspects and Special Challenges

Conclusions and Outlook



The principle of System on Chip and Wafer Level Packaging

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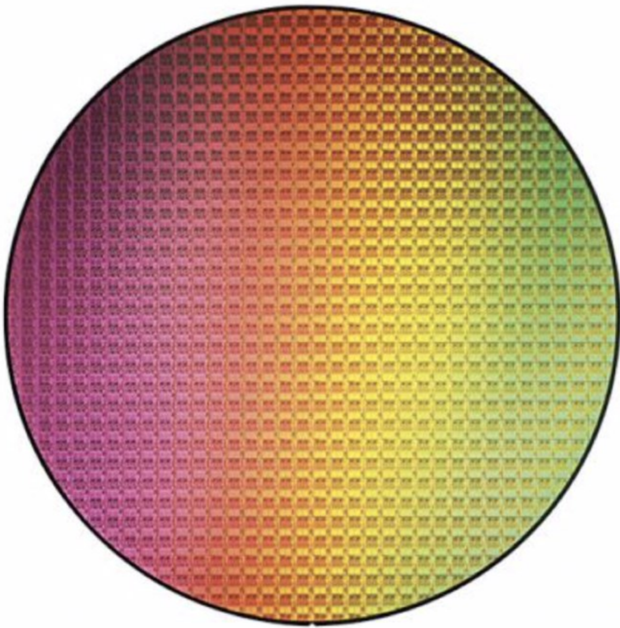

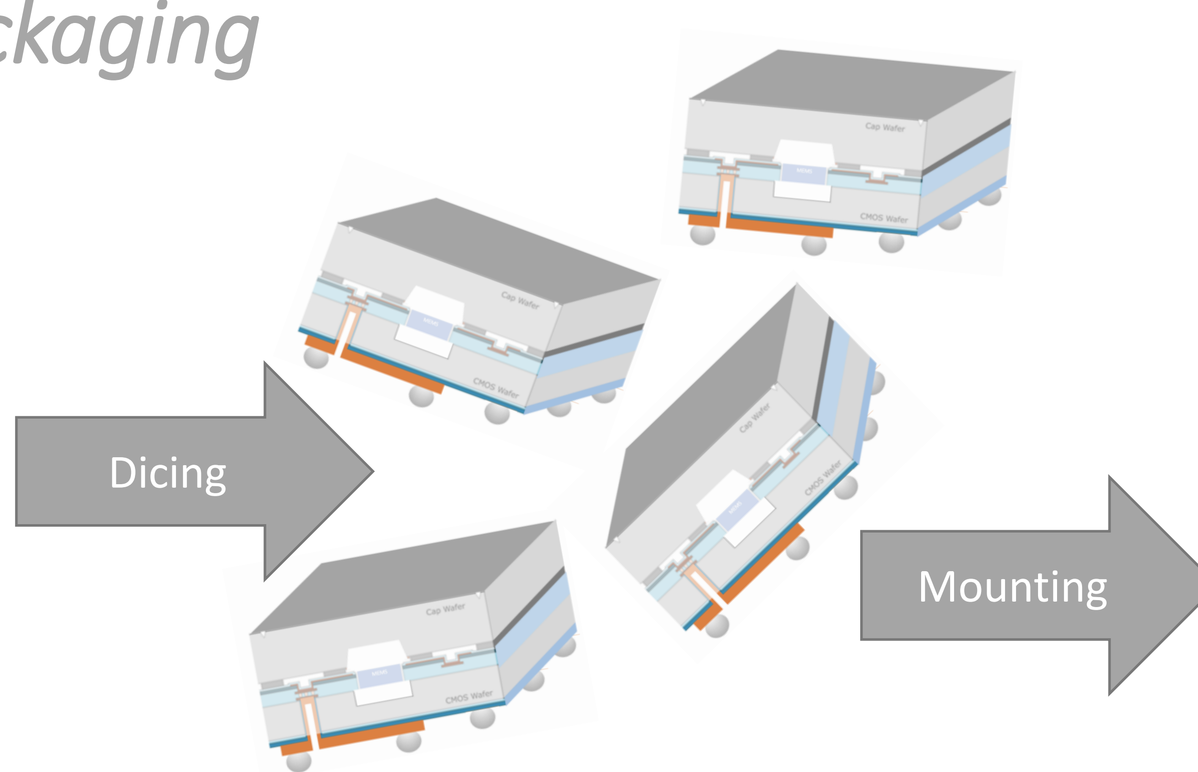

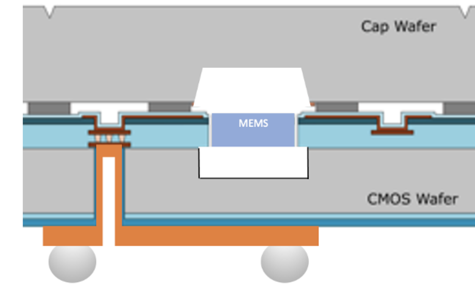

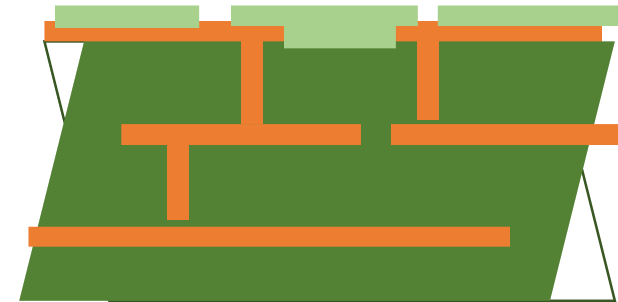

Do ***all*** the processing on wafer level
- Highest integration
- Parallel processing
- Cost efficient

Chips directly ***ready for mounting on board***
- All functionalities (CMOS, MEMS)
- Solder balls or solder pads
- Passivation and solder stop
- Smallest possible form factor

Highly integrated bords
- BCB or Ceramics
- Small solutions
- High functionality

The basic process integration scheme

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Application Idea
Concept

Electronic
Functions

CMOS

Sensor and
other Functions

MEMS

Capping, Sealing, Protecting
WAFER BONDING

Contacting
TSV, BGA, UBM, SOL-STOP

Wafer Process
FOUNDRY / IDM

Fully Functional Chip

BCB and Ceramics
Requirements

Materials
Processes
Design
Reliability

Modular
Approach for
Flexibility in
Development
and Production

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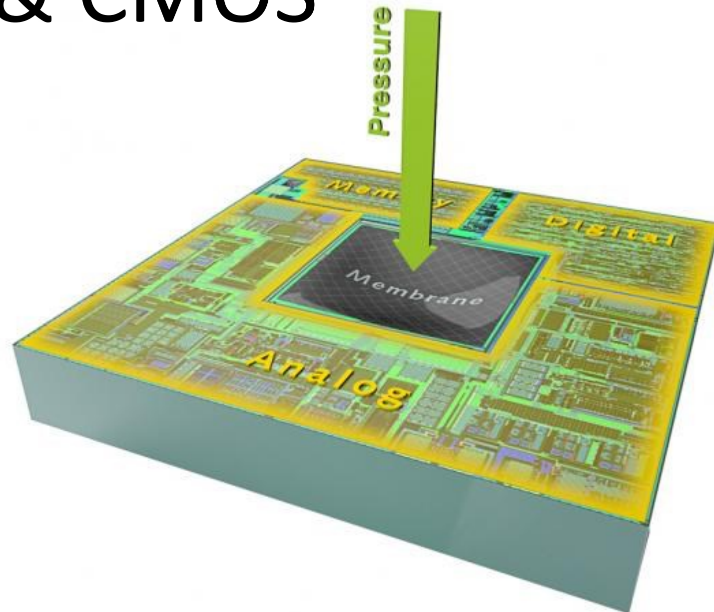
Monolithic Integration MEMS & CMOS



Wafer Bonding

TSVs

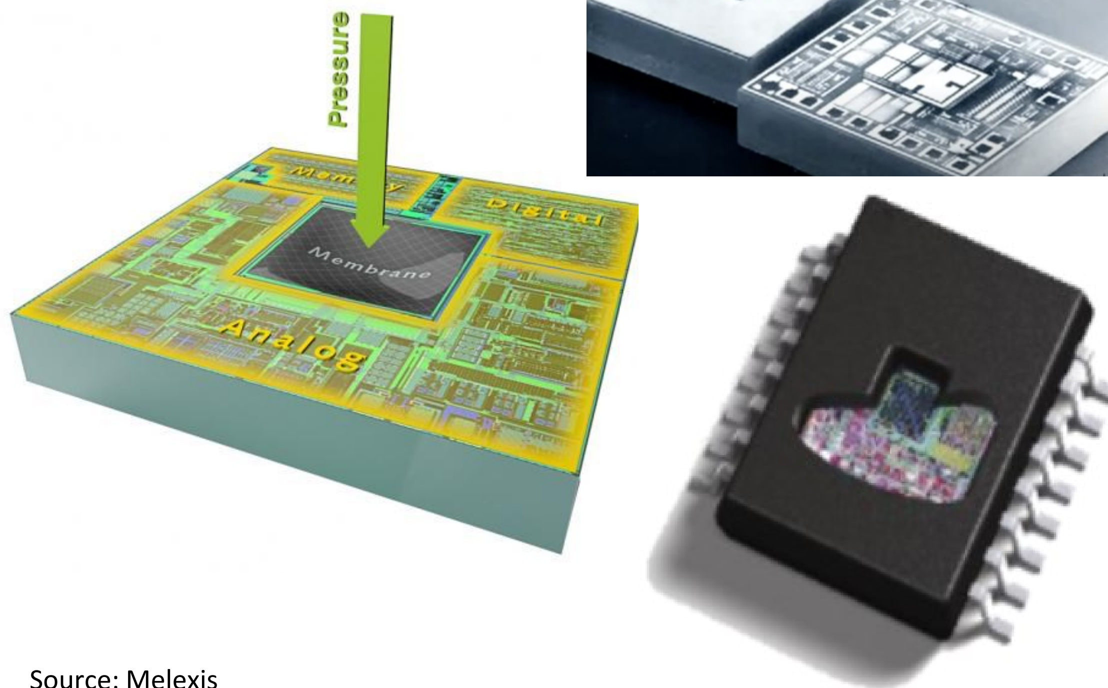
… with RDL, UBM, Solder Stop

… and how all can fit together

MEMS Devices requires electronics

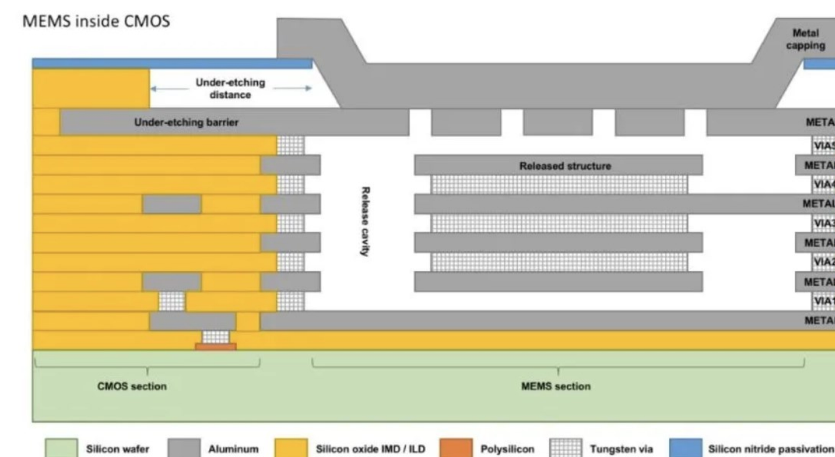
- Signal processing, sensor signal improving, driving signals,….
- Integration of MEMS ad CMOS on one and the same wafer/chip is well established

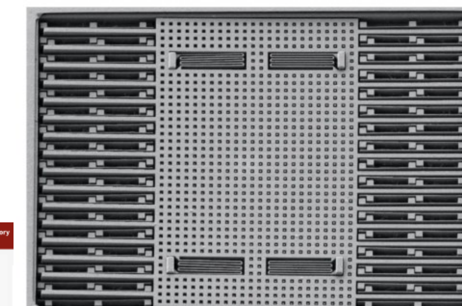
Bulk Micromachining



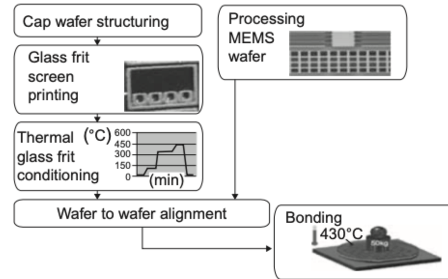
Source: Melexis

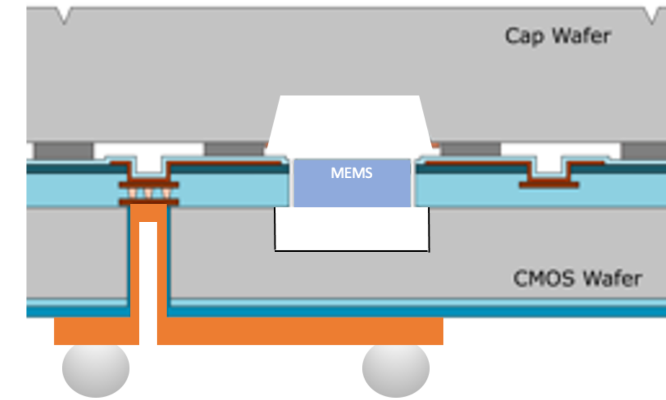
Surface Micromachining





A 2D motion sensor built in 0.18-µm CMOS (Image: Nanusens)

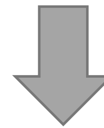


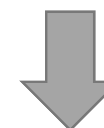


Wafer Level Capping
nearly no processes after wafer bonding
Dicing

Glass Frit Bonding
still very attractive process
Costs
Process Integration

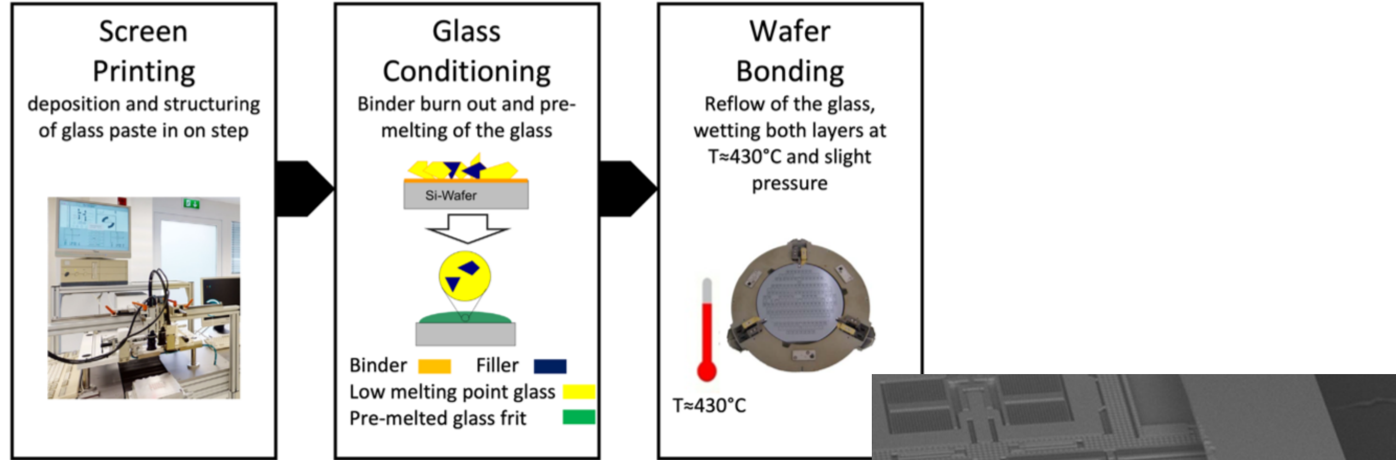
Wafer Level Packaging
many processes after wafer bonding
TSV
RDL/UBM
Bumping

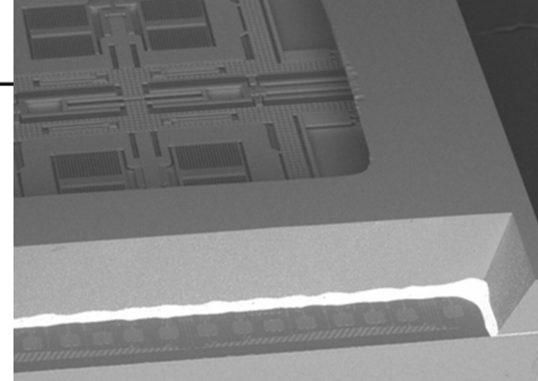


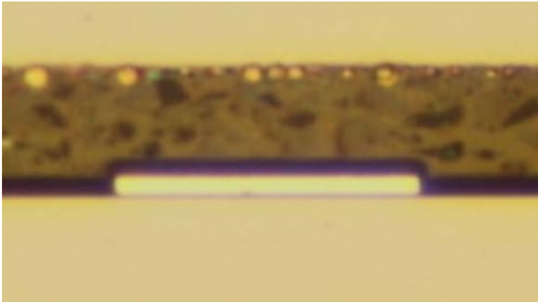


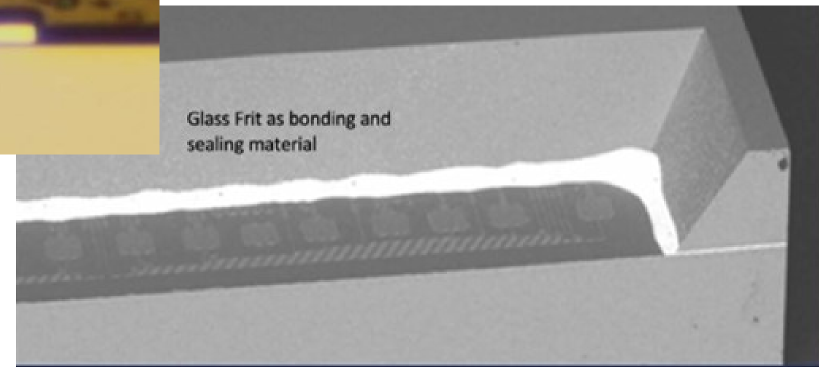
New requirements Chemical and thermal properties of glass frit materials are important for overall process integration
Maximum process temperatures after glass frit bonding
Cleaning processes

Glass Frit Bonding a short Introduction









Thermal profile for glass conditioning and bonding

Temperatur in °C

500
450
400
350
300
250
200
150
100
50
0

screen printing
drying
glazing
sealing
bonding

process steps

Microstructural details

glass and filler particles Attached to substrate by binder

slightly melted lead glass, porous structure burned binder can escape

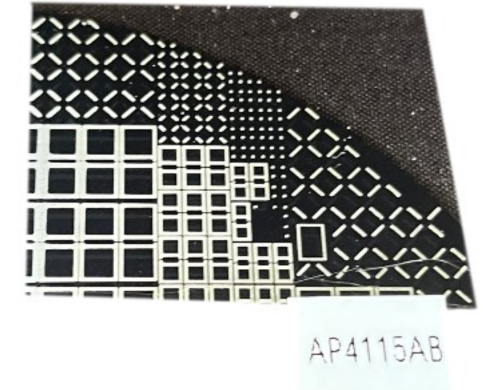
fully fired glass cleaved cross section

bonded glass frit (light gray) with embedded fillers (dark) – polished

Challenges and Current Developments
Glass Frit Bonding

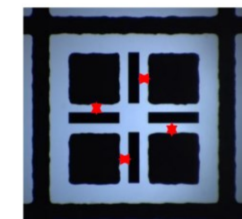
Development of Glass Frit Bonding processes based on lead free materials

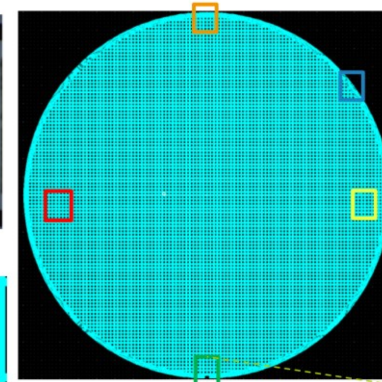
Screen Printing – Firing – Bonding – Reliability
chemical and electrical properties to be investigated
thermo-mechanical properties important - wafer bow



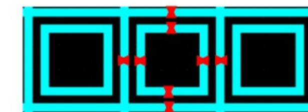
Conflicting requirements for screen printing

Small chips – small bond frames, can lead to high amount of paste covered areas - problems in release of the screen – different optimizations (screen and process) are necessary





Optimal bonding process – time, peak temperature, wafer bow, hermeticity / bonding strength



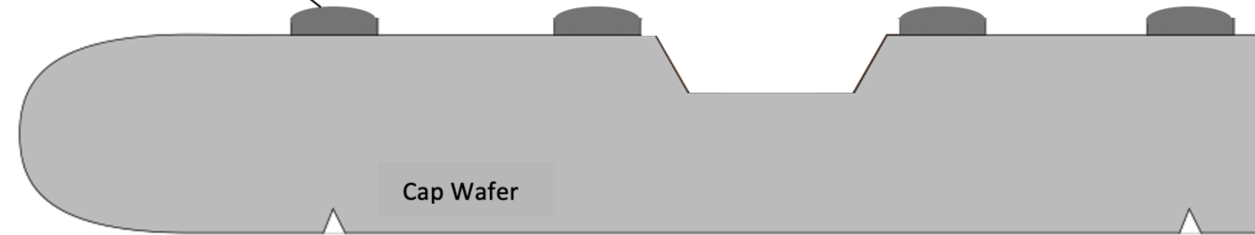
Wafer Configuration

In Wafer Process special configurations are required, such as:

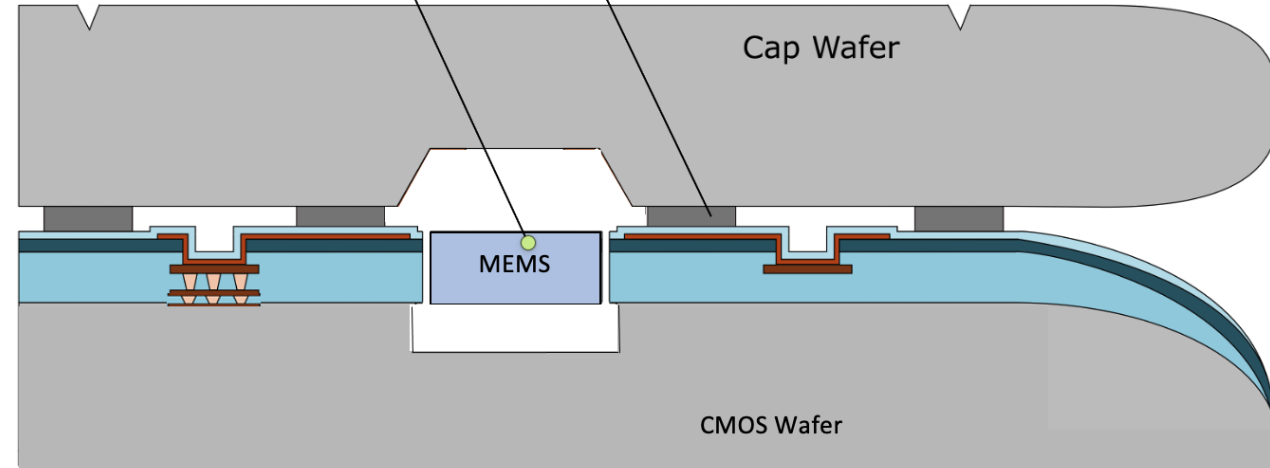
- chip and wafer edge sealing
- small edge exclusion zone
- thermal and chemical glass frit stability

… mostly related to wafer bonding.

a) cap wafer prepared for bonding: **glass frit**
– screen printed and thermally conditioned



b) Bonded wafer stack **glass frit** as bonding and sealing agent of **released MEMS**



Wafer Bonding with Electrical Contacting

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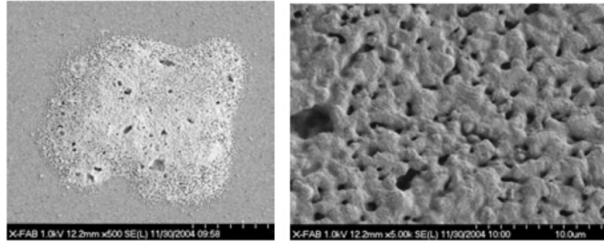
Fraunhofer ENAS

Conductive Glass Frit Bonding



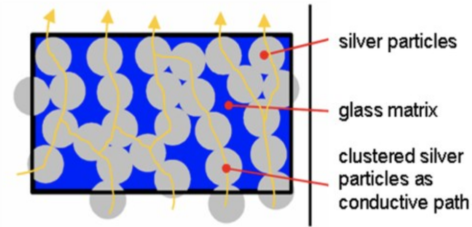
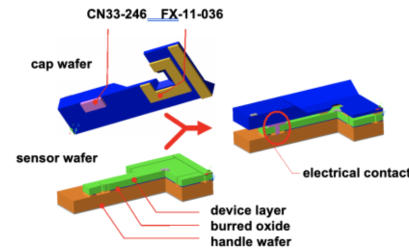


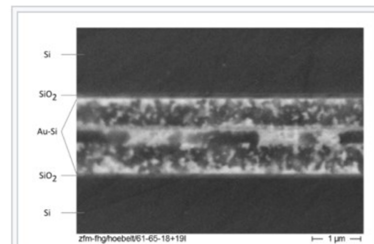
Figure 1: SEM images silver filled conductive glass frit

Figure 2: Principle of forming conductive paths in the frit



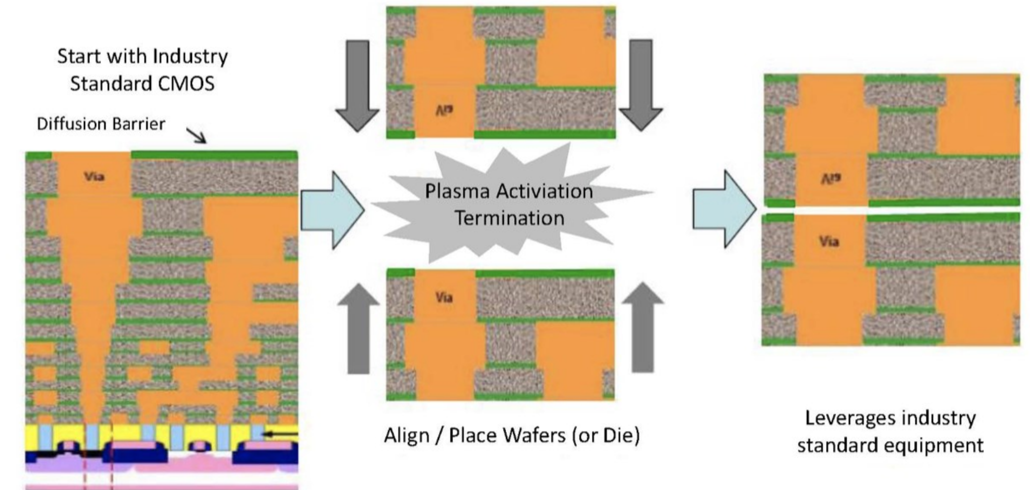
Eutectic Bonding

Lin, Y.-C.; Baum M.; Haubold, M.; Fromel J.; Wiemer, M.; Gessner T.; Esashi, M. (2009). "Development and evaluation of AuSi eutectic wafer bonding". *Solid-State Sensors, Actuators and Microsystems Conference, 2009. TRANSDUCERS 2009. International*. pp. 244–247. doi:10.1109/SENSOR.2009.5285519



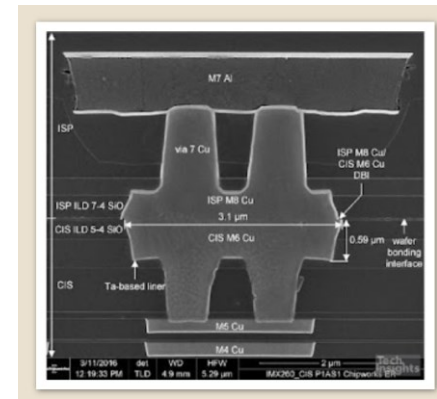
Cross-section SEM image of the bonding interface between Si and Au with 80.3 Si atom percentage.[1]

Hybride Wafer Bonding



Ziptronix Cu-Cu / Oxide "hybrid bonding" Process Flow

(Source: Permanent Wafer Bonding, Yole Développement, May 2014)



http://image-sensors-world.blogspot.com/2020/10/hybrid-bonding-review.html

TSVs – Process Selection

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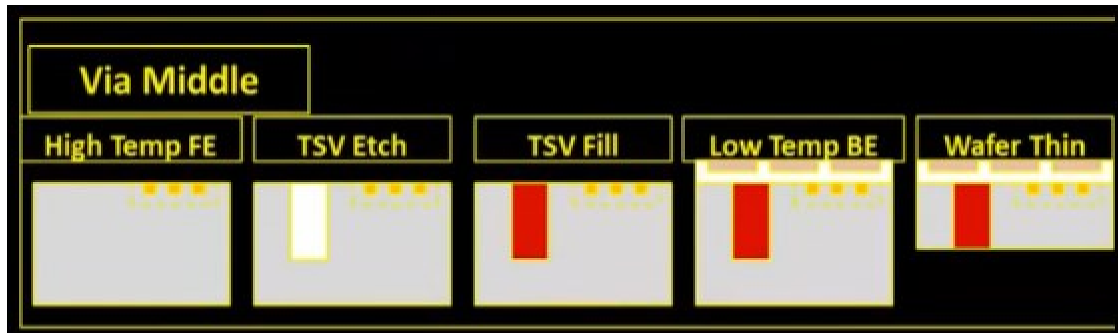
Via First: before device fabrication

→ Difficult process integration
→ Interactions with CMOS parameters



Via Middle: before metal line fabrication

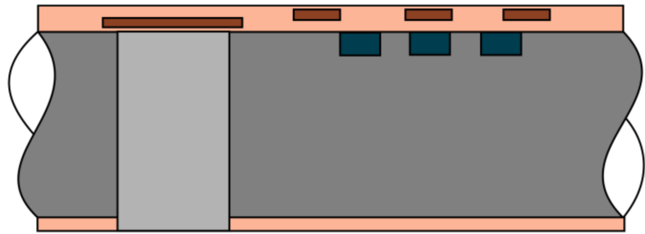
→ Difficult process integration
→ Interactions with CMOS parameters

Via Last: after metal line fabrication

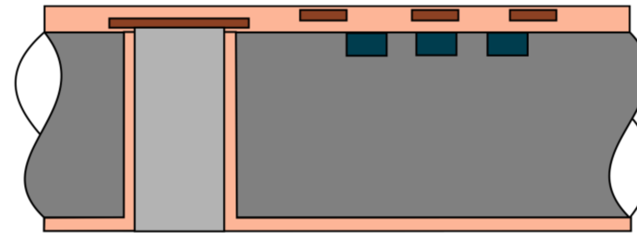
→ Independent from CMOS process
→ Independent process module
→ Universally applicable

TSV Process

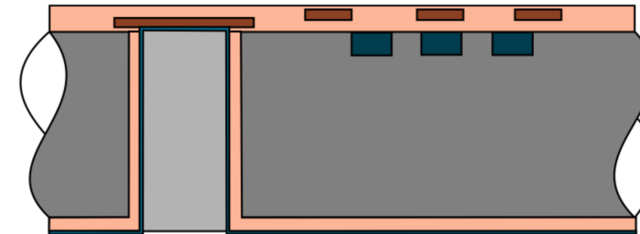
Wafer abdünnen & Ätzen der TSVs



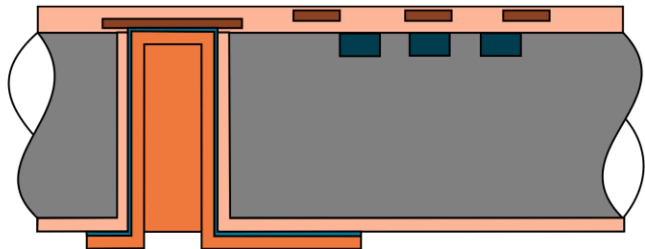
Abscheidung Isolation & Öffnen des Metallkontakts



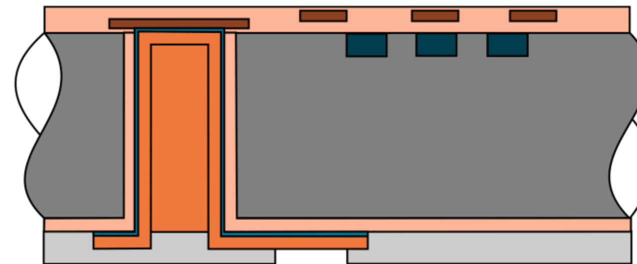
Abscheidung Barrier- und Saat-Schicht (B/S)



Galvanisches Cu & Entfernen B/S



Passivierung der TSVs



Finishing after Wafer TSV Process

Last process step of TSV is copper metallization, but this not solderable

Under Bump Metallization (UBM) is required…

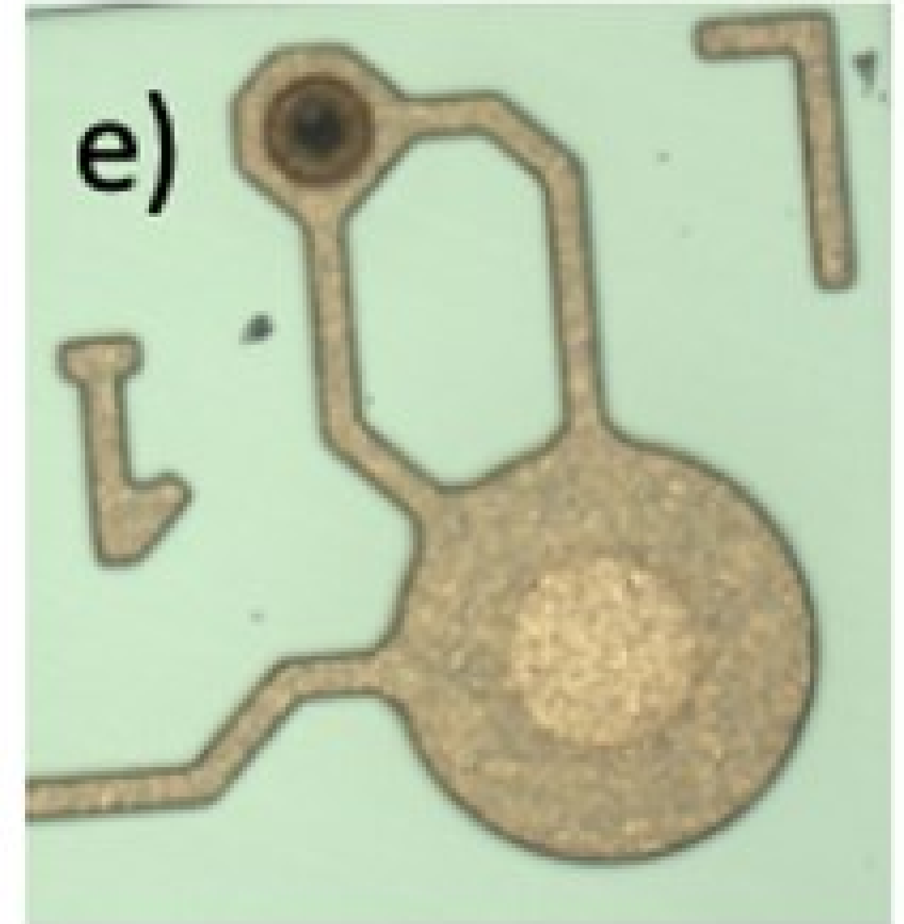
Nickel and Gold

E-less plated or sputtered (Lift off)

… and Solder Stop Layer (SolStop)

Polymers

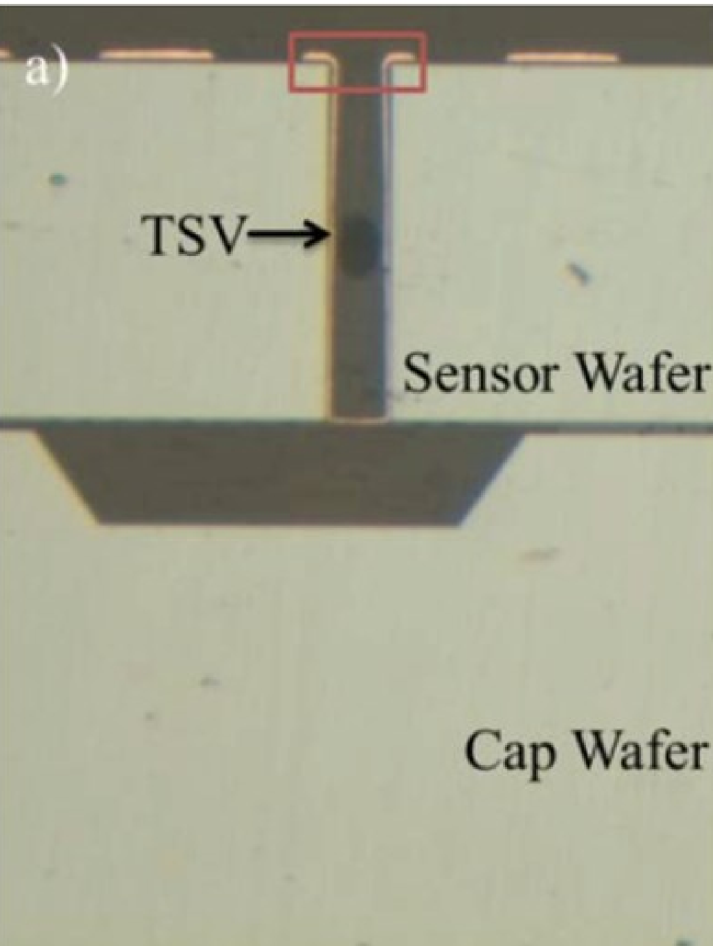
Oxide/Nitride…

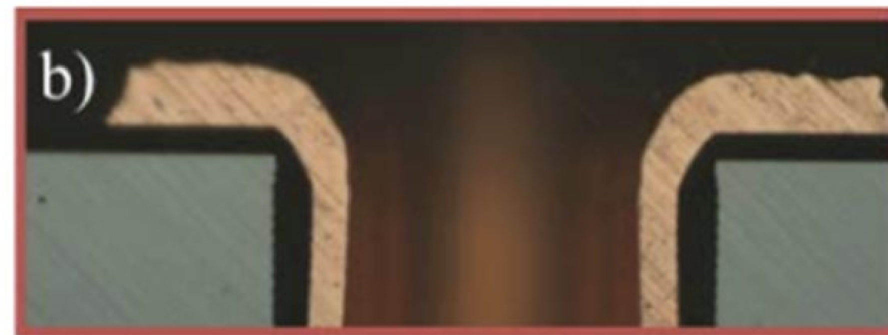


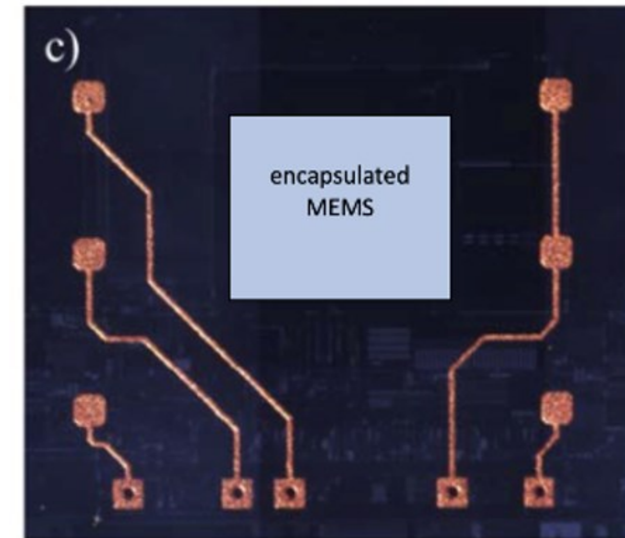
Example e-less Ni/Au at Polymer Passivation

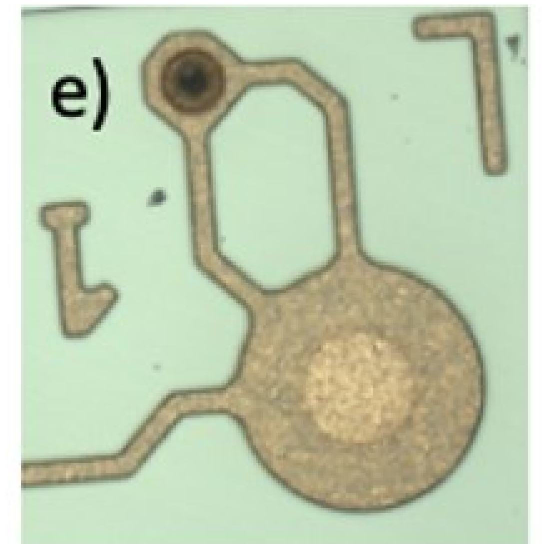
An example of a System on Chip

Chip Scale Package Solutions









Applications Aspects

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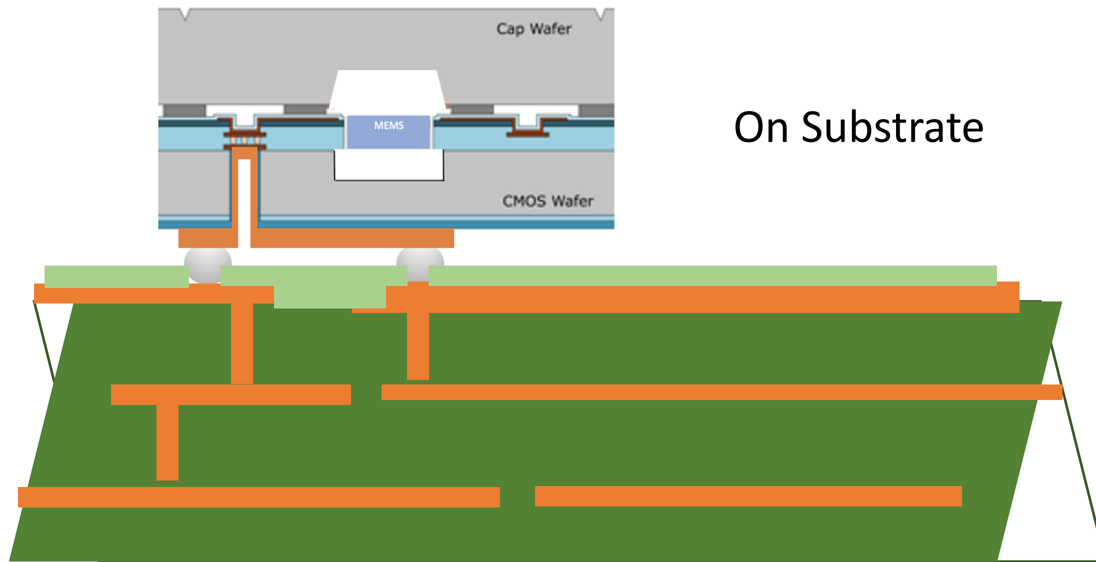
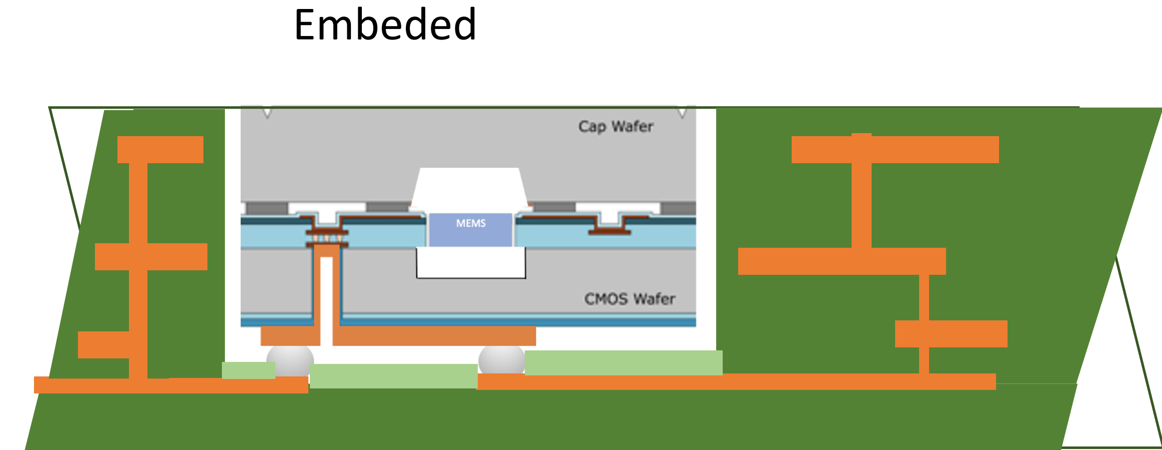
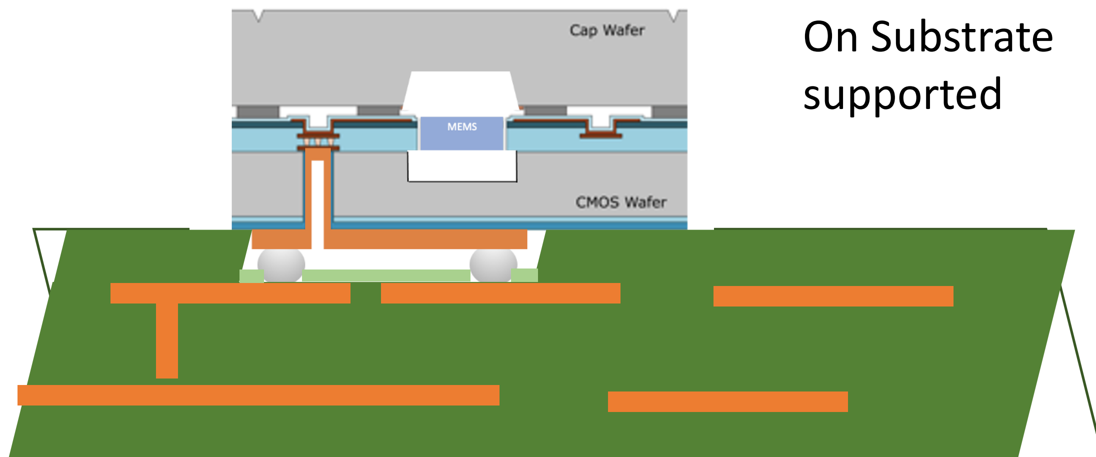


On Substrate

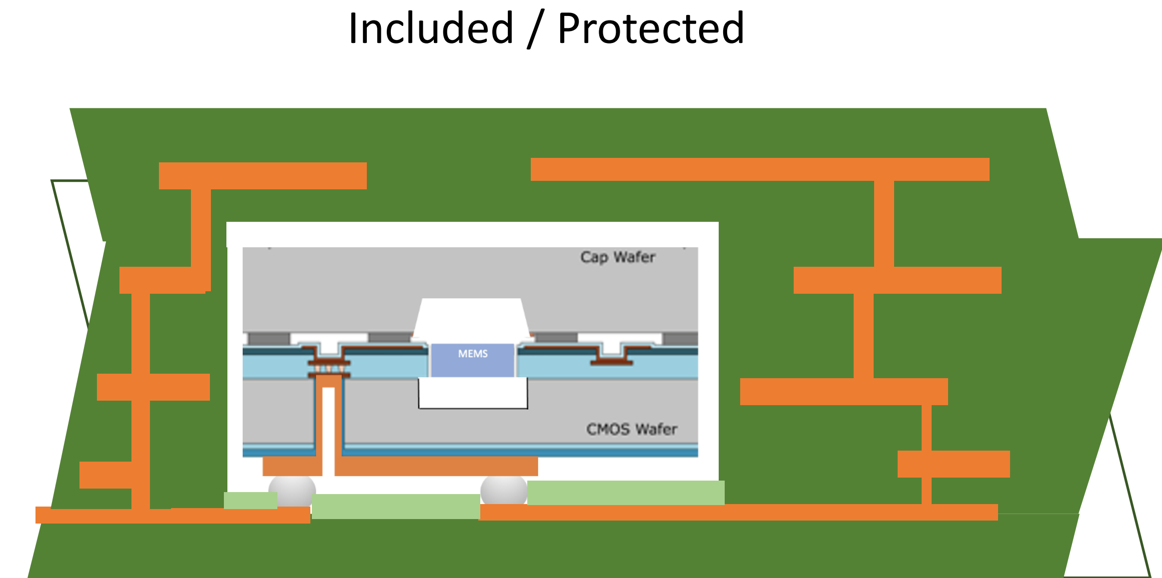
Embeded



Included / Protected



On Substrate supported



Challenges

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Wafer process

- Overall **technology integration** (e.g., thermal & chemical stability of glass frit bonding during TSV process)
- Preparation of solder process (solder balls – size, material and process; just solderable pads?)
- **Temperature limitation** (T > 250°C has influence on Cu grain growth)
- **Passivation** material (hard or soft, hydrophobic)
- **Dicing** of bonded wafer stack with hidden CMOS
- Supply chain (longer wafer process, but no assembly process)
- Follow up of commodity products (smaller CSP – out of standardization)
- **Shipment forms** (e.g., on trays, tape on reel)

Board or ceramic mounting

- **Total temperature budget** to be considered (soldering temperature, 5x reflow, low temp. solder required?)
- Does board mounting provide some **protection** (embedded, included, underfill, glob top?)
- **Thermal mechanical stress** (operating temperature, thermal cycles and shocks)
- **Co-design of boards and chips** (bridging critical dimensions)
- **Reliability**
- Cost structures – no assembly, but higher wafer and board costs

Conclusions and Outlook

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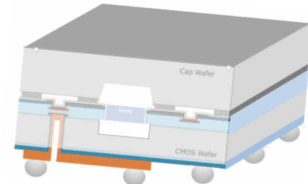
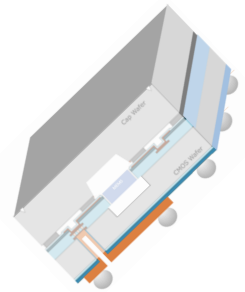
Chip scale packaged, system on chip solutions are becoming reality. They are providing extreme high integration densities - in themselves, but also for ceramic or BCB solutions (smallest possible from factor).

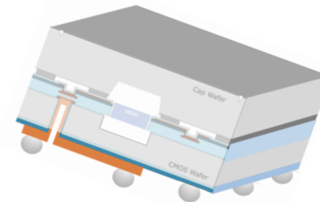


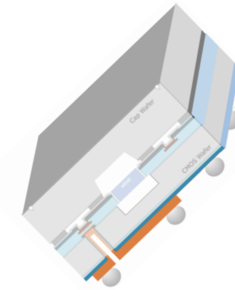
For such complex and highly integrated systems on chip, realized in wafer processes and without any single die assembly, different process blocks

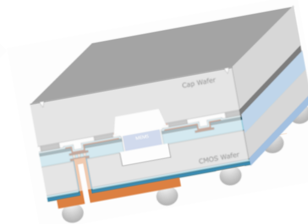
- (glass frit) wafer bonding
- TSV
- RDL, UBM, SolStop, Solder

… need to be combined and adapted to each other (process integration).









There are quite some challenges in number, but rather work to be done until all details are fitting together.

For sure, the chances of such solutions are dominating the challenges.

Acknowledgements

Roy Knechtel thanks the Carl-Zeiss-Foundation for the funding his professorship.

Thank you for your Attention!

I'm open for your questions.