AEMtec

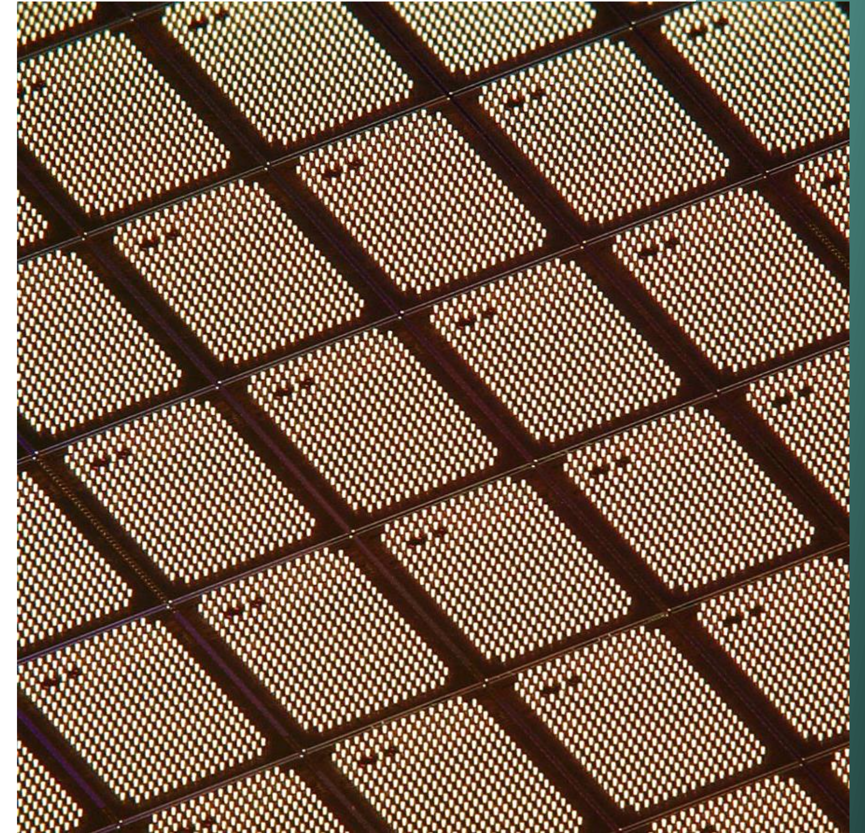
State of the art and novel wafer level solder bumping techniques

D.Lieske, 13.06.2023

37th Chemnitz Seminar
»Electronic Packaging and Applications«

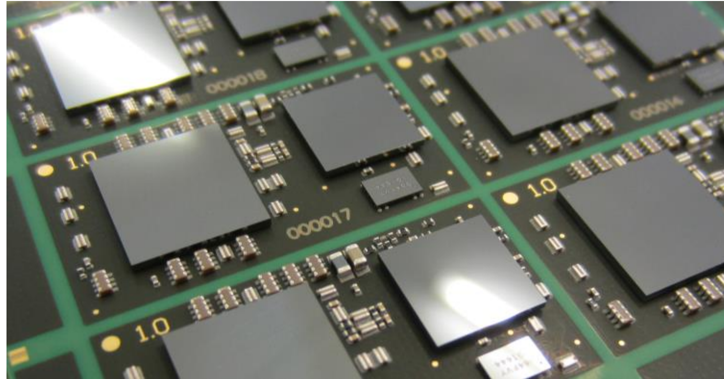
Wafer level bumping..

- is solder bump formation on wafer
- is state of the art for flip chip packaging process
- is the first choice for heterogeneous integration today
- has advantages compared to wire bonding e.g. high pin count, higher signal speed, faster for high volume
- is required for many more applications like Wafer Level Package, FanOut WLP or C2W (Chip to Wafer) and chiplet
- the demand is growing for the next decade

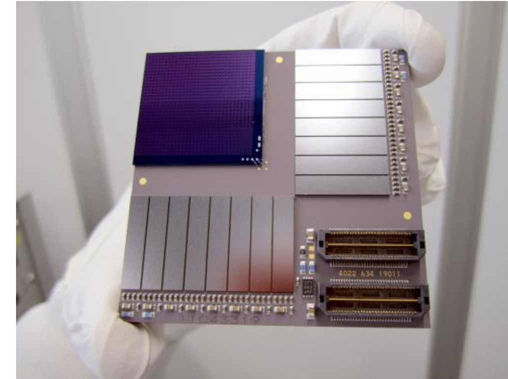


Heterogeneous integration examples

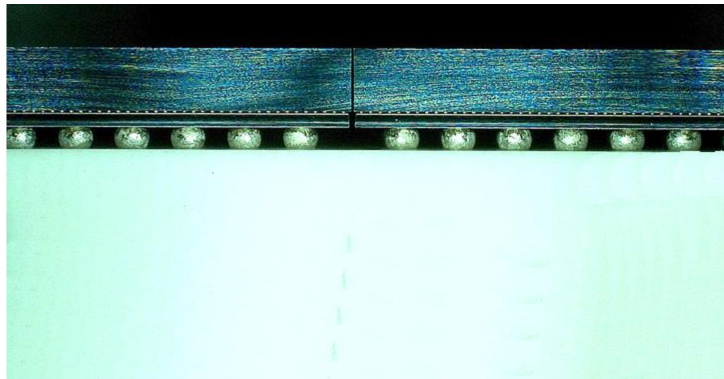
- SiP



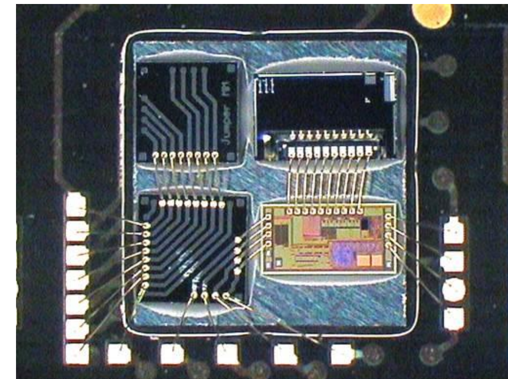
- MEMS



- X-Ray



- Sensors



Wafer level bumping – a brief introduction

- Requires a UBM solderable pad surface like NiAu, NiPdAu or Copper
- Contact pitch depending on contact size (400µm…60µm) down to 130µm +/-
- Chip to substrate, RDL interposer or Chip to chip interconnections (e.g. Bunch of wires) possible
- High pin count require fast process solutions, wire bonding for 500+ interconnects is not the best solution for Mass production
- Applications are for computing in nearly every new application and every market segment, (Asic controller, RF applications, image and signal processing,…)

Wafer level bumping process methods

With solder alloys

- UBM + Ball drop (very flexible, fast and less costly, any alloy types, large and small pitch, all SAC, low melting (BiSn, InSn48) and high melting (PbSn10))
- UBM + C4 electroplating (ball or copper pillar bumps, requires lithography, lowest pitch, limited alloy types)
- Solder printing

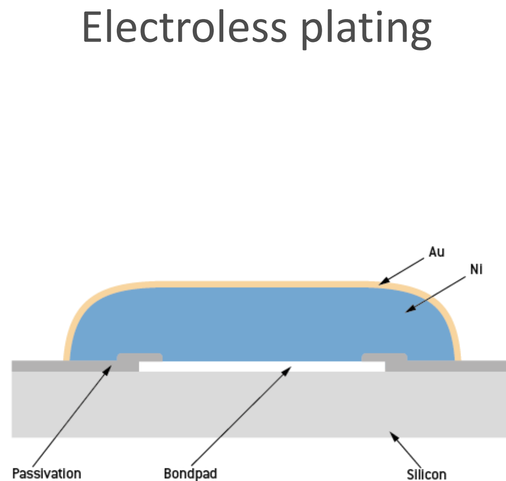
Others

- Au stud bumping (flexible, low cost, thermocompression)
- Electroless Nickel or NiAu bumping (small pitch, thermocompression e.g. ACF)

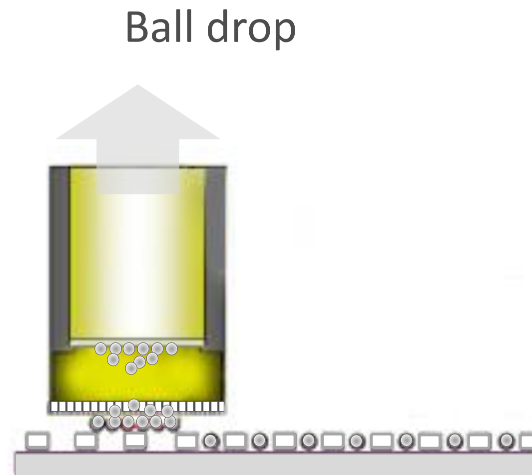
Wafer level bumping with Ball drop process

- Process is capable up to 3 Mio bumps per Wafer for 6 – 12 inch wafer

Electroless plating



Ball drop



Qualified*1)

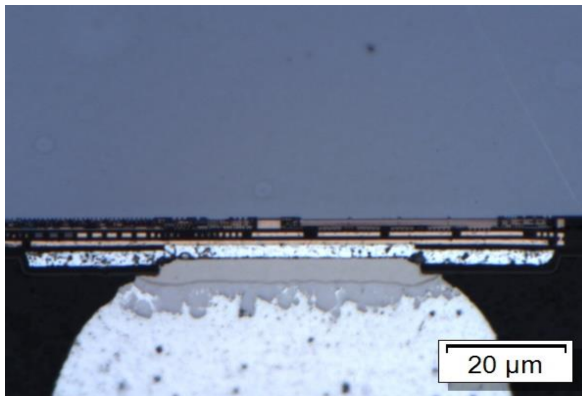
Method	Parameter	Duration	Rslt
Temperature Cycle Test	T_{high} = 125°C T_{low} = -55°C	2000 cycles	✓
High Temperature Storage	T = 150°C	1000 hours	✓
Temperature Humidity Storage	T = 85°C Φ = 85 % r. H.	1000 hours	✓

*1) UBM and Wafer level bumping is a qualified process, additionally it has to qualified via package qualification, depending on solder alloy type and application

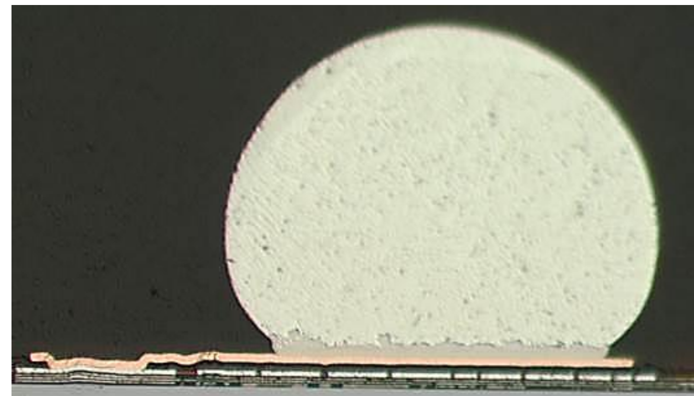
Typical Combinations of UBM and Solder

- UBM (electroless plating) and solder bumping AEMtec
- UBM (Electroplating) with or without RDL and solder bumping AEMtec
- UBM (Electroplating) solder bumping via plating other OSAT‘s

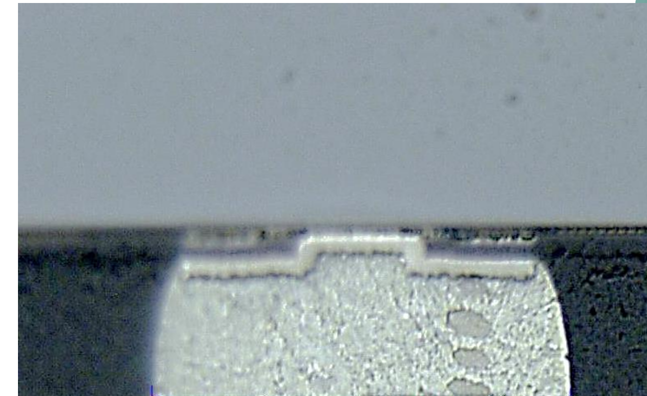
Electroless UBM + Ball drop
(AEMtec)



RDL + Ball drop
(AEMtec)



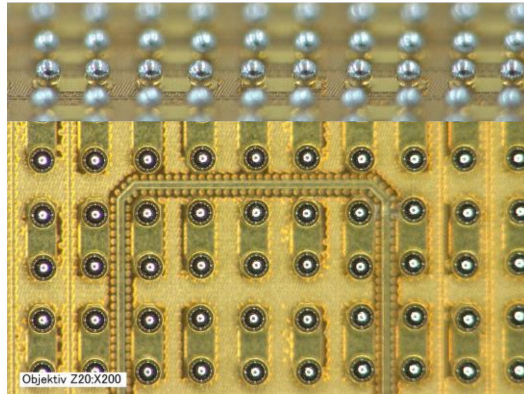
Electroplating UBM + Electroplating Solder
(other)



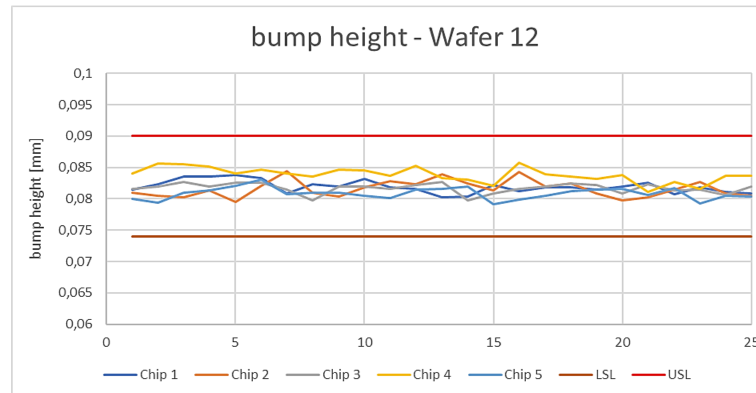
Properties of Solder bumping and results

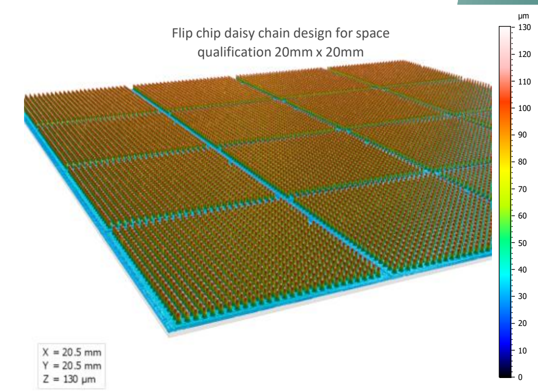
Benefits

- Fast process, no plating chemistry
- Accurate solder bump positions before reflow
- Stable bump height after soldering due to precise preform spheres



bump position before soldering





bump height distribution within +/-5µm (95µm ball diameter)

Properties of Solder bumping and results

Benefits

- Any solder alloy possible, fast exchange of allow type, fast product change
- Process is capable for double sided wafer with surface on backside which must not get into contact with liquids

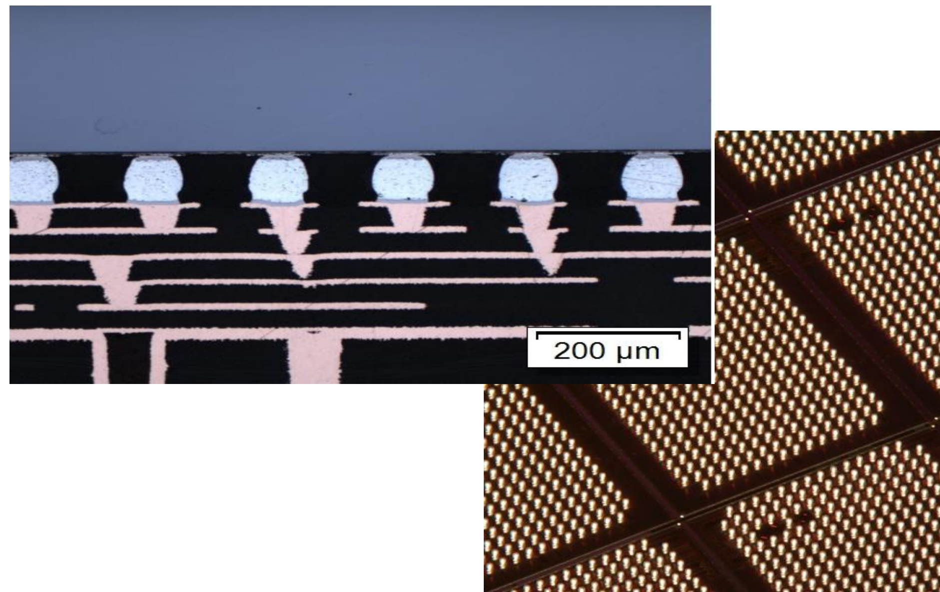
Con

- Flux cleaning required for water soluble flux or no clean flux possible without cleaning*1)

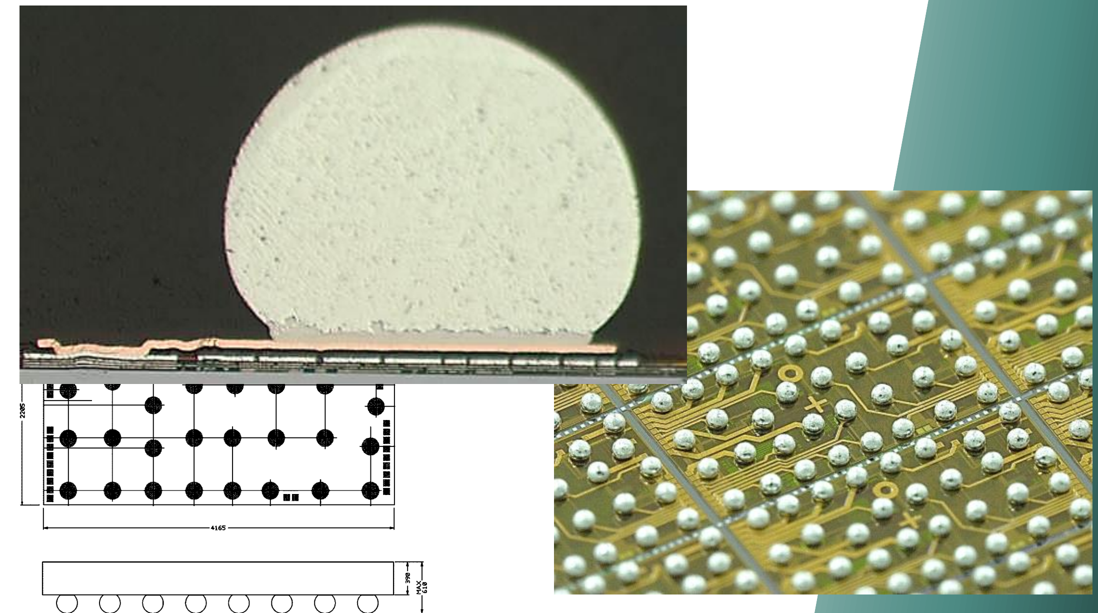
*1) No clean flux requires qualification with final product assembly process

Basic Applications

- Flip Chip package



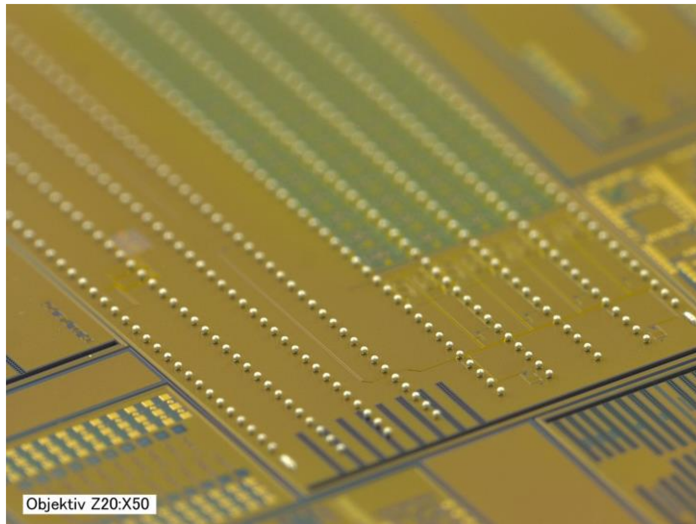
- WL-CSP



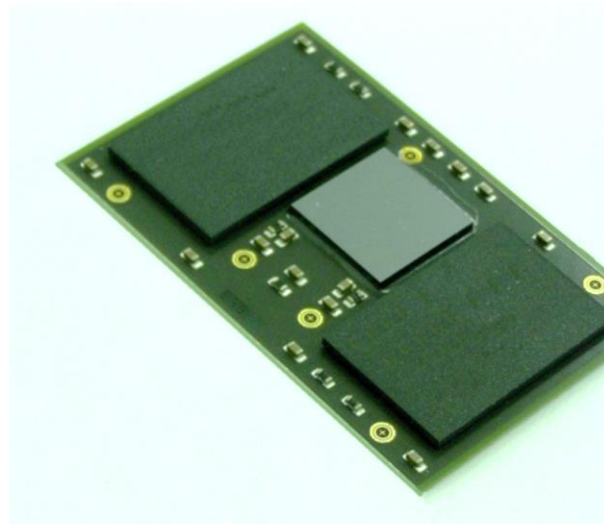
- Application: SIP/ MCM, Flip Chip package, RF package, Smart systems (optical-, gas-, liquid-, sensors, accelerometers,…), telecommunication, bit coin, medical, …

Novel Applications

- Silicon photonics



- ADAS



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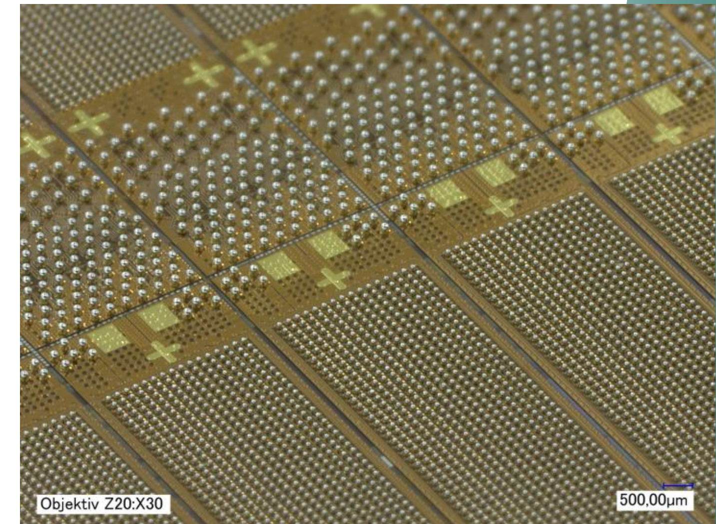
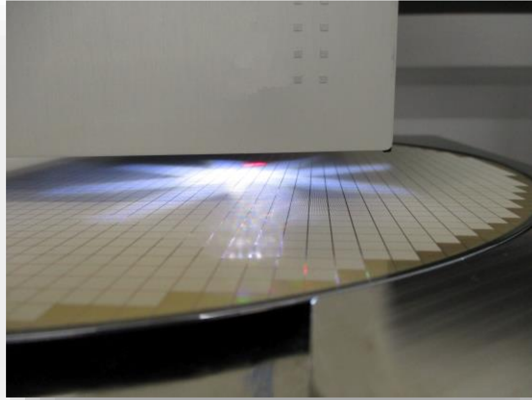
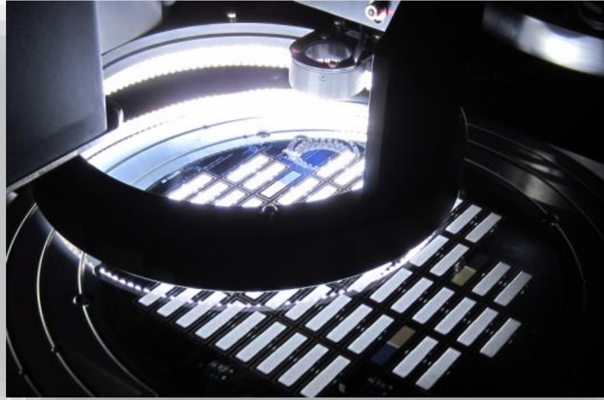


- Different solder sphere diameter on the same wafer is possible *new)
- Photonics SIP, HPC (high bandwidth, high speed) AI, autonomous driving, CdTe sensors

Unique wafer level bumping & Semiconductor packaging in Europe





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- ✓ Worldwide Customer Network
- ✓ Strong Institutes Network
- ✓ Strong Foundry Network

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