GLASS FRIT WAFER BONDING FOR ENCAPSULATING MONOLITHIC INTEGRATED CMOS-MEMS DEVICES

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Introduction

- CMOS-MEMS integration is an area of focus for X-FAB. Having both basic processes available in one foundry allows the realization of very complex technologies and advanced customer products. But to be successful, interactions of all processes need to be understood and managed.
  - MEMS transducers typically sense or control physical, optical, chemical properties, they are electrical interfaces to the "outside world"
  - Nearly any MEMS sensor or actuator needs dedicated ASIC for signal conditioning, conversion, communication, storage,..

➔ Combining both at one and the same chip as monolithic integration provides various benefits:

- Smaller system dimensions or form factor – important for mobile devices
- Increased performance: lower parasitic, lower power, higher reliability
- Cost saving potentials on device / system level

Why a general case study…

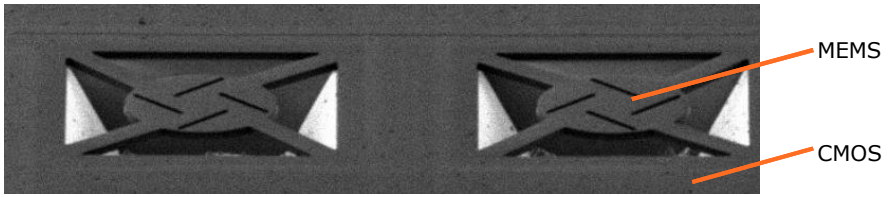
- CMOS MEMS integration is quite complex and can only be discussed in a good way on an example
- CMOS technologies are quite modular, generic and available as open platform technologies
- In the MEMS world there is still the 1st MEMS Law – any application needs its own technology, this leads to customer specific developments
- When combining CMOS and MEMS we will be with the MEMS part still in the field of special customer specific solution

➔ So there is not the one integration platform, but concerning technology examples we can reflect general conclusions and learnings,…

… in this sense I would like to give a general case study.

Describing the case study

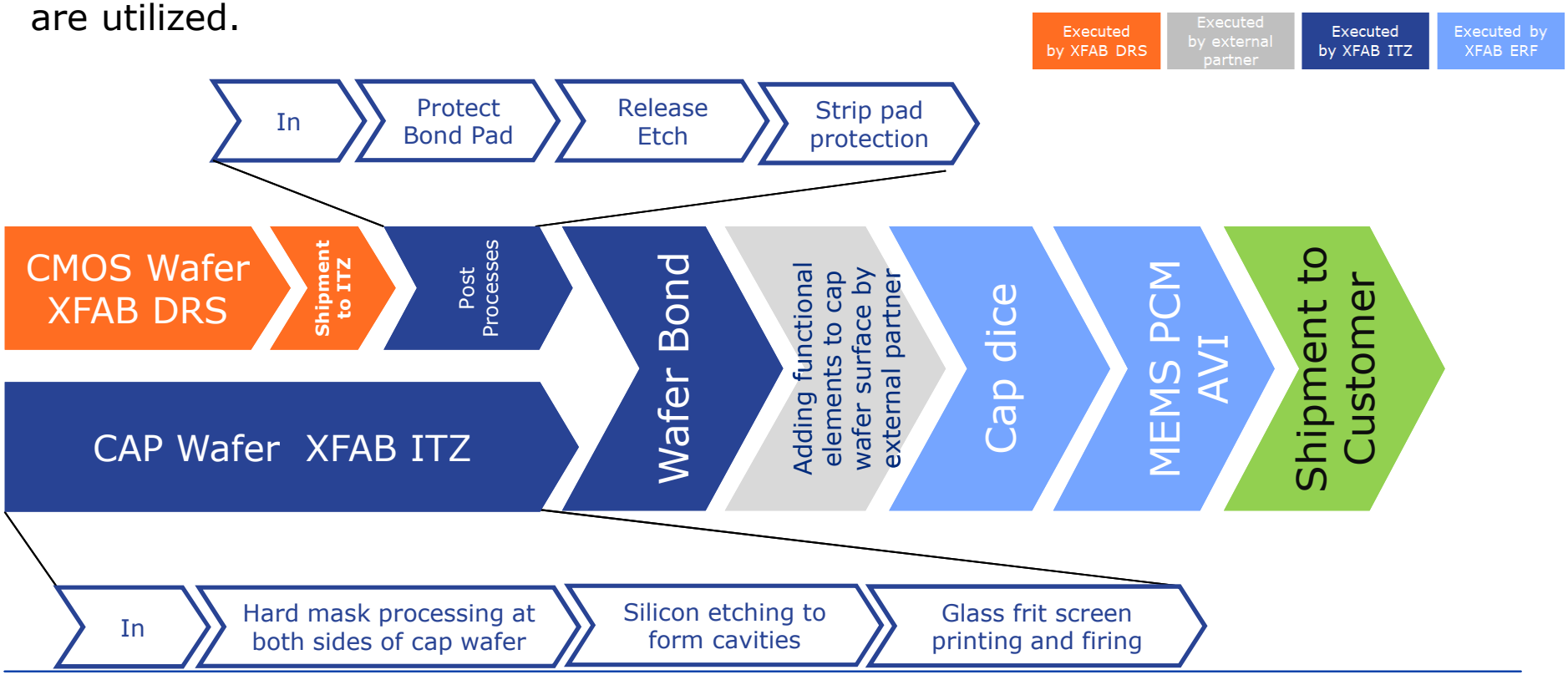
- This case study addresses a XA035-based integrated sensor. The sensor structure is constructed using standard features of the CMOS components. To reach the required performance, on chip ASIC including memories are needed. To make the sensor functional, parts of the CMOS structures need to be undercut by a silicon etching from the wafer front side.



- The result is a freestanding MEMS structure. This structure can either mechanically move or be used to detect thermal radiation. Structures are fragile and can be easily disturbed by particles or dust – Wafer level capping is required (wafer bonding process)

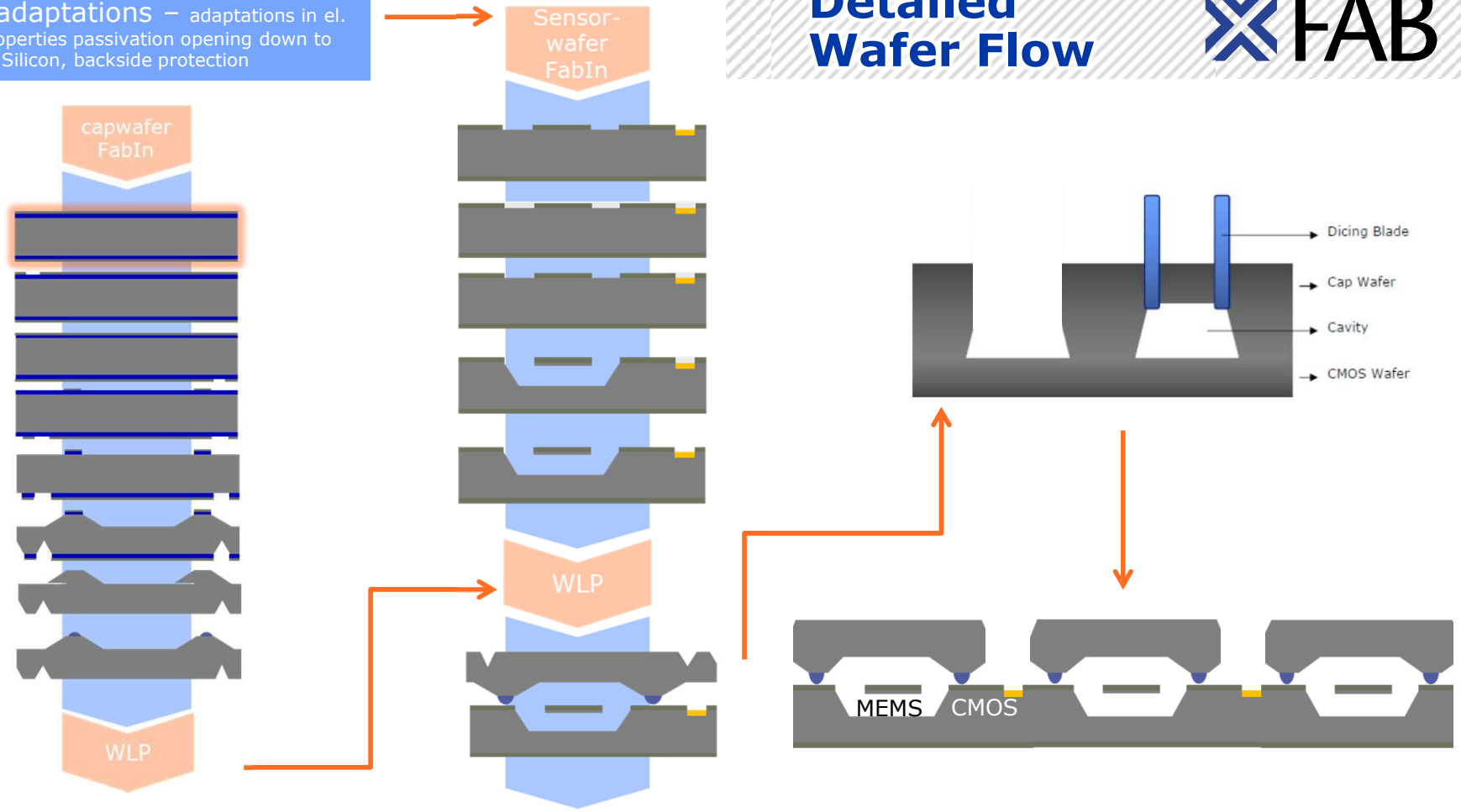
The principle flow

- To get the best possible process, the key competences of different X-FAB sites are utilized.



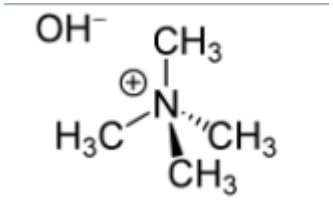
Detailed Wafer Flow

XA035 based CMOS Process with MEMS adaptations – adaptations in el. Layer properties passivation opening down to Silicon, backside protection

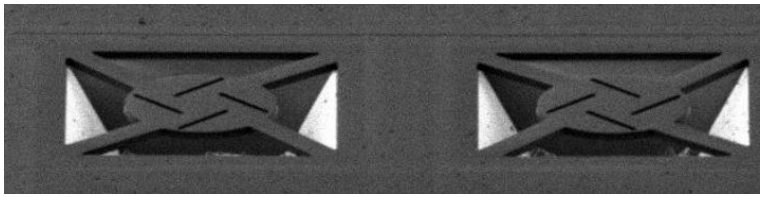


Special Process Step - Release Etch

- To make the sensor functional, parts of the CMOS structures need to be undercut by a silicon etching from the wafer front side.
- This etching step needs to be done in a CMOS compatible way – the introduction of critical mobile ions needs to be prevented.
- TMAH – Tetramethylammoniumhydroxid- was chosen to allow a CMOS compatible release etching.

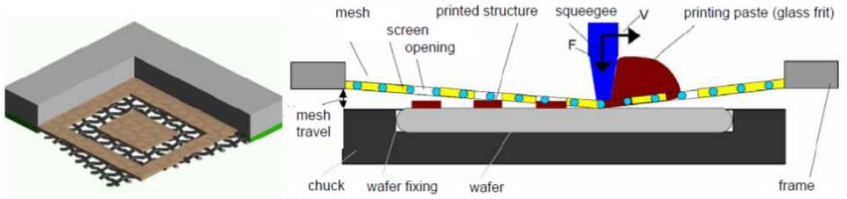


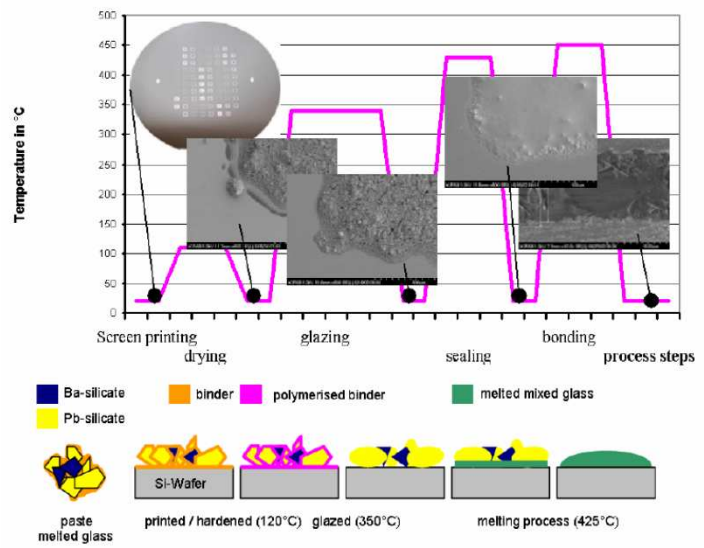
- But it turned out that this chemical is too aggressive: it destroys the bond pad – a buffered version of this chemical is much softer, to the pad - but requires very well defined processing conditions.
- A pad protection was even with the buffered chemical needed for high pad quality.

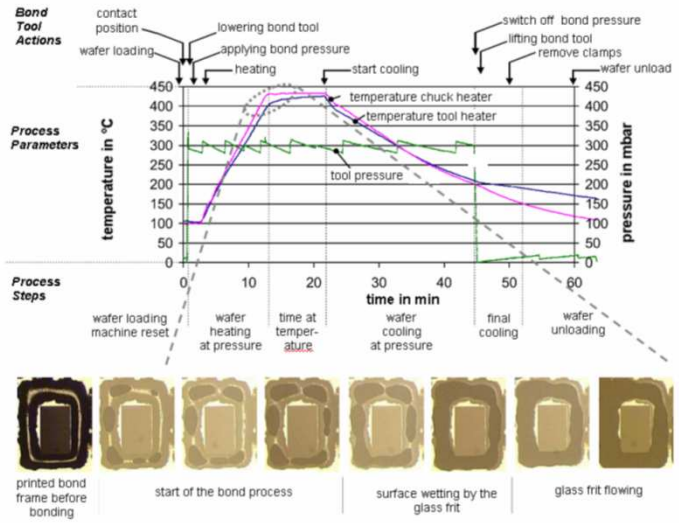


Glass Frit Bonding

- Glass Frit Bonding is an universal bonding process which can be applied on CMOS passivation.

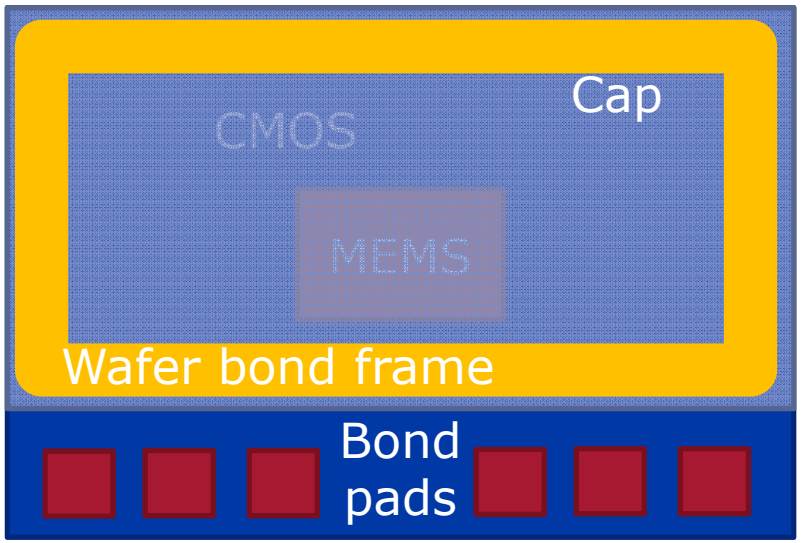






MEMS CMOS layout

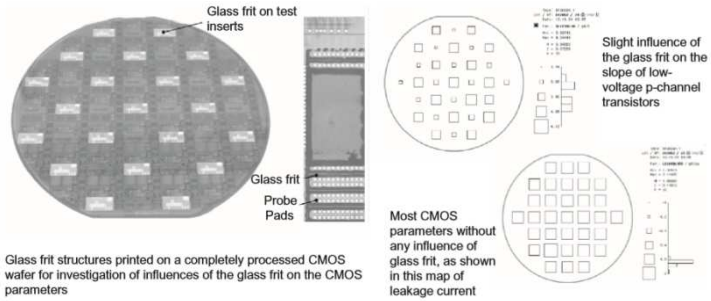
- To be economically successful, the chip area has to be used quite efficiently by a dense MEMS CMOS Design.



- Glass frit wafer bonding frame has to be over CMOS
- Wire bond pads ideally one chip side
- MEMS embedded in and close to CMOS

Technological Issues – Glass Frit Material

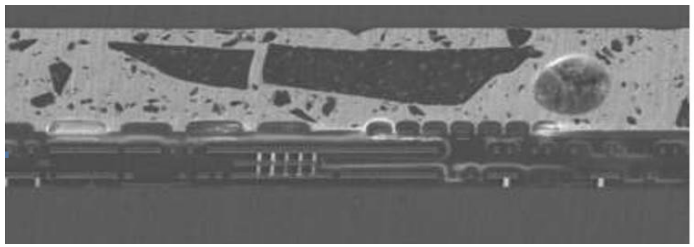
- Glass frit on CMOS tested as basic investigation at glass fit development



Glass frit structures printed on a completely processed CMOS wafer for investigation of influences of the glass frit on the CMOS parameters

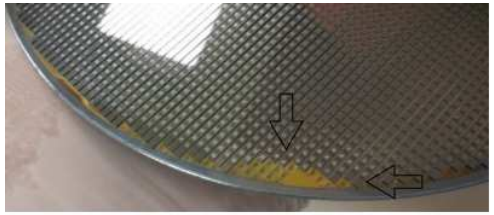
- At real process integration, damages of the electrical CMOS structures were noticed in wafer probing – root cause too large filler particles cracking passivation

- Counter measures successfully applied
  - Using glass frit material with smaller filler size
  - Flat passivation to avoid local stress concentrations
    - Another MEMS triggered modification of the CMOS process (module selection)

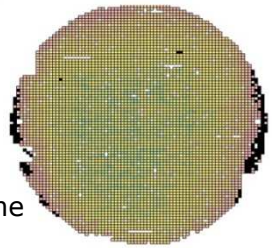


Glass Frit Yield

- Complex wafer processing is combined with high processing costs. This sets the overall yield in focus.
- One important aspect here is the wafer bonding yield – this has actually two aspects
  - Preventing lost caps in cap dicing process – lost caps are making problems in alter processing like wafer backside grinding



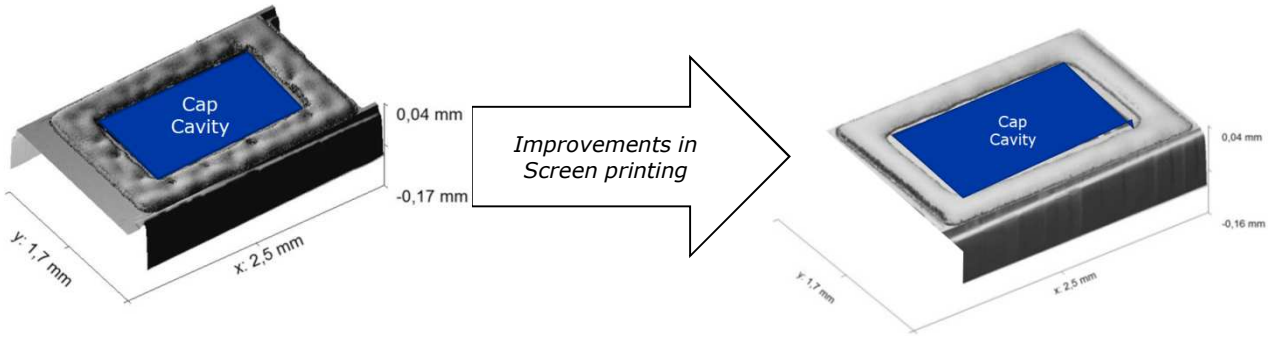
  - Non-hermetic dies – if the MEMS structure is not hermetically sealed, it is not full functional regarding performance and in addition we see various reliability risks
    - Non-hermetic dies can be detected in wafer sort test



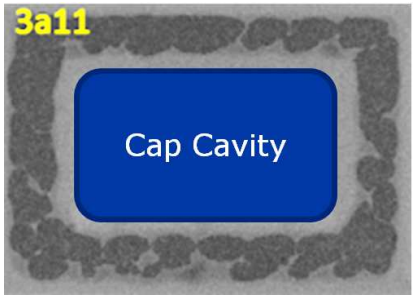
Black dies = leaky wafer bond frame

Glass Frit Wafer Bonding Improvements

- To improve the wafer bonding two main steps were required:
  - Better screen printing to have especially at wafer edge a well defined glass thickness



  - Slightly increased wafer bonding temperature
    - Let the glass flow to get a hermetic sealing



Incomplete glass flowing
no sealing

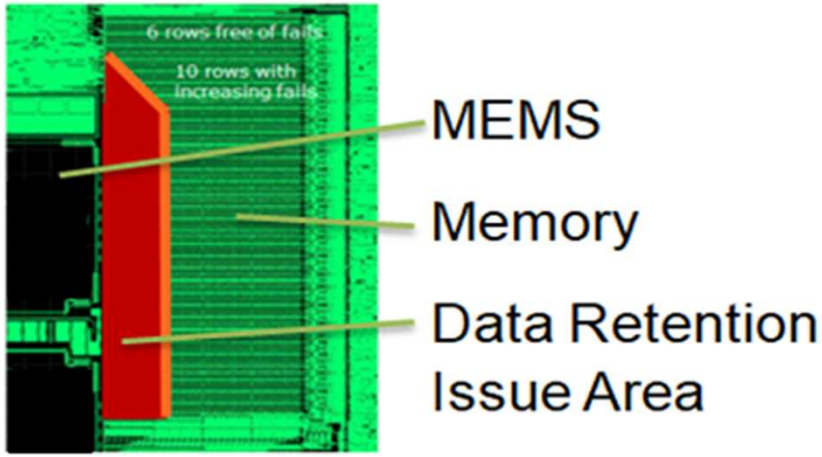
Complete glass flowing
sealing

MEMS CMOS Interaction

- To make the sensor functional, parts of the CMOS structures need to be undercut by a silicon etching from the wafer front side. This requires the opening of the CMOS passivation to get access to the silicon. This opening was identified as problematic, especially regarding its impact on memory blocks located nearby (data retention).

- At not hermetically sealed dies, Data retention issues were seen in a memory area close to the MEMS cavity – this is related to the required opening in the passivation

- By hermetic bonding this is prevented – the cap closes the gap in the passivation



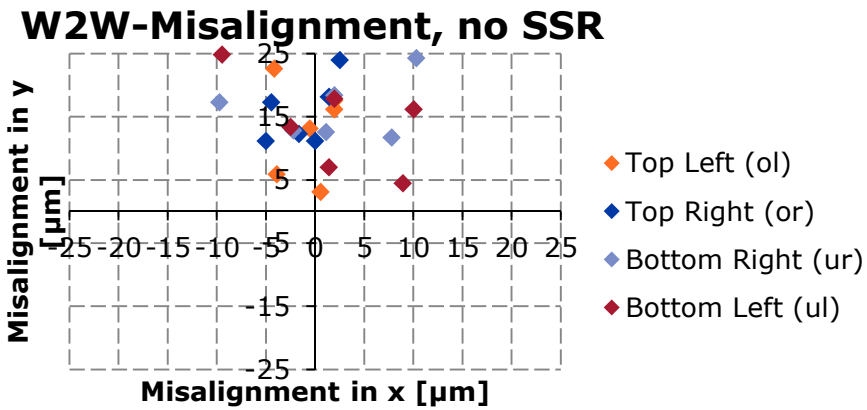
SEQUENTIAL-SPACER-REMOVAL-FUNCTION

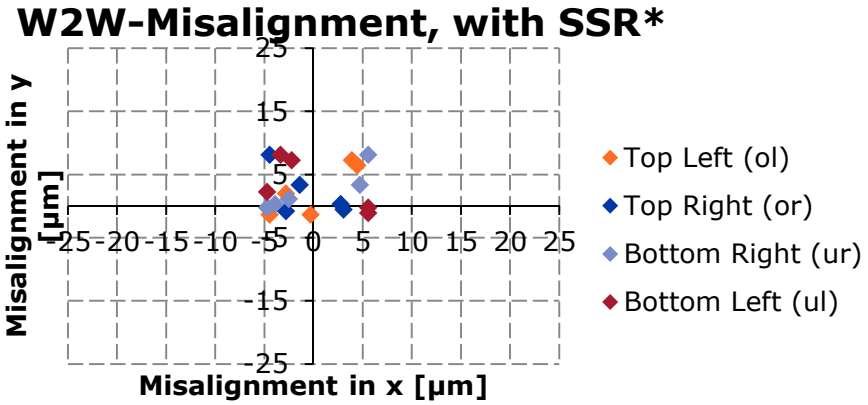
Purpose: Reduction of the W2W misalignment induced during the Bondingprocess

Approach: Sequential Spacer Removal instead of Simultaneous Removal of Spacers, combined with the temporary opening of the corresponding Clamps.

Material: 2 Batches of 6 Wafers, Misalignment was measured at 4 Points of each Wafer

Results: Significant improvement of the W2W misalignment as well as it's repeatability



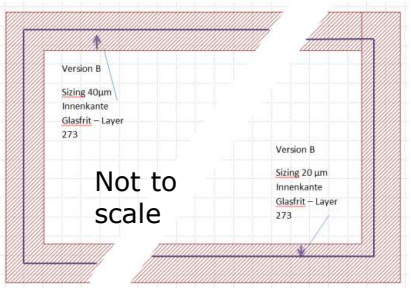


Ppk-Comparison	Ppk for Alignment in x	Ppk for Alignment in y
W2W-Misalignment, no SSR	1,55	0,57
W2W-Misalignment, with SSR*	2,06	2,07

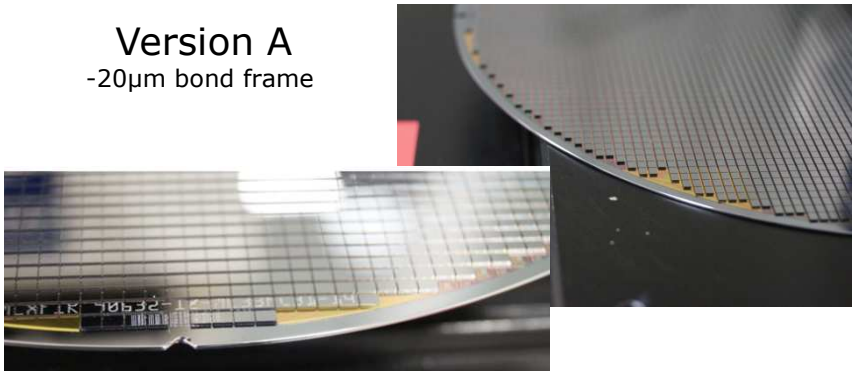
*The Misalignment of one Wafer from the Batch was not taken into consideration, since it's high Misalignment was the result of a handling Mistake during the loading of the Bonder

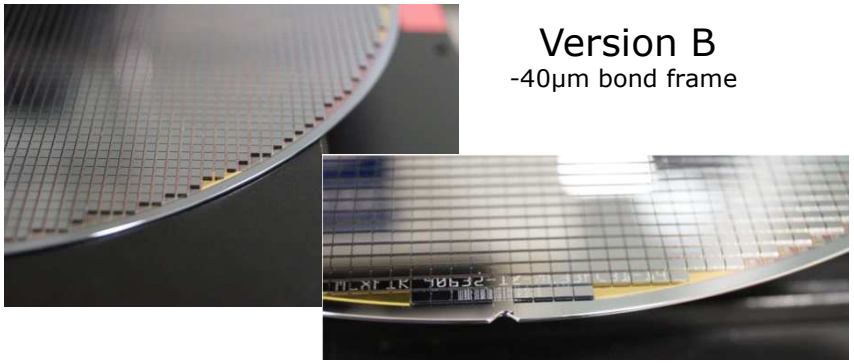
Smaller Glass Frit Bond Frames

- In terms of area consumption smaller glass frit bond frames are very attractive, so after the general glass frit bonding process improvements, smaller bond frames were tested at short loop wafers
  - The Glass frit bond frames were sized in two versions from their inner side
  - Screen printing was done with very good results
  - Bonding was done using the standard bonding recipe
  - In cap dicing nearly no caps got lost



Version A
-20µm bond frame



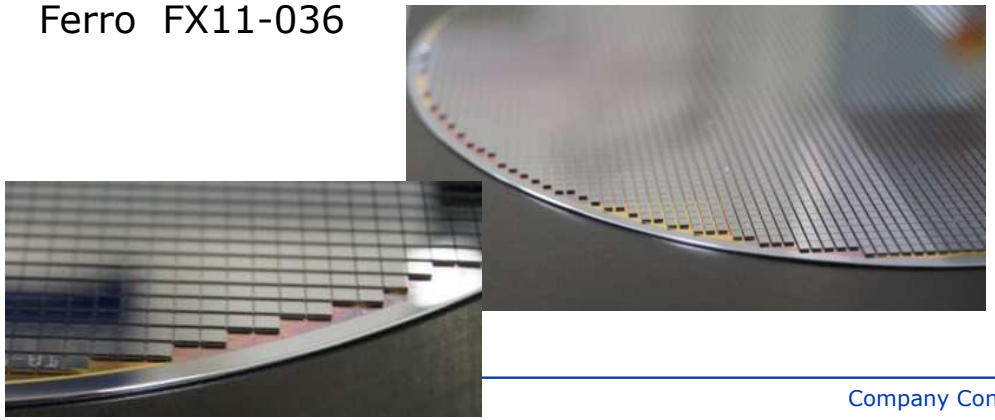


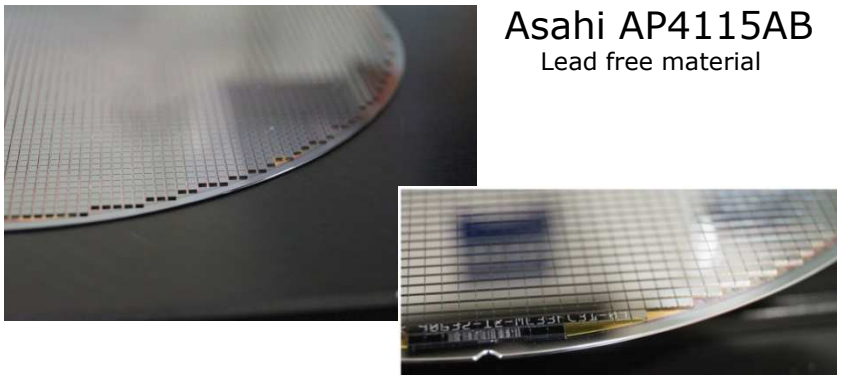
Version B
-40µm bond frame

Alternative Glass Frit Materials

- Due to different reasons alternative glass frit materials are interesting and are in evaluation
  - Lead free material due to new environmental protection standards may show up in future
  - Improved sensor functionalities for next generations – low vacuum sealing
  - Two alternative glass materials were printed and thermally conditioned by ENAS
  - Bonding was done using the standard bonding recipe
  - In cap dicing nearly no caps got lost

Ferro FX11-036





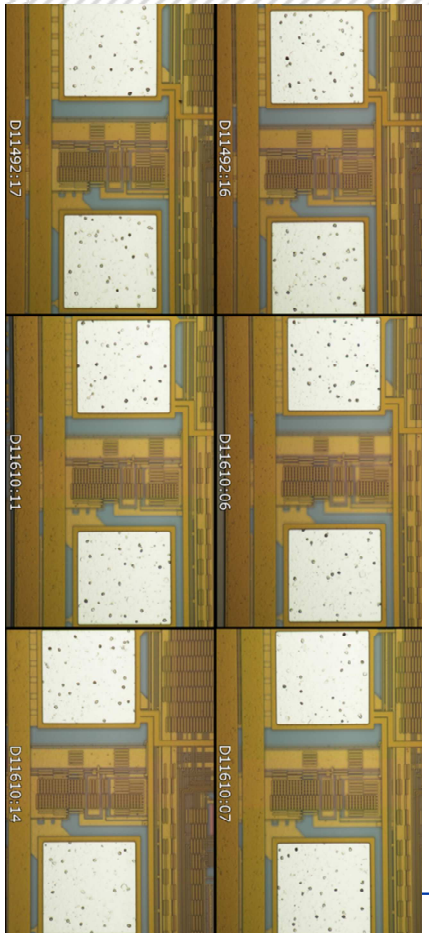
Asahi AP4115AB
Lead free material

Wire Bond Pad Quality (1)

- In MEMS processing, especially for CMOS integrated MEMS, the wire bond pad quality is essentially, but difficult to be maintained.
- Usually pads are opened at the end of the CMOS process – to allow CMOS PCM test, but open pads (aluminium or aluminium-copper) are sensitive to chemical and electrochemical reactions or corrosion
- On the other hand, in the MEMS processing chemicals, water, plasmas, temperatures,…

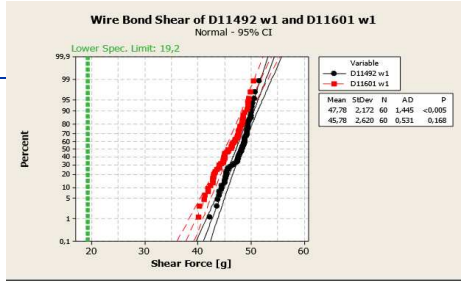
  … are acting necessarily to the pads when doing the MEMS processing and can harm them.

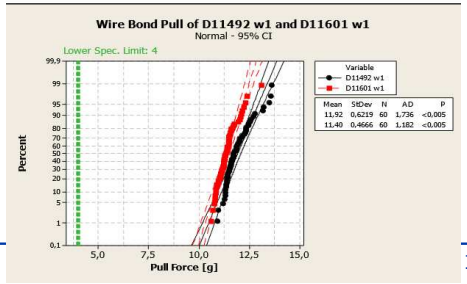
Wire Bond Pad Quality (2)



- The bond pad quality can be well maintained over a long and complex process, from opening the passivation until the last process step. Here many process steps are optimized to not harm the pads – actually it is recommended to protect the pads as best and as long as possible, but finally we have here an important process integration topic

- At the end wire bond pads are made for wire bonding. So beside the optical appearance the wire bond process has to be checked as well – wire pull and wire sheer tests are done and showed very good results





What else is important?

- When combining MEMS and CMOS to one complex process for advanced devices many other points need to considered…
  - Wafer edge engineering – avoid critical thin or sharp edges which causes problems in the processing or can generate particles
  - Defined scribe lines to avoid issues
  - Wafer backside quality – in this case the backside needs to be protected against uncontrolled etching or thinning in the MEMS release process
  - Wafer traceability – keep wafer number readable over complete process also after wafer bonding (e.g. back side laser marking)
  - Consider assembly and packaging process needs
  - Holistic process control concept
  - Overall yield management

  … and much, much more.

Summary and Conclusions

- CMOS-MEMS integration is an area of focus for X-FAB. Having both basic processes available in one foundry allows the realization of very complex technologies and advanced customer products.
- But to be successful interactions of all processes need to be understood and managed.
- MEMS structures and processes may generate problems,
  - such as necessarily passivation opening to allow MEMS release process, but generating weak points the CMOS part can be attacked by ions
  - Chemical and electrochemical wire bond pad attack
- But the MEMS processing could also solve this issue: here a cap wafer has to be hermetically bonded to protect the MEMS and to provide a defined atmosphere and it is closing the gap in the passivation.
- Finally, all is about process understanding and integration to make benefit out of combining MEMS and CMOS and avoid any critical negative influences.
- Very important here is the cap wafer bonding using a glass frit– understanding and optimizing this process Fraunhofer ENAS provide excellent support.

MANY THANKS Fraunhofer ENAS